DIO59020
USB-Compliant Single-cell Li-Ion Switching Charger with USB-OTG Boost Regulator

Features

- Fully Integrated, High-Efficiency Charger for Single-Cell Li-Ion and Li-Polymer Battery Packs
- Faster Charging than Linear
- Charge Voltage Accuracy: 0.5% at 25°C 1% from 0 to 125°C
- ±6% Input Current Regulation Accuracy
- ±4% Charge Current Regulation Accuracy
- 26V Absolute Maximum Input Voltage
- 6V Maximum Input Operating Voltage
- 2A Charge Rate
- Programmable through High-Speed I²C Interface(3.4Mb/s) with Fast Mode Plus Compatibility
  - Input Current
  - Fast-Charge/Termination Current
  - Charger Voltage
  - Recharge Voltage
  - Termination Enable
- 1.5MHz Synchronous Buck PWM Controller with Wide Duty Cycle Range
- Small Footprint 1μH External Inductor
- Dynamic Input Voltage Control
- Low Reverse Leakage to Prevent Battery Drain to VBUS
- 5V, 1A Boost Mode for USB OTG for 3.2V to 4.5V Battery Input
- Available in DFN3*3-12 Packages.

Descriptions

The DIO59020 combines a highly integrated switch-mode charger, to minimize single-cell Lithium-ion (Li-ion) charging time from a USB power source, and a boost regulator to power a USB peripheral from the battery.

The charging parameters and operating modes are programmable through an I²C Interface that operates up to 3.4Mbps. The charger regulator circuits switch at 1.5MHz to minimize the size of external passive components.

The DIO59020 provides battery charging in thr ee phases: pre-charge, constant current and c onstant voltage.

To ensure USB compliance and minimize charging time, the input current limit can be changed through the I²C by the host processor. Charge termination is determined by a programmable minimum current level.

The integrated circuit (IC) automatically restarts the charge cycle when the battery falls below an internal threshold. If the input source is removed, the IC enters a high-impedance mode, preventing leakage from the battery to the input. Charge current is reduced when the die temperature reaches 120°C, protecting the device and PCB from damage.

The DIO59020 can operate as a boost regulator on command from the system. The boost regulator includes a soft-start that limits inrush current from the battery and uses the same external components used for charging the battery.

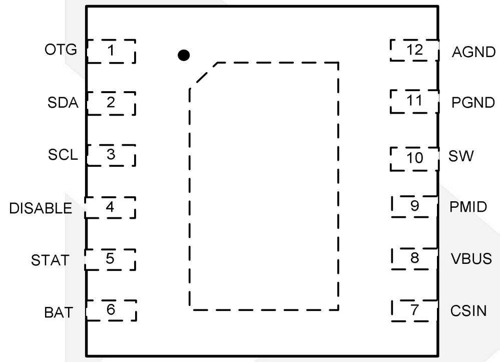
Applications

- Cell Phones, Smart Phones, PDAs
- Tablet, Portable Media Players
- Gaming Device, Digital Cameras

Ordering Information

Order Part Number	Top Marking		T_A	Package	
DIO59020CD12	59020	Green	-40 to 85°C	DFN3*3-12	Tape & Reel, 5000

Pin Assignments



DFN3*3-12

Figure 1. Pin Assignment (Top View)

Pin Definitions

Name	Description
VBUS	Charger Input Voltage and USB-OTG output voltage. Bypass with a 1μF capacitor to PGND.
NC	No Connect. No external connection is made between this pin and the IC's internal circuitry.
SCL	I^2C Interface Serial Clock. This pin should not be left floating.
PMID	Power Input Voltage. Power input to the charger regulator, bypass point for the input current sense, and high-voltage input switch. Bypass with a minimum of 10μF, 6.3V capacitor to PGND.
SDA	I^2C Interface Serial Data. This pin should not be left floating.
SW	Switching Node. Connect to output inductor.
STAT	Status. Open-drain output indicating charge status. The IC pulls this pin LOW when charging.
PGND	Power Ground. Power return for gate drive and power transistors. The connection from this pin to the bottom of CMID should be as short as possible.
OTG	On-The-Go. Enables boost regulator in conjunction with OTG_EN and OTG_PL bits (see Table 13).
CSIN	Charging current detection input terminal.
DISABLE	Charge Disable. If this pin is HIGH, charging is disabled. When LOW, charging is controlled by the I^2C registers.
BAT	Battery Voltage. Connect to the positive (+) terminal of the battery pack. Bypass with a 0.1μF capacitor to PGND if the battery is connected through long leads.
AGND	Analog ground.

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter		Rating	Unit
VBUS Voltage	Continuous	-1.4 to 26.0	V
	Pulsed, 100ms Maximum Non-Repetitive	-2.0 to 26.0	
STAT Voltage		-0.3 to 26.0	V
PMID Voltage		6.5	V
SW, CSIN, VBAT, DISABLE Voltage		-0.3 to 6.5	
Voltage on Other Pins		-0.3 to 6.5	V
Maximum V_{BUS} Slope above 5.5V when Boost or Charger are Active		4	V/μs
ESD	HBM	2000	V
	CDM	500	
Junction Temperature		-40 to 150	°C
Storage Temperature		-65 to 150	°C
Lead Soldering Temperature, 10 Seconds		260	°C

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Parameter		Rating	Unit
Supply Voltage		4 to 6	V
Maximum Battery Voltage when Boost enabled		4.5	V
Negative VBUS Slew Rate during VBUS Short Circuit, $C_{MID} \leqslant 4.7\mu F$	$T_A \leqslant 60°C$	4	V/μs
	$T_A \geqslant 60°C$	2	
Ambient Temperature		-30 to 85	°C
Junction Temperature		-30 to 120	°C

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Electrical Characteristics

V_{IN} = 5V, T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supplies						
I_{VBUS}	VBUS Current	V_{BUS}>$V_{BUS(min)}$, PWM Switching		10		mA
		V_{BUS}> $V_{BUS(min)}$; PWM Enabled, Not Switching (Battery OVP Condition); I_IN Setting=100 mA		0.2		mA
		0°C<TJ<85°C, HZ_MODE=1		96		μA
I_{LKG}	VBAT to VBUS Leakage Current	0°C<TJ<85°C, HZ_MODE=1, VBAT=4.2V, VBUS=0V		1.6	5.0	μA
I_{BAT}	Battery is charge Current in High-Impedance Mode	0°C<TJ< 85°C, HZ_MODE=1, VBAT=4.2V		12	20	μA
		DISABLE=1, 0°C<TJ<85°C, VBAT=4.2V		12	20	
Charger Voltage Regulation						
V_{OREG}	Charge Voltage Range		4.2		4.4	V
	Charge Voltage Accuracy	TA=25°C	-0.5%		0.5%	
		TJ=0 to 125°C	-1%		1%	
Charging Current Regulation						
I_{OCHRG}	Output Charge Current Range	V_{SHORT}<V_{BAT}<V_{OREG}, R_{SENSE}=68mΩ	550		1500	mA
		V_{SHORT}<V_{BAT}<V_{OREG}, R_{SENSE}=51mΩ	735		1996	
	Charge Current Accuracy Across R_{SENSE}	20mV ≤ V_{IREG}≤ 40mV	-6		6	%
		V_{IREG}>40mV	-4		4	%
Logic Levels: DISABLE, SDA, SCL, OTG						
V_{IH}	High-Level Input Voltage		1.05			V
V_{IL}	Low-Level Input Voltage				0.4	V
I_{IN}	Input Bias Current	Input Tied to GND or V_{IN}		0.01	1.00	μA
Charge Termination Detection						
$I_{(TERM)}$	Termination Current Range	V_{BAT}>V_{OREG}–V_{RCH}, R_{SENSE}=68mΩ	46		368	mA
	Termination Current Accuracy	[V_{CSIN}– V_{BAT}] from 3mV to 20mV	-10		10	%
		[V_{CSIN}– V_{BAT}] from 20mV to 40mV	-3		3	%
	Termination Current Deglitch Time			30		ms

Input Power Source Detection						
$V_{IN(MIN)}$	VBUS Input Voltage Rising	To Initiate and Pass VBUS Validation	3.75	4	4.25	V
V_{hys}				0.3		V
t_{VBUS_VALID}	VBUS Validation Time			30		ms
Special Charger (V_{BUS})						
V_{SP}	Special Charger Set point Accuracy		-3		3	%
Input Current Limit						
I_{INLIM}	Input Current Limit Threshold	REG[7:6]=00		100		mA
		REG[7:6]=01	470	500	530	
		REG[7:6]=10	750	800	850	
		REG[7:6]=11		No limit		
Battery Recharge Threshold						
V_{RCH}	Recharge Threshold	Below $V_{(OREG)}$	50		200	mV
	Deglitch Time	V_{BAT} Falling Below V_{RCH} Threshold		30		ms
STAT Output						
$V_{STAT(OL)}$	STAT Output Low	I_{STAT}=10mA			0.4	V
$I_{STAT(OH)}$	STAT High Leakage Current	V_{STAT}=5V			1	μA
Sleep Comparator						
V_{SLP}	Sleep-Mode Entry Threshold, $V_{BUS}-V_{BAT}$	$4V \le V_{BAT} \le V_{OREG}$, V_{BUS} Falling	0	0.04	0.1	V
$V_{SLP-EXIT}$	Sleep-Mode Exit Threshold, $V_{BUS}-V_{BAT}$			0.1		V
t_{SLP_EXIT}	Deglitch Time for VBUS Rising Above V_{BAT} by V_{SLP}	Rising Voltage		30		ms
Power Switches						
$R_{DS(ON)}$	Q3 On Resistance(VBUS to PMID)	$I_{IN(LIMIT)}$=500mA		86		mΩ
	Q1 On Resistance(PMID to SW)			85		
	Q2 On Resistance(SW to GND)			75		
Charger PWM Modulator						
f_{SW}	Oscillator Frequency			1.5		MHz
D_{MAX}	Maximum Duty Cycle				100	%
D_{MIN}	Minimum Duty Cycle			6		%
I_{SYNC}	Synchronous to Non-Synchronous Current Cut-Off Threshold	Low-Side MOSFET(Q2) Cycle-by-Cycle Current Limit		300		mA

Boost Mode Operation(OPA_MODE=1, HZ_MODE=0)						
V_{BOOST}	Boost Output Voltage at VBUS	2.5V < V_{BAT}<4.5V, I_{LOAD} from 0 to 200mA	4.85	5.05	5.2	V
		3.0V < V_{BAT}<4.5V, I_{LOAD} from 0 to 500mA	4.8	5.05	5.2	
$I_{BAT(BOOST)}$	Boost Mode Quiescent Current	PFM Mode, V_{BAT}=3.6V, I_{OUT}=0		500		μA
$I_{LIMPK(BST)}$	Q2 Valley Current Limit			2.5		A
$UVLO_{BST}$	Minimum Battery Voltage for Boost Operation	While Boost Active		2.6		V
		To Start Boost Regulator		2.7		
Battery Detection						
I_{DETECT}	Battery Detection Sink Current	Begins after Charge Termination Detected		10		mA
t_{DETECT}	Battery Detection Time			30		ms
Protection and Timers						
$VBUS_{OVP}$	VBUS Over-Voltage Shutdown	V_{BUS} Rising	5.82	6	6.2	V
	Hysteresis	V_{BUS} Falling		200		mV
$I_{LIMPK(CHG)}$	Q1 Cycle-by-Cycle Peak Current Limit	Charge Mode		3.4		A
V_{SHORT}	Battery Short-Circuit Threshold	V_{BAT} Rising	1.95	2	2.05	V
	Hysteresis	V_{BAT} Falling		100		mV
I_{SHORT}	Linear Charging Current	V_{BAT}<V_{SHORT}	20	30	40	mA
$T_{SHUTDWN}$	Thermal Shutdown Threshold	T_J Rising		145		℃
	Hysteresis	T_J Falling		10		
T_{CF}	Thermal Regulation Threshold	Charge Current Reduction Begins		120		℃
t_{INT}	Detection Interval			30		ms

I²C Timing Specifications

Guaranteed by design.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	
		High-Speed Mode, $C_B \leq 100pF$			3400	
		High-Speed Mode, $C_B \leq 400pF$			1700	
t_{BUF}	Bus-Free Time between STOP and START Conditions	Standard Mode		4.7		μs
		Fast Mode		1.3		
$t_{HD;STA}$	START or Repeated START Hold Time	Standard Mode		4		μs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
t_{LOW}	SCL LOW Period	Standard Mode		4.7		μs
		Fast Mode		1.3		μs
		High-Speed Mode, $C_B \leq 100pF$		160		ns
		High-Speed Mode, $C_B \leq 400pF$		320		ns
t_{HIGH}	SCL HIGH Period	Standard Mode		4		μs
		Fast Mode		600		ns
		High-Speed Mode, $C_B \leq 100pF$		60		ns
		High-Speed Mode, $C_B \leq 400pF$		120		ns
$t_{SU;STA}$	Repeated START Setup Time	Standard Mode		4.7		μs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
$t_{SU;DAT}$	Data Setup Time	Standard Mode		250		ns
		Fast Mode		100		
		High-Speed Mode		20		
$t_{HD;DAT}$	Data Hold Time	Standard Mode	0		3.45	μs
		Fast Mode	0		900	ns
		High-Speed Mode, $C_B \leq 100pF$	0		70	ns
		High-Speed Mode, $C_B \leq 400pF$	0		150	ns
t_{RCL}	SCL Rise Time	Standard Mode	$20+0.1C_B$		100	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, $C_B \leq 100pF$		10	80	
		High-Speed Mode, $C_B \leq 400pF$		20	160	
t_{FCL}	SCL Fall Time	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, $C_B \leq 100pF$		10	40	

		High-Speed Mode, $C_B \leqslant 400pF$		20	80	
t_{RDA} t_{RCL1}	SDA Rise Time Rise Time of SCL after a Repeated START Condition and after ACK Bit	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, $C_B \leqslant 100pF$		10	80	
		High-Speed Mode, $C_B \leqslant 400pF$		20	160	
t_{FDA}	SDA Fall Time	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, $C_B \leqslant 100pF$		10	80	
		High-Speed Mode, $C_B \leqslant 400pF$		20	160	
$t_{SU;STO}$	Stop Condition Setup Time	Standard Mode		4		μs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
C_B	Capacitive Load for SDA, SCL				400	pF

Timing Diagrams

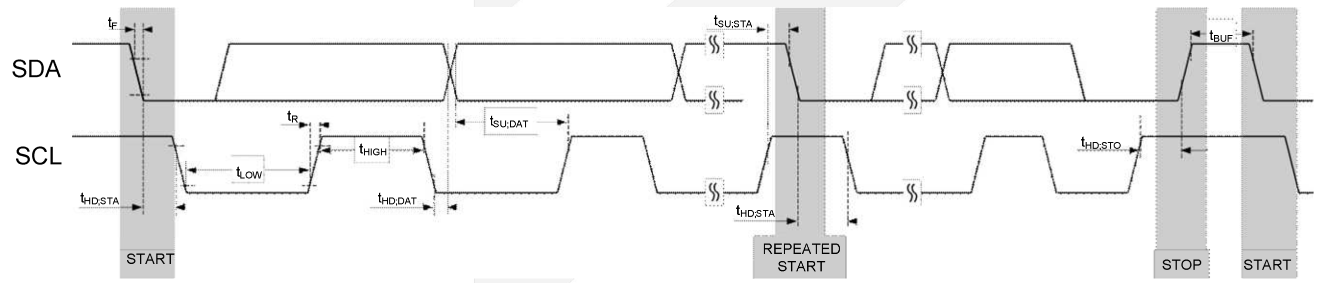
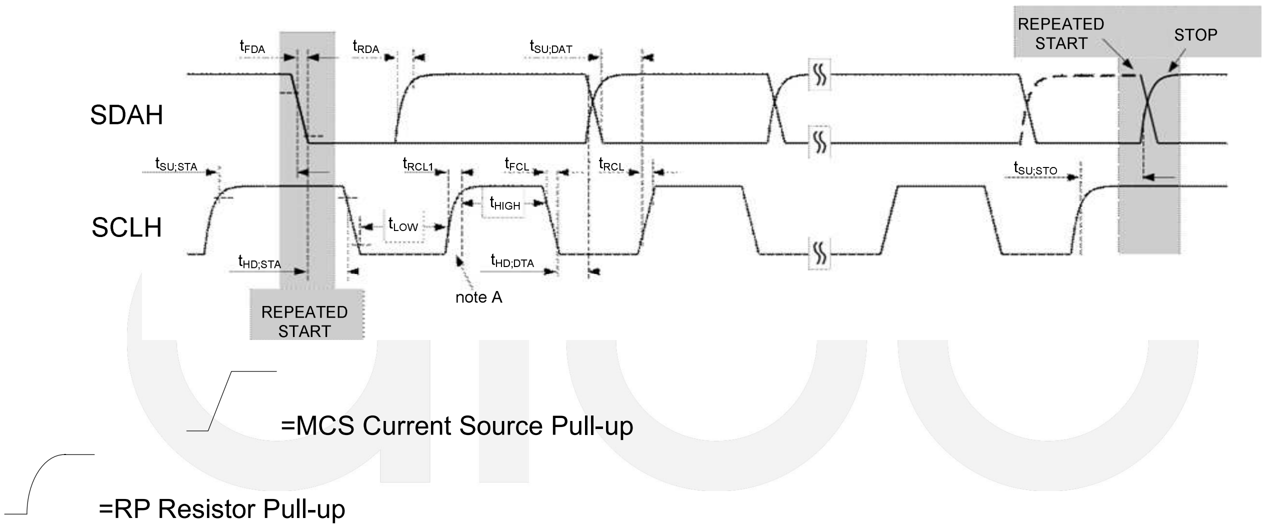


Figure 2. I²C Interface Timing for Fast and Slow Modes



Note A: First rising edge of SCH after Repeated Start and after each ACK bit.

Figure 3. I²C Interface Timing for High-Speed Mode

Typical Application

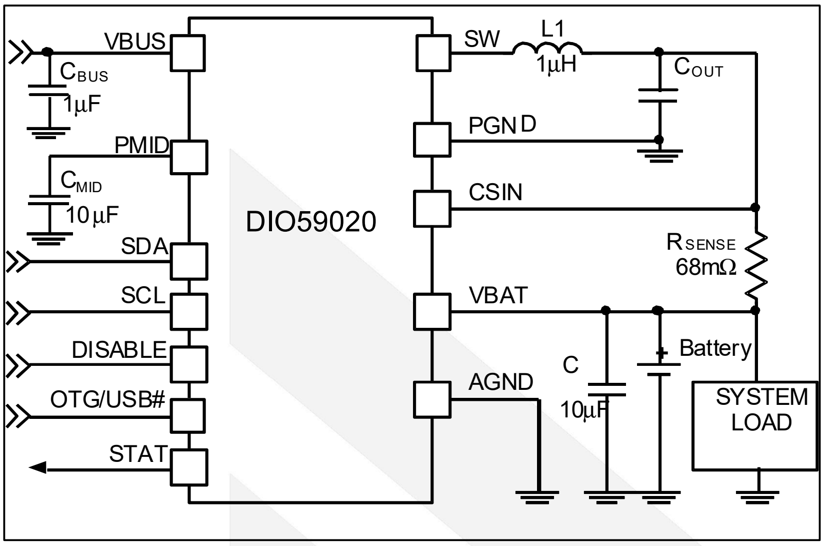
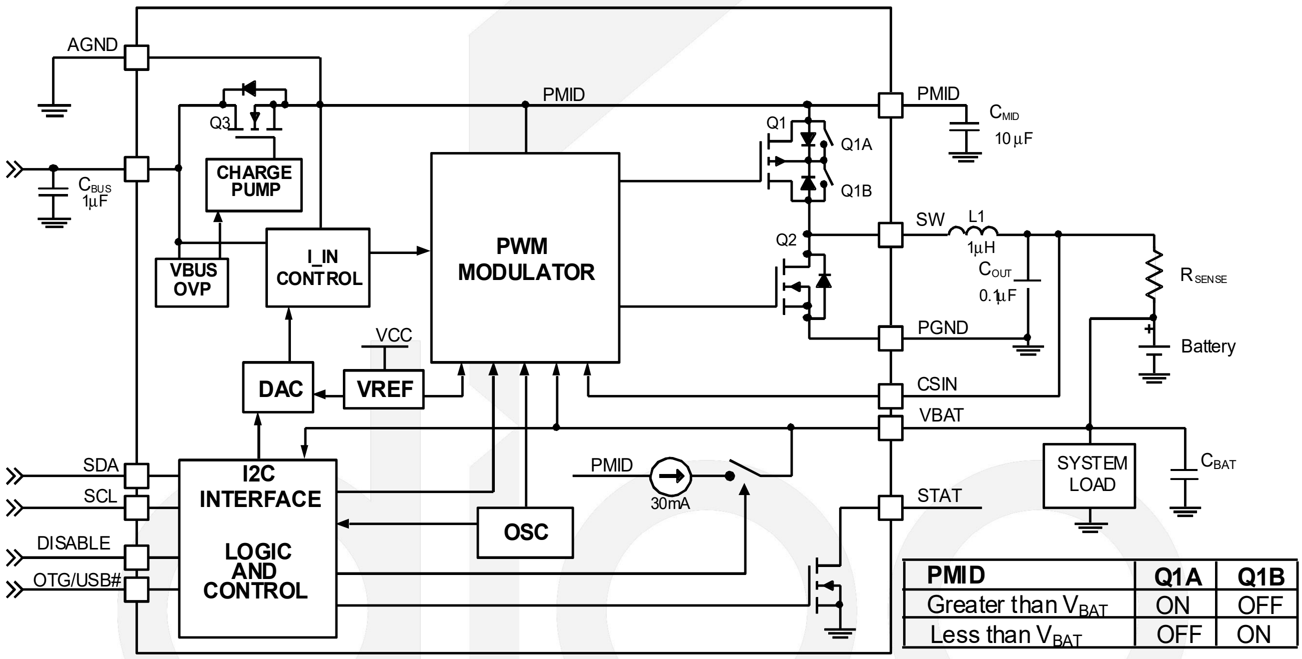


Figure 4. Typical Application

Block Diagram



PMID	Q1A	Q1B
Greater than V_{BAT}	ON	OFF
Less than V_{BAT}	OFF	ON

Figure 5. IC and System Block Diagram

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Application Information

Circuit Description/Overview

When charging batteries with a current-limited input source, such as USB, a switching charger's high efficiency over a wide range of output voltages minimizes charging time.

DIO59020 combines a highly integrated synchronous buck regulator for charging with a synchronous boost regulator, which can supply 5V to USB On-The-Go (OTG) peripherals. The regulator employs synchronous rectification for both the charger and boost regulators to maintain high efficiency over a wide range of battery voltages and charge states.

The DIO59020 has three operating modes:

1. Charge Mode:
   Charge a signal-cell Li-ion or Li-polymer battery.
2. Boost Mode:
   Provide 5V power to USB-OTG with an integrated synchronous rectification boost regulator using the battery as input.
3. High-Impedance Mode:
   Both the boost and charging circuits are OFF in this mode. Current flow from VBUS to the battery or from the battery to VBU is blocked in this mode. This mode consumes very little current from VBUS or the battery.

Note: Default setting is denoted bold typeface.

Charge Mode

In charge Mode, DIO59020 employs four regulation loops:

1. Input Current: Limits the amount of current drawn from VBUS. This current is sensed internally and can be programmed through the I²C interface.
2. Charging Current: Limits the maximum charging current. This current is sensed using an external R_{SENSE} resistor.
3. Charge Voltage: The regulator is restricted from exceeding this voltage. As the internal battery voltage roses, the battery's internal impedance and R_{SENSE} work in conjunction with the charge voltage regulation to decrease the amount of current flowing to the battery. Battery charging is completed when the voltage across R_{SENSE} drops below the I_{TERM} threshold.
4. Temperature: If the IC's junction temperature reaches 120℃,charge current is reduced until the IC's temperature stabilizes at 120℃.
5. An additional loop limits the amount of drop on VBUS to a programmable voltage (V_{SP}) to accommodate "special chargers" that limit current to a lower current than might be available from a "normal" USB wall charger.

Battery Charging Curve

If the battery voltage is below V_{SHORT}, a linear current source pre-charges the battery until V_{BAT} reaches V_{SHORT}. The PWM charging circuit is then started and the battery is charged with a constant current if sufficient input power is available. The current slew rate is limited to prevent overshoot.

The DIO59020 is designed to work with a current-limited input source at VBUS. During the current regulation phase of charging, I_{INLIM} or the programmed charging current limits the current available to charge the battery and power the system. The effect of I_{INLIM} on I_{CHARGE} can be seen in Figure 7.

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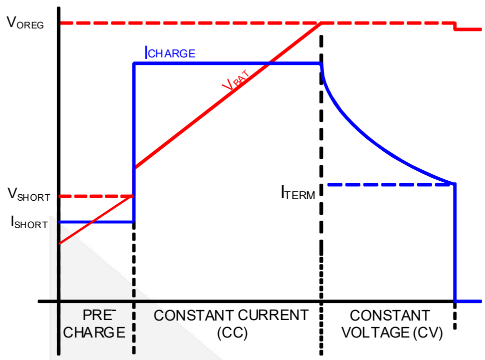

Figure 6. Charge Curve, I_{CHARGE} Not Limited by I_{INLIM}

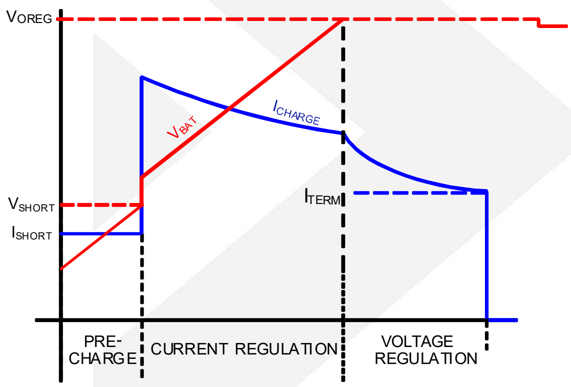

Figure 7. Charge Curve, I_{INLIM} Limits I_{CHARGE}

Assuming that V_{OREG} is programmed to the cell's fully charged "float" voltage, the current that the battery accepts with the PWM regulator limiting its output (sensed at VBAT) to V_{OREG} declines, and the charger enters the voltage regulation phase of charging. When the current declines to the programmed I_{TERM} value, the charge cycle is complete. Charge current termination can be disabled by resetting the TE bit (REG[3]).

The charger output or "float" voltage can be programmed by the OREG bits from 4.2V to 4.4V, as shown in Table 1.

Table 1. OREG Bits (OREG[7:2]) vs. Charge V_{OUT} (V_{OREG}) Float Voltage

Decimal	Hex	V_{OREG}
0~35	00~23	4.20
36~40	24~28	4.30
41~43	29~2B	4.35
44~62	2C~3E	4.40

The following charging parameters can be programmed by the host through I²C.

Table 2. Programmable Charging Parameters

Parameter	Name	Register
Output Voltage Regulation	V_{OREG}	REG2[7:2]
Battery Charging Current Limit	I_{OCHRG}	REG4[6:4]
Input Current Limit	I_{INLIM}	REG1[7:6]
Charge Termination Limit	I_{TERM}	REG4[2:0]

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A new charge cycle begins when one of the following occurs:

- The battery voltage falls below V_{OREG}-V_{RCH}
- VBUS Power on Reset (POR) clears and the battery voltage is below the V_{SHORT}.
- $\overline{CE}$ or HZ_MODE is rest through I²C write to CONTROL1 (Reg1) register.

Charge Current Limit ($I_{OCHARGE}$)

Table 3. $I_{OCHARGE}$ (REG4 [6:4]) Current as Function of $I_{OCHARGE}$ Bits and R_{SENSE} Resistor Values

DEC	BIN	HEX	V_{RSENSE} (mV)	$I_{OCHARGE}$ (mA)	
				51mΩ	68mΩ
0	000	00	37.5	735	551
1	001	01	44.4	870	653
2	010	02	51.2	1004	753
3	011	03	57.5	1127	846
4	100	04	71.3	1398	1048
5	101	05	78.1	1531	1149
6	110	06	91.9	1802	1351
7	111	07	101.8	1996	1498

Table 4. V_{RCH} (REG7 [1:0]) Recharge Voltage

DEC	BIN	HEX	V_{RCH} (mV)
0	00	00	50
1	01	01	100
2	10	02	150
3	11	03	200

Termination Current Limit

Current charge termination is enabled when TE (REG1[3]) =1. Typical termination current values are given in Table 5.

Table 5. I_{TERM} Current as Function of I_{TERM} Bits (REG4[2:0]) and R_{SENSE} Resistor Values

I_{TERM}	V_{RSENSE} (mV)	I_{TERM} (mA)	
		51mΩ	68mΩ
0	3.1	61	46
1	6.3	124	92
2	9.4	184	138
3	12.5	245	184
4	15.6	306	230
5	18.8	369	276
6	21.9	429	322
7	25	490	368

When the charge current falls below I_{TERM}, PWM charging stops and the STAT bits change to READY (00) for about 30ms while the IC determines whether the battery and charging source are still connected. STAT then changes to CHARGE DONE (10), provided the battery and charger are still connected.

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PWM Controller in Charge Mode

The IC uses a current-mode PWM controller to regulator the output voltage and battery charge currents. The synchronous rectifier (Q2) has a current limit that which off the FET when the current is negative by more than 300mA peak. This prevents current flow from battery.

V_{BUS} POR/Non-Compliant Charger Rejection

When the IC detects that VBUS has risen above $V_{IN(MIN)}$ (4.3V), the IC applies a 250Ω load from VBUS to GND. To clear the VBUS POR (Power-On-Reset) and begin charging, VBUS must remain above $V_{IN(MIN)}$ and below $VBUS_{OVP}$ for t_{VBUS_VALID} (30ms) before the IC initiates Charging. The VBUS validation sequence always occurs charging is initiated or re-initiated (for example, after a VBUS OVP fault or a V_{RCH} recharge initiation).

t_{VBUS_VALID} ensures that unfiltered 50/60Hz chargers and other non-compliant chargers are rejected.

Input Current Limiting

To minimize charging time without overloading VBUS current limitations, the IC's input current limit can be programmed by the I_{INLIM} bits (REG1[7:6]).

Table 6. Input Current Limit

I_{INLIM} REG[7:6]	Input Current Limit
00	100 mA
01	500 mA
10	800 mA
11	No limit

Flow Charts

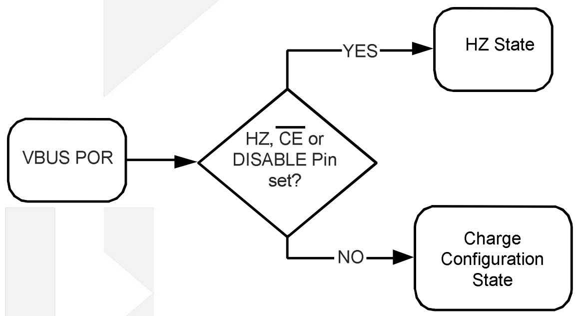

Figure 8. Charger VBUS POR

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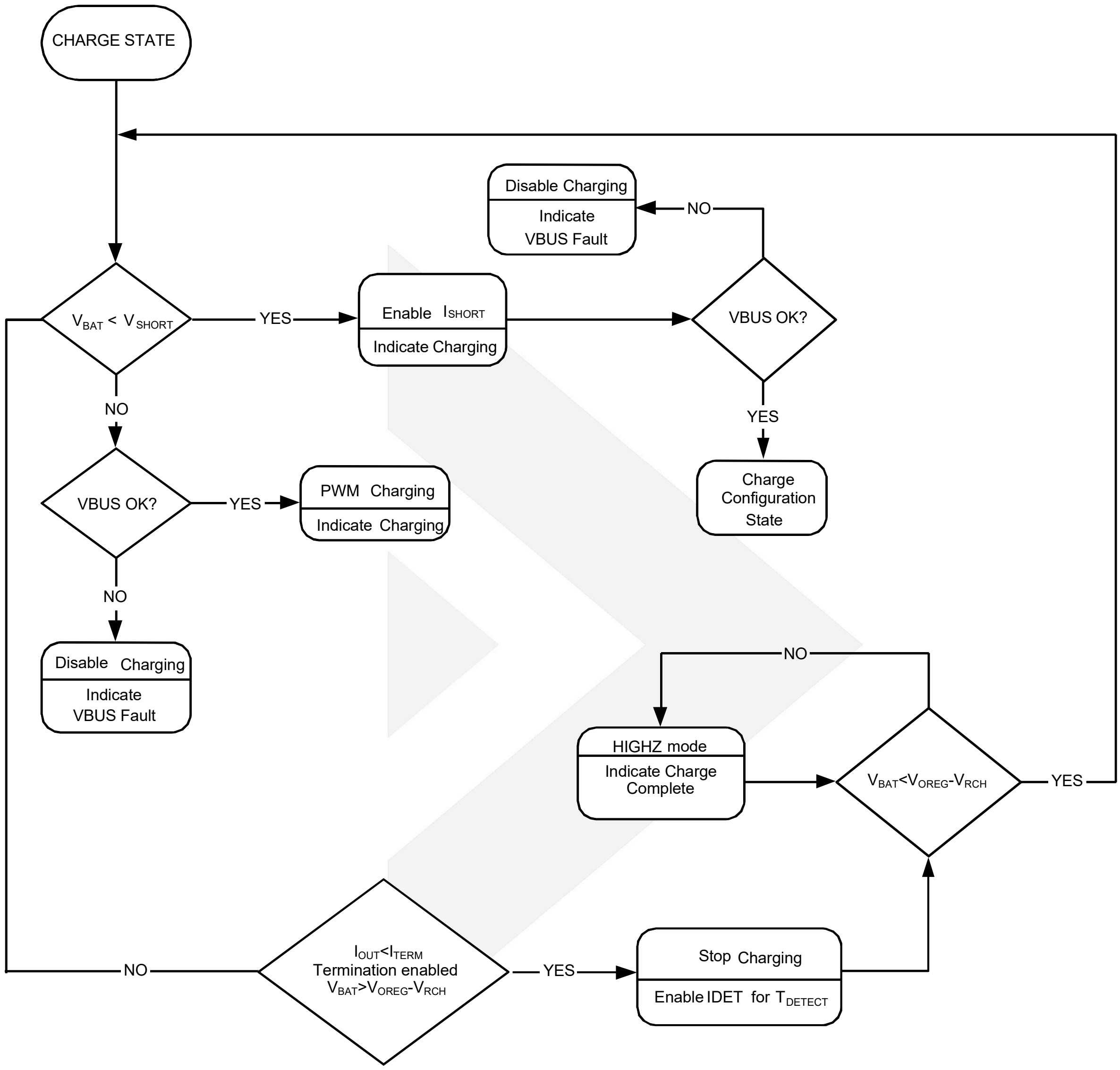

Figure 9. Charge Mode

Special Charger

The DIO59020 has additional functionality to limit input current in case a current-limited "special charger" is supplying VBUS. These slowly increase the charging current until either.

- I_{INLIM} or $I_{OCHARGE}$ is reached

or

- V_{BUS}=V_{SP}.

If V_{BUS} collapses to V_{SP} when the current is ramping up, the DIO59020 charge with an input current that keeps V_{BUS}=V_{SP}. When the V_{SP} control loop is limiting the charge current, the SP bit (REG5[4]) is set.

Table 7. V_{SP} as Function of SP Bits (REG5[2:0])

SP (REG5[2:0])			
DEC	BIN	HEX	V_{SP}
0	000	00	4.225
1	001	01	4.300
2	010	02	4.375
3	011	03	4.450
4	100	04	4.525
5	101	05	4.600
6	110	06	4.675
7	111	07	4.750

Thermal Regulation and Protection

When the IC's junction temperature reaches T_{CF} (about 120℃), the charger reduces its output current to prevent overheating. If the temperature increases beyond $T_{SHUTDOWN}$; charging is suspended, the FAULT bits are set to 101, and STAT is pulsed HIGH. In Suspend Mode, all timers stop and the state of the IC's logic is preserved. Charging resumes at programmed current after the die cools to about 120℃.

Charge Mode Input Supply Protection

Sleep Mode

When V_{BUS} falls below V_{BAT}+V_{SLP} and V_{BUS} is above $V_{IN(MIN)}$, the IC enters Sleep Mode to prevent the battery from draining into VBUS. During Sleep Mode, reverse current is disabled by body switching Q1.

Input Supply Low-Voltage Detection

The IC continuously monitors VBUS during charging. If V_{BUS} falls below $V_{IN(MIN)}$, the IC:

1. Terminates charging.
2. Pulses the STAT pin, sets the STAT bits to 11, and sets the FAULT bits to 011.

If V_{BUS} recovers above the $V_{IN(MIN)}$ rising threshold after time t_{INT} (about two seconds), the charging process is repeated. This function prevents the USB power bus from collapsing or oscillating when the IC is connected to a suspended USB port or a low-current-capable OTG device.

Input Over-Voltage Detection

When the V_{BUS} exceeds $VBUS_{OVP}$, the IC:

1. Turns off Q3
2. Suspends charging
3. Sets the FAULT bits to 001, sets the STAT bits to 11, and pulses the STAT pin.

When V_{BUS} falls about 200mV below $VBUS_{OVP}$, the fault is cleared and charging resumes after V_{BUS} is revalidated (see VBUS POR/Non-Compliant Charger Rejection).

VBUS Short While Charging

If VBUS is shorted with a very low impedance while the IC is charging with $I_{INLIMIT}$=100mA, the IC may not meet datasheet specifications until power is removed. To trigger this condition, V_{BUS} must be driven from 5V to GND with a high slew rate. Achieving this slew rate requires a 0Ω short to the USB cable less than 10cm from the connector.

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Charge Mode Battery Detection & Protection

VBAT Over-Voltage Protection

The OREG voltage regulation loop prevents V_{BAT} from overshooting the OREG voltage when the battery is removed. If the VBAT Pin voltage is higher than 4.8V, the IC sets the FAULT bits to 100, sets the STAT bits to 11, and pulses the STAT pin.

Battery Detection During Charging

The IC can detect the presence, absence. During normal charging, once VBAT is close to VOREG and the termination charging, once VBAT is close to VOREG and the termination charge current is detected, the IC terminates charging and sets the STAT bits to 10. It then turns on a discharge current, I_{DETECT}, for t_{DETECT}. If VBAT is still above 2V, the battery is present and the IC sets the FAULT bits to 000. If VBAT is below 2V, the battery is absent and the IC:

1. Operation with No Battery
2. Sets the FAULT bits to 111.

Battery Short-Circuit Protection

If the battery voltage is below the short-circuit threshold (V_{SHORT}); a linear current source, I_{SHORT}, supplies V_{BAT} until V_{BAT}>V_{SHORT}.

System Operation with No Battery

The DIO59020 continues charging after VBUS POR with the default parameters and 500mA input current limit, regulating the V_{BAT} line to 3.78V (if set V_{OREG} at 4.2V). In this way, the DIO59020 can start the system without a battery. Re-connect power to VBUS or reset DISABLE pin, IC can exit No Battery Mode.

Charger Status/Fault Status

The STAT pin indicates the operating condition of the IC and provides a fault indicator for interrupt driven systems.

Table 8. STAT Pin Function

EN_STAT	Charge State	STAT Pin
X	No Charging	OPEN
1	Charging	LOW
x	Fault	2Hz Pulse

The FAULT bits (Reg0[2:0]) indicate the type of fault in Charge Mode (see Table 9).

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Table 9. Fault Status Bits During Charge Mode

Fault Bit			Fault Description
B2	B1	B0	
0	0	0	Normal (No Fault)
0	0	1	VBUS OVP
0	1	0	Sleep Mode
0	1	1	Poor Input Source
1	0	0	Battery OVP
1	0	1	Thermal Shutdown
1	1	0	N.A
1	1	1	No Battery

Charge Mode Control Bits

Setting either HZ_MODE or $\overline{\text{CE}}$ through I^2C disables the charger and puts the IC into High-Impedance Mode.

Table 10. DISABLE Pin and $\overline{\text{CE}}$ Bit Functionality

Charging	DISABLE Pin	$\overline{\text{CE}}$	HZ_MODE
ENABLE	0	0	0
DISABLE	X	1	X
DISABLE	X	X	1
DISABLE	1	X	X

Operational Mode Control

OPA_MODE (REG1[0]) and the HZ_MODE (REG1[1]) bits in conjunction with the FAULT state define the operational mode of the charger.

Table 11. Operation Mode Control

HZ_MODE	OPA_MODE	FAULT	Operation Mode
0	0	0	Charge
0	X	1	No charging
0	1	0	Boost
1	X	X	High Impedance

Boost Mode

Boost Mode can be enabled if OTG pin and OPA_MODE bits as indicated in Table 12 The OTG pin ACTIVE state is 1 if OTG_PL=1 and 0 when OTG_PL=0.

If boost is active using the OTG pin, Boost Mode is initiated even if the HZ_MODE=1. The HZ_MODE bit overrides the OPA_MODE bit.

Table 12. Enabling Boost

OTG_EN	OTG Pin	HZ_MODE	OPA_MODE	BOOST
1	ACTIVE	X	X	Enabled
X	X	0	1	Enabled
X	$\overline{\text{ACTIVE}}$	X	0	Disabled
0	X	1	X	Disabled
1	$\overline{\text{ACTIVE}}$	1	1	Disabled
0	ACTIVE	0	0	Disabled

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Boost COT Control

The IC uses a constant on-time and valley current detect to regulate VBUS. The regulator achieves excellent transient response by employing current-mode modulation. This technique causes the regulator to exhibit a load line. During COT Mode, the output voltage drops slightly as the input current rises.

PFM Mode

If VBUS>$VREF_{BOOST}$ (nominally 5.05V) when the valley current comes to 0, the regulator enters PFM Mode. Boost pulses are inhibited until V_{BUS}<$VREF_{BOOST}$. Once V_{BUS}<$VREF_{BOOST}$, boost pulses are allowed for one or several times until V_{BUS}>$VREF_{BOOST}$. Therefore the regulator behaves like a burst mode regulator, with the average of its output voltage ripple at 5.05V in PFM Mode.

Table 13. Boost PWM Operating States

Mode	Description	Invoked When
LIN	Linear Startup	V_{BAT}>V_{BUS}
SS	Boost Soft-Start	V_{BUS}<V_{BST}
BST	Boost Operation Mode	V_{BAT}>$UVLO_{BST}$ and SS Completed

Startup

When the boost regulator is shut down, current flow is prevented from V_{BAT} to V_{BUS}, as well as reverse flow from V_{BUS} to V_{BAT}.

LIN State

When EN rises, if V_{BAT}>$UVLO_{BST}$, the regulator attempts to bring PMID within 200mV of VBAT using an internal 800mA current source from VBAT (LIN State). If PMID has not achieved V_{BAT}- 200mV after 500μs, a FAULT state is initiated.

SS State

When PMID>V_{BAT}-200mV, the boost regulator begins switching with a SS modulator. The output slews up slowly and smoothly until V_{BUS}=$VREF_{BOOST}$.

If the output fails to achieve set point (VBST) within SS time, normally 128μs, a fault state is initiated.

BST State

This is the normal operating mode of the regulator. The regulator uses a constant on-time and valley current detect modulation scheme. The minimum t_{ON} is proportional to $\frac{V_{OUT} - V_{IN}}{V_{OUT}}$, which keeps the regulator's switching frequency reasonably constant in CCM.

To ensure the VBUS does not pump significantly above the regulation point, the boost switch remains off as long as FB>V_{REF}.

Boost Faults

If a Boost FAULT OCCURS:

1. OPA_MODE bit is reset.
2. The power stage is in High-Impedance Mode.

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3. The FAULT bits (REG0[2:0]) are set per Table 14.

Restart After Boost Faults

If boost was enabled with the OPA_MODE bit and OTG_EN=0, Boost Mode can only be enabled through subsequent I²C commands since OPA_MODE is reset on boost faults. If OTG_EN=1 and the OTG pin is still ACTIVE (see Table 12), the boost restarts after a 10ms delay, as shown in Figure 10. If the fault condition persists, restart is attempted every 10ms until the fault clears or an I²C command disables the boost.

Table 14. Fault Bits During Boost Mode

Fault Bit			Fault Description
B2	B1	B0	
0	0	0	Normal (no fault)
0	0	1	V_{BUS}>$VBUS_{OVP}$
0	1	0	VBUS fails to achieve the voltage required to advance to the next state during soft-start or sustained (>50μs) current limit during the BST state.
0	1	1	N/A: This code does not appear.
1	0	0	N/A: This code does not appear.
1	0	1	Thermal shutdown
1	1	0	N/A: This code does not appear.
1	1	1	N/A: This code does not appear.

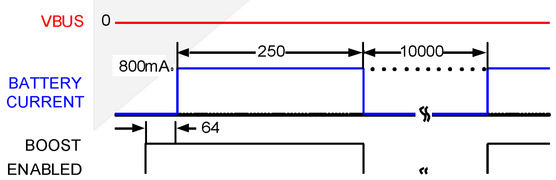

Figure 10. Boost Response Attempting to Start into VBUS Short Circuit (Times in μs)

Monitor Register (Reg10H)

Additional status monitoring bits enable the host processor to have more visibility into the status of the IC. The monitor bits are real-time status indicators.

I²C Interface

The DIO59020's serial interface is compatible with Standard, Fast, Fast Plus, and High-Speed Mode I²C-Bus specifications. The SCL line is an input and the SDA line is a bi-directional open-drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and signaling ACK. All data is shifted in MSB (bit 7) first.

Slave Address

Table 15. I²C Slave Address Byte

Part Type	7	6	5	4	3	2	1	0
DIO59020	1	1	0	1	0	1	0	R/$\overline{W}$

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In hex notation, the slave address assumes a 0LSB.The hex slave address for the DIO59020 is D4H and is D6H for all other parts in the family.

Bus Timing

As shown in Figure 11, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

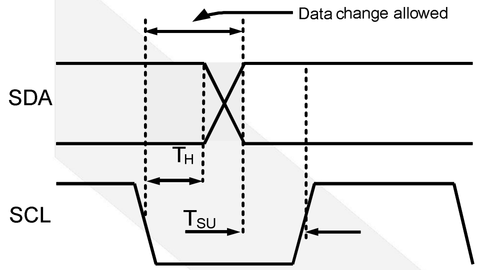

Figure 11. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH.A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 12.

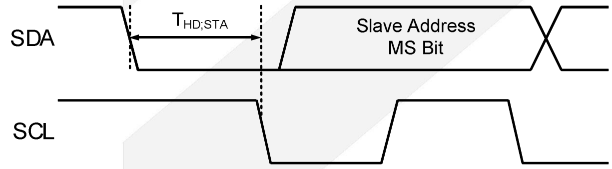

Figure 12. Start Bit

A transaction ends with a STOP condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 13.

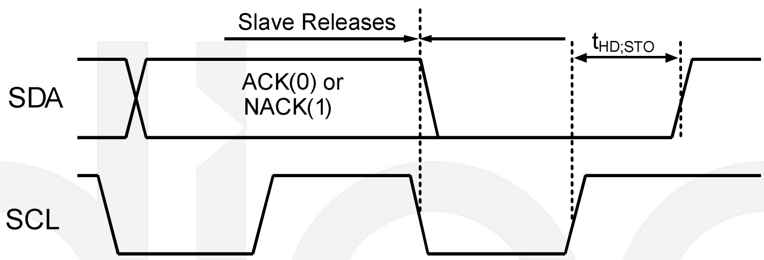

Figure 13. Stop Bit

During a read from theDIO59020(Figure 15,Figure 16), the master issues a Repeated Start after sending the register address and before resending the slave address. The Repeated Start is a 1-to-0transition on SDA while SCL is HIGH, as shown in Figure 14.

High-Speed (HS) Mode

The protocols for High-Speed(HS), Low-Speed(LS), and Fast-Speed(FS) Modes are identical except the bus speed for HS Mode is 3.4MHz. HS Mode is entered when the bus master sends the HS master code 00001XXX after a start condition. The master code is sent in Fast or Fast Plus Mode (less than1MHz clock); slaves do not

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ACK this transmission.

The master then generates a repeated start condition (Figure 14) that causes all slaves on the bus to switch to HS Mode. The master then sends I²C packets, as described above, using the HS Mode clock rate and timing.
The bus remains in HS Mode until a stop bit (Figure13) is sent by the master. While in HS Mode, packets are separated by repeated start conditions (Figure 14).

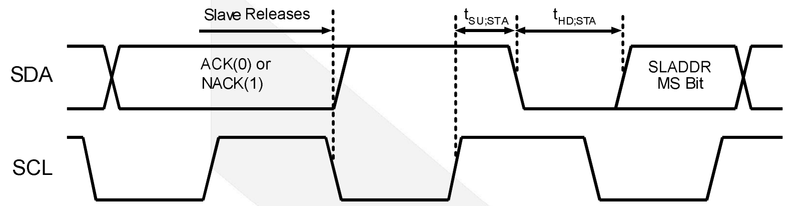

Figure 14. Repeated Start Timing

Read and Write Transactions

The figure below outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as Master Drives Bus and Slave Drive Bus . All addresses and data are MSB first.

Table 15. Bit Definitions for Figure 15, Figure 16

Symbol	Definition
S	START, see Figure 12
A	ACK. The slave drives SDA to 0 to acknowledge the preceding packet.
$\overline{A}$	NACK. The slave sends a 1 to NACK the preceding packet.
R	Repeated START, see Figure 14
P	STOP, see Figure 13.

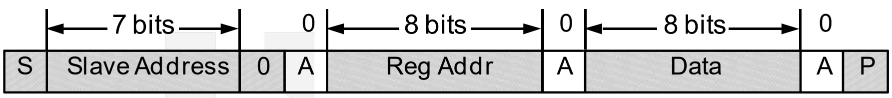

Figure 15. Write Transaction

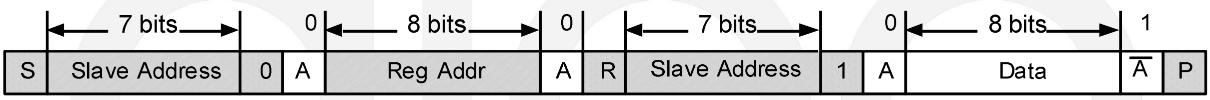

Figure 16. Read Transaction

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Register Bit Definitions

1 CONTROL0 Register (0x00) Default Value=X1XX0XXX

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NAME	Reserved	EN_STAT	STAT		BOOST	FAULT		
R/W	R/W	R/W	R		R	R		
Function	Unused	0 : Prevents STAT pin from going LOW during charging; STAT pin still pulses to enunciate faults 1: Enables STAT pin LOW when IC is charging.	00 :Ready 01 : Charge in progress 10 : Charge done 11 : Fault		0 : IC is not in Boost Mode 1 :IC is in Boost Mode	for Charge Mode: 000 = Normal (No Fault) 001 = VBUS OVP 010 = Sleep Mode 011 = Poor Input Source 100 = Battery OVP 101 = Thermal Shutdown 110 = N.A 111 = No Battery for Boost Mode: 000 = Normal (no fault) 001 = VBUS>$VBUS_{OVP}$ 010 = VBUS fails to achieve the voltage required to advance to the next state during soft-start or sustained (>50µs) current limit during the BST state. 011 = N/A: This code does not appear. 100 = N/A: This code does not appear. 101 = Thermal shutdown 110 = N/A: This code does not appear. 111 = N/A: This code does not appear.		

2 CONTROL1 Register (0x01) Default Value=0111 0000 (70h)

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NAME	I_{INLIM}		Reserved		TE	$\overline{CE}$	HZ_MODE	OPA_MODE
R/W	R/W		R/W		R/W	R/W	R/W	R/W
Function	Input current limit: 00:100 mA 01 :500 mA 10 :800 mA 11: No limit		Unused		0: Disable charge current termination. 1: Enable charge current termination.	0: Charger enabled. 1: Charger disabled.	0: Not High-Impedance Mode. 1: High-Impedance Mode.	0: Charge Mode. 1: Boost Mode.

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3 OREG Register (0x02) Default Value=0000 1010 (0Ah)

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NAME	OREG						OTG_PL	OTG_EN
R/W	R/W						R/W	R/W
Function	Charger output "float" voltage; programmable from 4.2 to 4.4V; defaults to 000010 (4.2V), 00 0000~10 0011 : 4.2V; 10 0100~10 1000 : 4.3V; 10 1001~10 1011: 4.35V; 10 1100~11 1110: 4.4V;						0: OTG pin active LOW. 1: OTG pin active HIGH.	0 : Disables OTG pin. 1: Enables OTG pin.

4 IC_INFO Register (0x03) Default Value=1001 0100 (94h)

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NAME	Reserved			PN			REV	
R/W	R			R			R	
Function	Identifies the IC supplier.			Part number bits.			IC Revision, revision 1.X, where X is the decimal of these three bits.	

5 IBAT Register (0x04) Default Value=1000 1001 (89h)

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NAME	Reserved	$V(I_{OCHARGE})$			Reserved	$V(I_{TERM})$		
R/W	R/W	R/W			R/W	R/W		
Function	0 = Unused	Programs the maximum charge current 000: 37.5mV; 001: 44.4mV; 010: 51.2 mV; 011: 57.5 mV; 100: 71.3 mV; 101: 78.1 mV; 110: 91.9 mV; 111: 101.8 mV; The charge current step ($I_{OCHARGE}$) is calculated using: $I_{OCHARGE} = V(I_{OCHARGE})/R_{SENSE}$;			Unused	Sets the current used for charging termination 000 : 3.1mV; 001: 6.3mV; 010: 9.4mV; 011: 12.5mV; 100: 15.6mV; 101: 18.8mV; 110: 21.9mV; 111: 25mV; The termination current step (I_{TERM}) can be calculated using: $I_{TERM} = V(I_{TERM})/R_{SENSE}$;		

6 SP_CHARGER Register (0x05) Default Value=011X X100

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NAME	Reserve	Reserve	Reserve	SP	EN_LEVEL	VSP		
R/W	R/W	R/W	R/W	R	R	R/W		
Function	Unused	Unused	Unused	0: Special charger is not active (V_{BUS} is able to stay above V_{SP}). 1: Special charger has been detected and V_{BUS} is being regulated to V_{SP}.	0: DISABLE pin is LOW. 1: DISABLE pin is HIGH.	Special charger input regulation voltage 000: 4.225V; 001: 4.300V; 010: 4.375V; 011: 4.450V; 100: 4.525V; 101: 4.600V; 110: 4.675V; 111: 4.750V		

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7 Register (0x07) **Default Value=0000 0001 (01h)**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NAME	Reserved			Reserved	Reserved		V_{RCH}	
R/W	R/W			R/W	R/W		R/W	
Function	Unused			Unused	Unused		Recharge voltage of V_{OREG} drops. 00: 50mV; 01: 100mV; 10: 150mV; 11: 200mV	

8 MONITOR Register (0x10h)

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NAME	I_{TERM_CMP}	V_{BAT_CMP}	LINCHG	T_100	I_{CHG}	I_{BUS}	V_{BUS_VALID}	CV
R/W	R	R	R	R	R	R	R	R
Function	I_{TERM_CMP}: ITERM comparator output. 0: V_{CSIN}-V_{BAT}<V_{ITERM}. 1 : V_{CSIN}-V_{BAT}>V_{ITERM} V_{BAT_CMP} Output of VBAT comparator in charging mode，0: V_{BAT}<V_{SHORT} 1 : V_{BAT}>V_{SHORT} **LINCHG** In charging mode, 0: 30mA linear charger Not Enable; 1: 30mA linear charger Enable. **T_100** Thermal comparator 0: T_J<100℃; 1: T_J>100℃ I_{CHG} In charging mode, 0: Charging Current Controlled by I_{CHARGE} Control Loop .1: Charging Current Not Controlled by I_{CHARGE} Control Loop. I_{BUS} In charging mode, 0: I_{BUS} Limiting Charging Current. 1: Charge Current Not Limited by I_{BUS} V_{BUS_VALID} When V_{BUS}>V_{BAT} ,0:V_{BUS} Not Valid 1: V_{BUS} is Valid **CV** In charging mode. 0: Constant Current Charging. 1: Constant Voltage Charging.								

PCB Layout Recommendations

Bypass capacitors should be placed as close to the IC as possible. In particular, the total loop length for CMID should be minimized to reduce overshoot and ringing on the SW, PMID, and VBUS pins. All power and ground pins must be routed to their bypass capacitors, using top copper whenever possible. Copper area connecting to the IC should be maximized to improve thermal performance if possible.

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CONTACT US

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