DIO3480AH
DP/DM Dual SPDT Switch + Comparator with Adjustable Over Voltage Protection

Features

- *DP/DM Dual SPDT Switch:*
  - Supply Range 2.3V to 5.5V
  - 6V to 21V Overvoltage Protection (OVP) on Common Pins
  - Low R_{ON} of 9Ω Maximum
  - BW of 1.2GHz Typical
  - C_{ON} of 4pF Typical
- *Over Voltage Protection Load Switch:*
  - Low Power Disable Mode
  - 1.8V Compatible Logic Inputs
  - ESD (HBM) pass 2000V
  - Surge Protection: IEC 61000-4-5: >100V
  - Over-Temperature Protection (OTP)
  - ESD Protection:
    - IEC 61000-4-2 Air Discharge: > 15kV
    - IEC 61000-4-2 Contact Discharge: > 8kV
  - +/- 100V EOS Protection
- *Comparator:*
  - Ultra Low Power Consumption: 0.3μA (TYP)
  - Wide Supply Voltage Range: 2.3V to 5.5V
- Package:
  - 24-Ball WLCSP, 4*6 Array, 0.4mm Pitch

Applications

- Mobile Handsets and Tablets

Descriptions

The DIO3480AH is a switch unit including a DP/DM dual SPDT switch, a comparator, and a load switch with adjustable OVP.

The DP/DM dual SPDT switch protection on the I/O pins can tolerate up to 20V with automatic shutoff circuitry to protect system components behind the switch.

The load switch features a low- R_{ON} internal FET and an operating range of $2.5V_{DC}$ to $25V_{DC}$ (absolute maximum of $30V_{DC}$). An internal clamp is capable of shunting surge voltages>100V, protecting downstream components and enhancing system robustness.

The internal ultra low-power comparator with a typical power supply current of 0.3μA. It has the best-in-class power supply current versus propagation delay performance. Featuring a push-pull output stage, the comparator allows for operation with absolute minimum power consumption when driving any capacitive or resistive load.

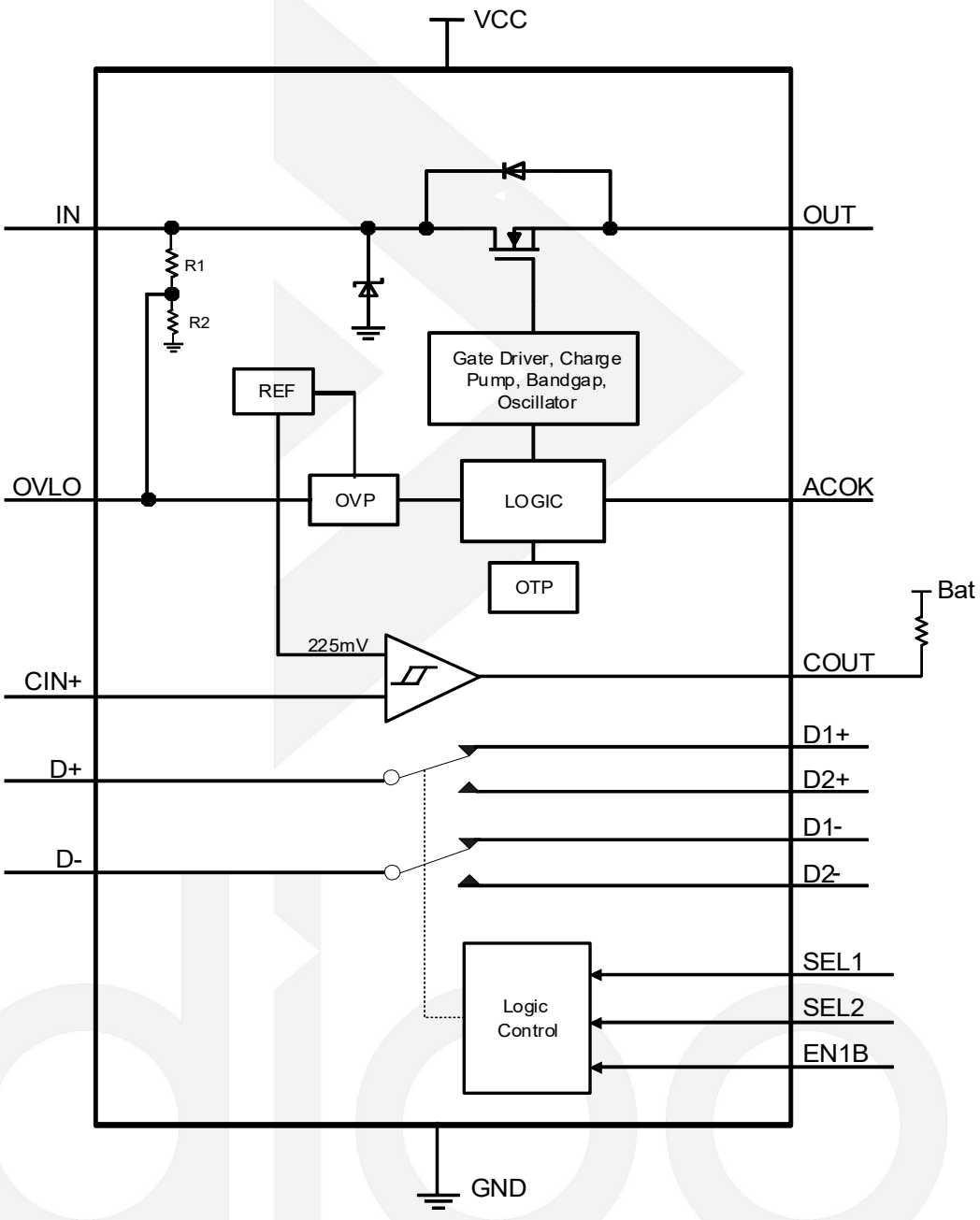
The DIO3480AH comes in a small WLCSP-24 package making it a perfect candidate for mobile and space constrained applications.

Ordering Information

Order Part Number	Top Marking		T_A	Package	
DIO3480AH	OPPD3480	Green	-40 to 85℃	WLCSP-24	Tape & Reel, 3000

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Function Block Diagram



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Pin Assignments

WLCSP-24

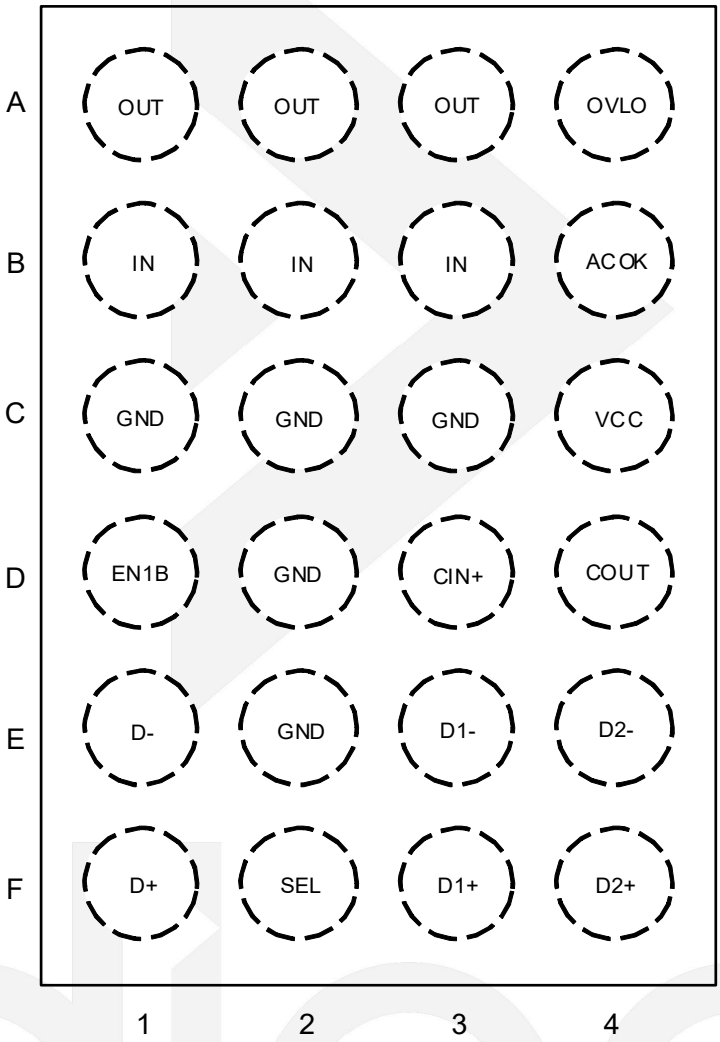


Figure 1 Top View

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Pin Description

Name	Bump	Type	Description
OUT	A1/A2/A3	O	Power switch output pin.
OVLO	A4	I/O	External OVLO adjustment pin.
IN	B1/B2/B3	PWR	Power switch input power supply pin.
ACOK	B4	O	Open drain power good output.
GND	C1/C2/C3/D2/E2	GND	Ground.
VCC	C4	PWR	Data line switches and comparator input power supply pin.
EN1B	D1	I	Active low enable, for power switch path only.
CIN+	D3	I	Comparator IN+.
COUT	D4	O	Open Drain Comparator OUT.
D-	E1	I/O	Common terminal 2.
D+	F1	I/O	Common terminal 1.
SEL	F2	I	Data line switch select, low for COM to NC, high for COM to NO.
D1-	E3	I/O	Normal closed terminal 2.
D1+	F3	I/O	Normal closed terminal 1.
D2-	E4	I/O	Normal open terminal 2.
D2+	F4	I/O	Normal open terminal 1.

Truth Table

Control Input, SEL	Function
Low Logic Level	D1+ connected to D+, D1- connected to D-
High Logic Level	D2+ connected to D+, D2- connected to D-

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Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter		Range	Unit
Over Voltage Protection Load Switch				
V_{IN}	V_IN to GND (1)(2)		-6 to 30	V
V_{OUT}	V_OUT to GND		-0.3 to V_{IN}+0.3	V
V_{OVLO}	OVLO to GND		-0.3 to 30	V
V_{EN1B_ACOK}	Maximum DC Voltage Allowed on EN1B or ACOK Pin		6	V
I_{IN}	Switch I/O Current (Continuous)		6	A
Surge	IEC 61000-4-5, Surge Protection	V_{IN}	±100	V
ESD	IEC 61000-4-2 System ESD (V_{BUS})	Air Gap	15.0	kV
		Contact	8.0	
DP/DM Dual SPDT Switch				
V_{CC}	Supply Voltage		-0.5 to 6	V
$V_{I/O}$	Input / Output DC Voltage (D+, D-)		-0.5 to 20	V
Surge	IEC 61000-4-5, Surge Protection	D+, D-	25	V
$V_{I/O}$	Input / Output DC Voltage (D1+/D1-, D2+/D2-)		-0.5 to 6	V
V_I	Digital Input Voltage (SEL)		-0.5 to 6	V
I_K	Input-Output Port Diode Current (D+, D-, D1+/D1-, D2+/D2-)		-50	mA
I_{IK}	Digital Logic Input Clamp Current (SEL) (V_I<0)		-50	mA
I_{CC}	Continuous Current Through VCC (Max)		100	mA
I_{GND}	Continuous Current Through GND (Min)		-100	mA
ESD	Human Body Model (All pins)		2	kV
Comparator				
Input Voltage			(CIN+)-0.3 to (CIN+)+0.3	V
Signal input terminals current			±10	mA
ESD Human Body Model (All pins)			2	kV
Temperature Items				
T_{STG}	Storage Temperature Range		-65 to 150	℃
T_J	Maximum Junction Temperature		150	℃
T_L	Lead Temperature (Soldering, 10 Seconds)		260	℃

(1) Maximum reverse current to V_{IN} pin less than 6A.

(2) For V_{IN}＞22V, I_{IN}＜200mA, clamp power is less than 4.5W.

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Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Rating	Unit
T_A	Operating Free-Air Temperature Industrial	-40 ~ 85	℃
Over Voltage Protection Load Switch			
V_{IN}	Supply Voltage	2.5 to 21	V
I_{OUT}	Output Current	5	A
DP/DM Dual SPDT Switch			
V_{CC}	Supply Voltage	2.3 ~ 5.5	V
$V_{I/O(D+,D-)}$	Analog Input /Output Voltage	0 ~ 18	V
$V_{I/O(D1+/D1-,\ D2+/D2-)}$		0 ~ 4.5	V
V_I	Digital Input Voltage (SEL)	0 ~ 5.5	V
$I_{I/O(D+,D-,\ D1+/D1-,\ D2+/D2-)}$	Analog Input /Output Port Continuous Current	-50 ~ 50	mA
Comparator			
Supply Voltage		2.3 ~ 5.5	V
Quiescent current	T_A=25°C	500 (Max)	nA
	T_A=–40°C to 125°C	1000 (Max)	nA

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Over Voltage Protection Load Switch Electrical Characteristics

T_A=-40℃ to 85℃, unless otherwise specified. Typical values are V_{IN}=5.0V, I_{IN}≤5A, C_{IN}=0.1μF and T_A=25℃.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN_CLAMP}	Input Clamping Voltage	I_{IN}=10mA		21.8	23	V
I_Q	Input Quiescent Current	V_{IN}=5V, EN1B=0V		85		μA
V_{UVLO}	Under Voltage Trip Level	V_{IN} Rising		2.25	2.4	V
		V_{IN} Falling		1.95	2.1	V
V_{IN_OVLO}	Internal Over-Voltage Trip Level	V_{IN} Rising, OVLO=GND	6.1	6.4	6.7	V
V_{OVLO_TH}	OVLO Set Threshold	V_{IN}=2.5V to V_{OVLO}	1.15	1.20	1.25	V
V_{OVLO_RNG}	Adjustable OVLO Threshold Range	V_{IN}=2.5V to V_{OVLO}	6		21	V
V_{OVLO_SELECT}	External OVLO Select Threshold		0.25	0.30	0.32	V
R_{ON}	Resistance from V_{IN} to V_{OUT}	V_{IN}=5V, I_{OUT}=1A, T_A=25℃		25	40	mΩ
C_{OUT}	OUT Load Capacitance	V_{IN}=5V			1000	μF
I_{OLVO}	OVLO Input Leakage Current	V_{OVLO}=V_{OVLO_TH}	-100		100	nA
T_{SDN}	Thermal Shutdown			130		℃
T_{SDN_HYS}	Thermal Shutdown Hysteresis			20		℃
Digital Signals						
V_{OL}	ACOK Output Low Voltage	I_{SINK}=1mA			0.4	V
V_{IH_EN1B}	Enable HIGH Voltage	V_{IN}=2.5V to V_{OVLO}	1.2			V
V_{IL_EN1B}	Enable LOW Voltage	V_{IN}=2.5V to V_{OVLO}			0.5	V
I_{ACOK_LEAK}	ACOK Leakage Current	V_{ACOK}=3V, ACOK Deserted	-0.5		0.5	μA
I_{EN1B_Leak}	EN1B Leakage Current	V_{IN}=5.0V, V_{OUT}=Float	-1.0		1.0	μA
Timing Characteristics						
t_{DEB}	Debounce Time	Time from 2.5V<V_{IN}<V_{IN_OVLO} to V_{OUT}=0.1 x V_{IN}		15		ms
t_{START}	Soft-Start Time	Time from V_{IN}=V_{IN_min} to 0.2 x ACOK, V_{IO}=1.8V with 10kΩ Pull-up Resistor		30		ms
t_{ON}	Switch Turn-On Time (2)	R_L=100Ω, C_L=22μF, V_{OUT} from 0.1 x V_{IN} to 0.9 x V_{IN}	1.5	2	4	ms
t_{OFF}	Switch Turn-Off Time(2)	R_L=100Ω, C_L=0μF, V_{IN}>V_{OVLO} to V_{OUT}=0.8 x V_{IN}		100		ns

(2) Guaranteed by characterization under room temperature.

Specifications subject to change without notice.

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DP/DM Dual SPDT Switch Electrical Characteristics

T_A=-40°C to 85°C, V_{CC}=2.3V to 5.5V, GND=0V, Typical values are at V_{CC}=3.3 V, T_A=25°C, (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply						
V_{CC}	Power Supply Voltage		2.3		5.5	V
I_{CC}	Active Supply Current	SEL=0V, 1.8V or V_{CC}, V_{CC}≤4.4V, 0V<$V_{I/O}$<3.6V T_A = 25°C to 65°C		30	35	μA
	Supply Current During OVP Condition	SEL=0V, 1.8V or V_{CC}, V_{CC}≤4.4V, $V_{I/O}$>V_{POS_THLD} T_A = 25°C to 65°C		30	35	μA
DC Characteristics						
R_{ON}	ON-State Resistance	$V_{I/O}$=0.4V, I_{SINK}=8mA, Refer to Figure 2.		5.5	9	Ω
ΔR_{ON}	ON-State Resistance Match Between Channels	$V_{I/O}$=0.4V, I_{SINK}=8mA, Refer to Figure 2.		0.3		Ω
$R_{ON\ (FLAT)}$	ON-State Resistance Match Flatness	$V_{I/O}$=0V to 0.4V, I_{SINK}=8mA, Refer to Figure 2.		0.09	0.4	Ω
Z_{ON}	ON State Impedance to GND		5	8		MΩ
Digital Characteristics						
V_{IH}	Input Logic High	SEL	1.4			V
V_{IL}	Input Logic Low	SEL			0.5	V
I_{IH}	Input High Leakage Current	SEL=1.8V, V_{CC}	-1	0.3	5	μA
I_{IL}	Input Low Leakage Current	SEL=0V	-1	0	5	μA
R_{PD}	Internal Pull-Down Resistor On Digital Input Pins			6		MΩ
C_I	Digital Input Capacitance	SEL=0V, 1.8V or V_{CC} f=1MHz		3.4		pF
Protection						
V_{OVP_TH}	OVP Positive Threshold		4.8	5.1	5.4	V
V_{OVP_HYST}	OVP Threshold Hysteresis		75	230	425	mV

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V_{CLAMP_V}	Maximum Voltage To Appear On D1+/- and D2+/- Pins During OVP Scenario	$V_{D+/-}$=0 to 16V t_{RISE} and t_{FALL}(10% to 90%)=100ns R_L=Open, Switch ON or OFF	0		9.0	V
		$V_{D+/-}$=0 to 16V t_{RISE} and t_{FALL}(10% to 90%)=100ns R_L=50Ω, Switch ON or OFF	0		9.0	V

Dynamic Characteristics

T_A=-40°C to 85°C, V_{CC}=2.3V to 5.5V, GND=0V, Typical values are at V_{CC}=3.3V, T_A=25°C, (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
C_{ON}	IO Pins ON Capacitance	$V_{D+/-}$=0 or 3.3V, f=240MHz Switch ON		4	6	pF
O_{ISO}	Differential OFF Isolation	R_L=50Ω, C_L=5pF, f=100kHz, Switch OFF, Refer to Figure 4.		-103		dB
		R_L=50Ω, C_L=5pF, f=240MHz, Switch OFF, Refer to Figure 4.		-30		dB
X_{TALK}	Channel To Channel Crosstalk	R_L=50Ω, C_L=5pF, f=100kHz, Switch ON, Refer to Figure 5.		-93		dB
BW	Bandwidth	R_L=50Ω, Switch ON, Refer to Figure 6.		1.2		GHz
I_{LOSS}	Insertion Loss	R_L=50Ω, f=240MHz, Switch ON, Refer to Figure 6.		-0.7		dB

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Comparator Electrical Characteristics

At T_A=25°C, V_{CC}=2.3V to 5V, C_L=15pF, unless otherwise noted.

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
Offset Voltage						
V_{REF}	Reference Voltage	T_A=25°C to 65°C	218.5	225	231.5	mV
V_{HYS}	Hysteresis			20	30	mV
dV_{OS}/dT	Input offset voltage drift	T_A=–40°C to 125°C			±70	μV/°C
PSRR	Power-supply rejection ratio	T_A=–40°C to 125°C		66		dB
CMRR	Common Mode Rejection Ratio	T_A=–40°C to 125°C		65		dB
Input Voltage Range						
V_{CM}	Common-mode voltage range	T_A=–40°C to 125°C	- 0.1		0.1	V
Input Bias Current						
I_B	Input bias current	T_A=25°C		30	100	pA
		T_A=–40°C to 125°C			20	nA
	Input offset current			8		pA
C_{LOAD}	Capacitive load drive			60		pF
Output Type		Open-Drain				

Switching Characteristics

At T_A=25°C, V_{CC}=2.3V to 5V, C_L=15pF, Output pull up to 1.8V by 10kΩ. unless otherwise noted.

Symbol	Parameter	Condition		MIN	TYP	MAX	Unit
t_{PHL}	Propagation delay time	High-to-low	Input overdrive=50mV			50	μs
			Input overdrive=100mV			50	
t_{PLH}		Low-to-high	Input overdrive=50mV			50	
			Input overdrive=100mV			50	
t_R	Rise time					300	ns
t_F	Fall time					300	
t_{ON}	Power up time					600	μs

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Detailed Description

USB2.0 High Speed (480Mbps) Switch Port

The DIO3480AH integrated a USB2.0 high speed (480Mbps) switch, which is designed to fully protect the USB Type-C data ports (D+ and D- differential data lines). The device can function as either two channel 2:1 multiplexer or 1:2 de-multiplexer. Meanwhile DIO3480AH can also be used in typical type C USB 2.0 data ports.

Secondly, The DIO3480AH can also be adopted in such applications where the USB data ports has potential short to VBUS with relatively higher charging voltage. In such scenario, DIO3480AH maintains excellent signal integrity and reliability via the internal OVP protection module (tolerate up to and even more than 20V DC) and up to 1.2GHz bandwidth data path.

OVP (Overvoltage Protection)

The OVP function of the DIO3480AH is designed to isolate the non-common ports from the potential shorts of common port D+/- lines to VBUS at the USB connector. By comparison, the DIO3480AH will immediately turn OFF the internal switches and isolate the rest of data path at lower voltage side (D1+/- and D2+/-) from the high voltage surge of more than 20V appearing at common ports side (D+/-).

Application Information

There are many USB designs in which the USB hubs or controllers have a limited number of USB I/Os or sharing the USB connector. The DIO3480AH can effectively expand the limited USB I/Os by multiplexing or de-multiplexing between multiple USB data lines to interface them to a single USB hub or controller or route signals from on connector to two different USB controllers. With the independent control of the two switches (via SEL1 and SEL2), DIO3480AH can be used to cross switch single-ended signals in non-USB applications.

Typical Application

The DIO3480AH is used to switch signals between the USB paths, which goes to the baseband/application processor, or the UART pins, which goes to debug port. The DIO3480AH has integrated the 6MΩ pull-down resistors at SEL1, SEL2, and OEB pins. The pull-down at SEL1 and SEL2 pins ensure the D1+/D1- channel is selected by default. The pull-down on OEB enables the switch when power is up.

Design Advice

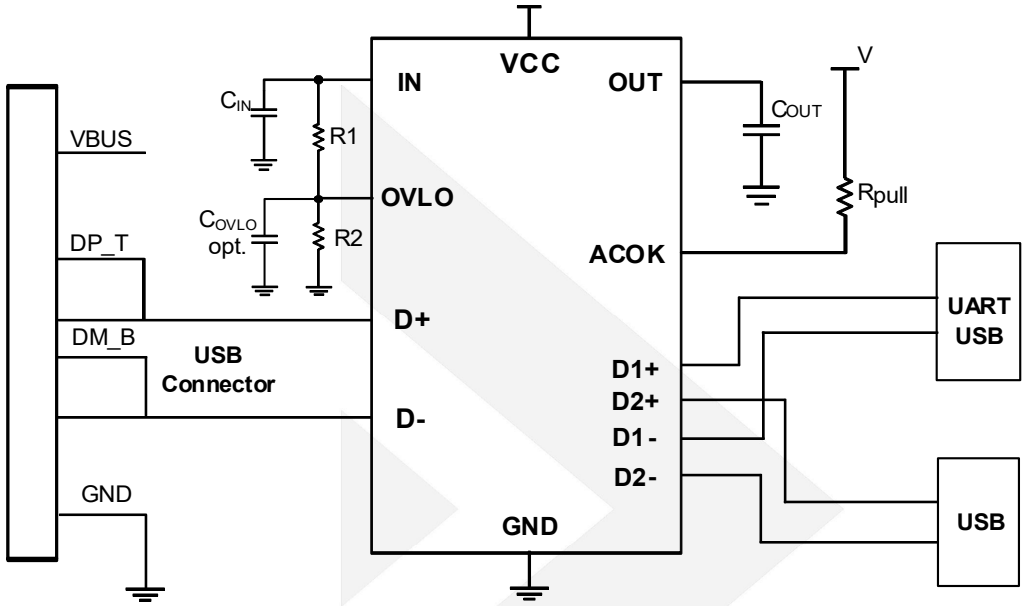
The DIO3480AH can function properly without any external components. However, it is highly recommended that unused pins must be connected to ground through a 50Ω resistor to prevent signal reflections back into the device. A 100nF bypass capacitor is recommended to be placed close to DIO3480AH VCC pin.

On-The-Go (OTG) Functionality

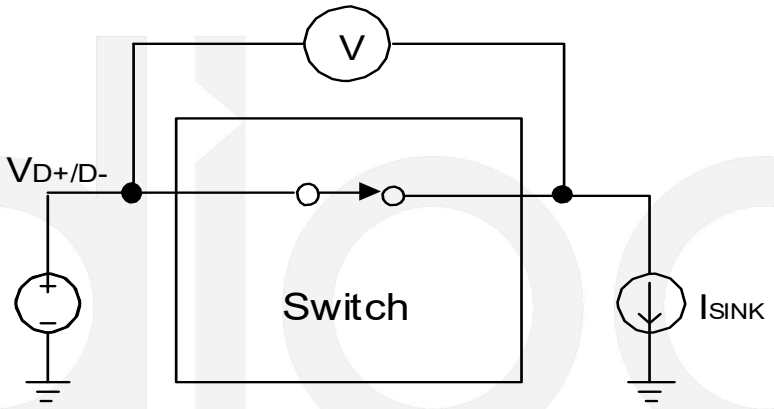
During OTG operation, the integrated OVP load switch is initially disabled and the power FET's bulk diode is forward biased. The bulk diode represents ~0.7V drop across the device, which remains until the V_IN voltage increases past 2.5V, when the device is fully enabled. While the device is disabled and the body diode is forward biased, the max DC current through the diode is 1.8A. This current is limited by the thermal performance of the device (0.7V x 1.8A=1.36W). The EN1B pin must be pulled LOW to ensure the device fully enables and the transient should not exceed the RC time constant of the C_IN and C_OUT capacitors. At the system level, over-voltage and current protection should be provided outside the DIO3480AH.

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Application Information



Test Diagram



Channel ON, $R_{ON}=V/I_{SINK}$

Figure 2 ON-State Resistance (R_{ON})

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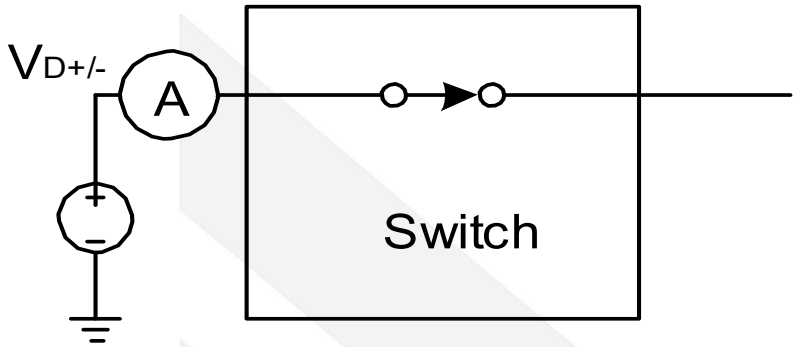


Figure 3 ON Leakage

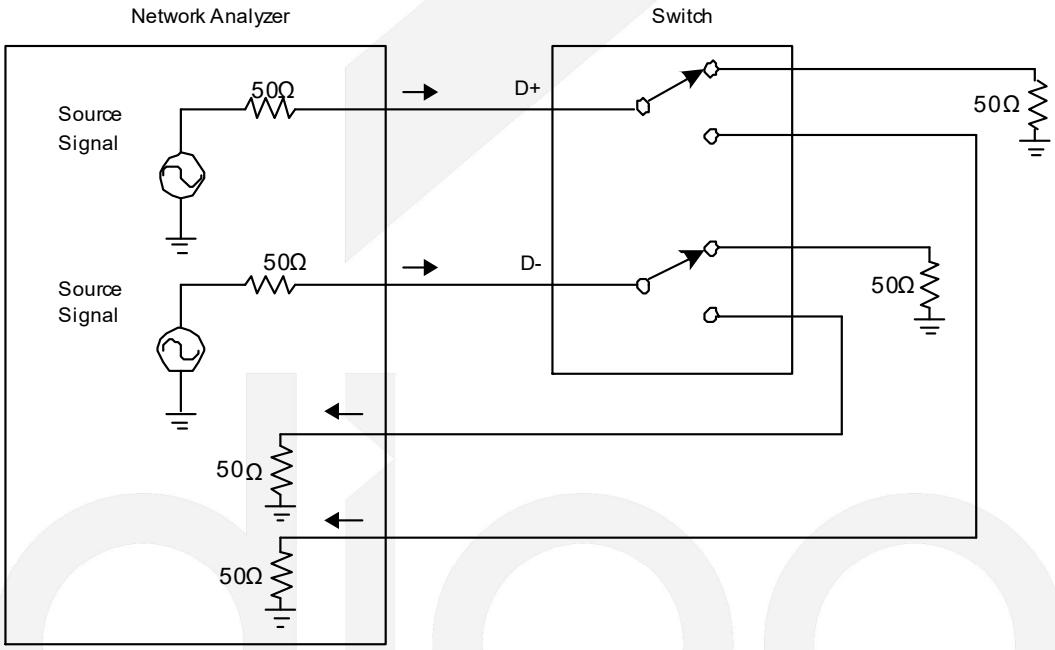


Figure 4 OFF Isolation

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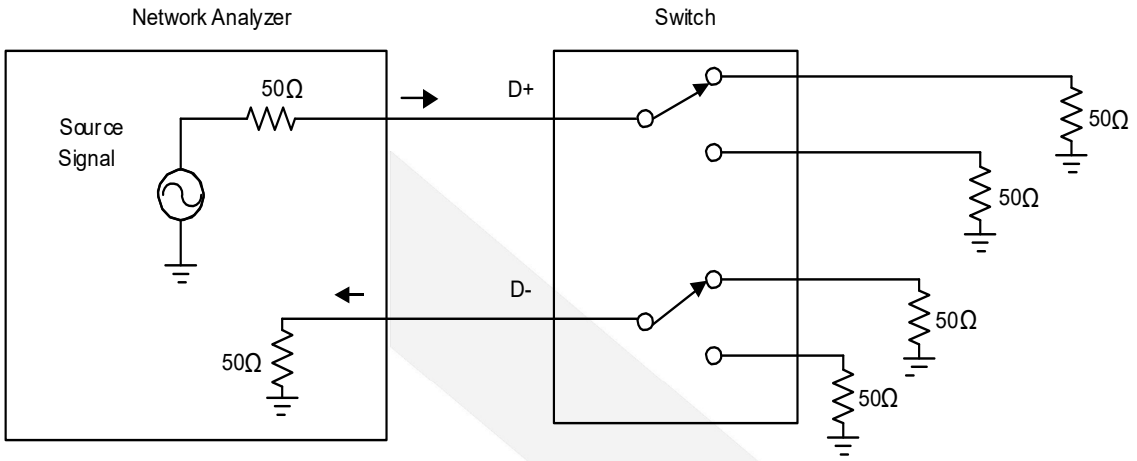


Figure 5 Cross Talk

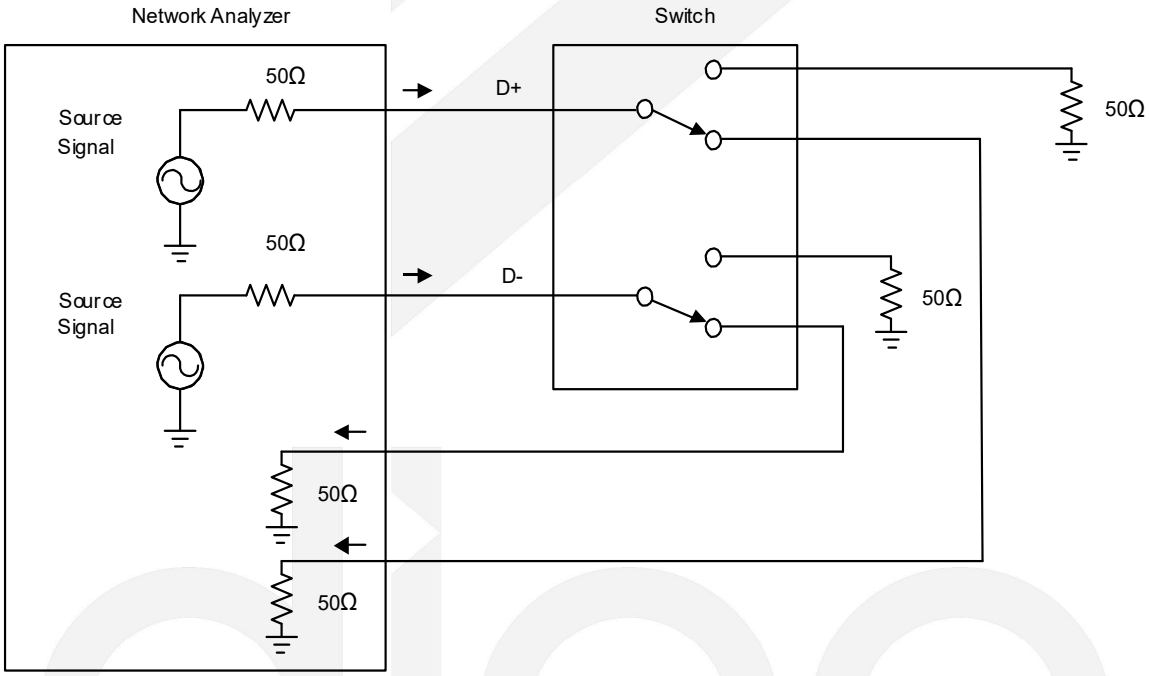


Figure 6 BW and Insertion Loss

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Typical Performance Characteristic

At T_A=25°C, V_{CC}=2.3V to 5V, C_L=15pF, unless otherwise noted.

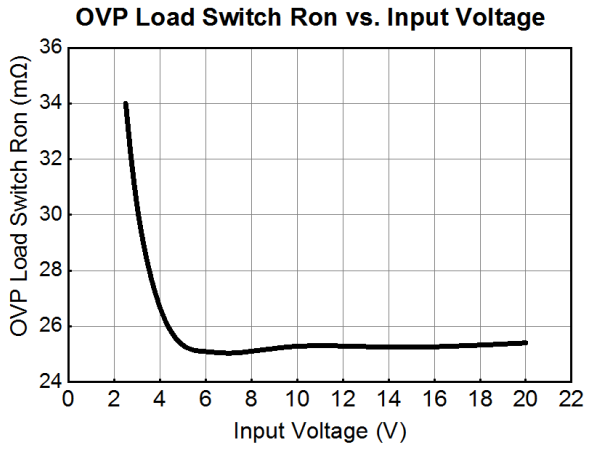


Figure 1. OVP Load Switch Ron Vs. Input Voltage (I_{Load}=1A)

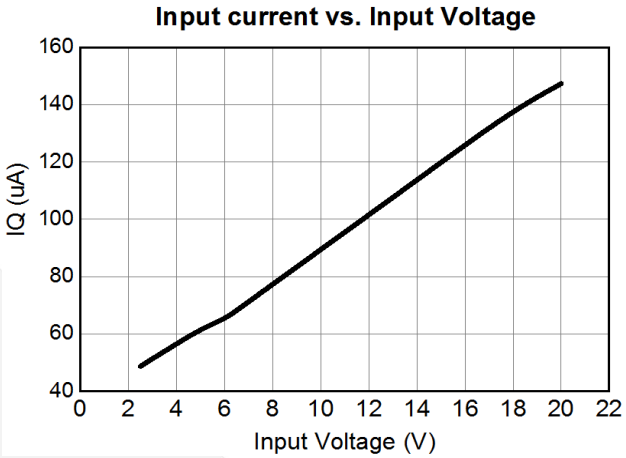


Figure 2. Input current Vs. Input Voltage (No Load)

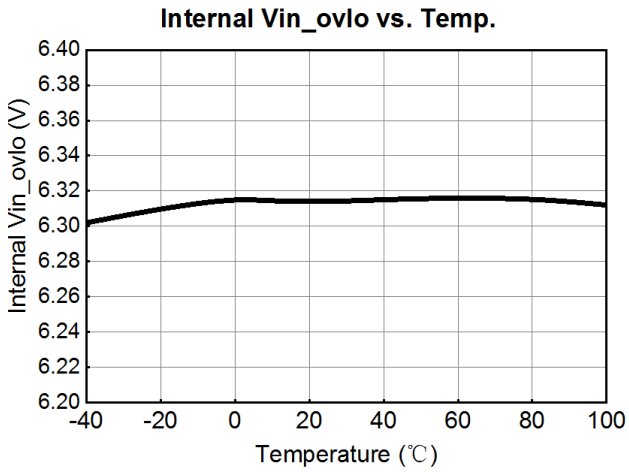


Figure 3. Internal V_{IN_OVLO} Vs. Temp.

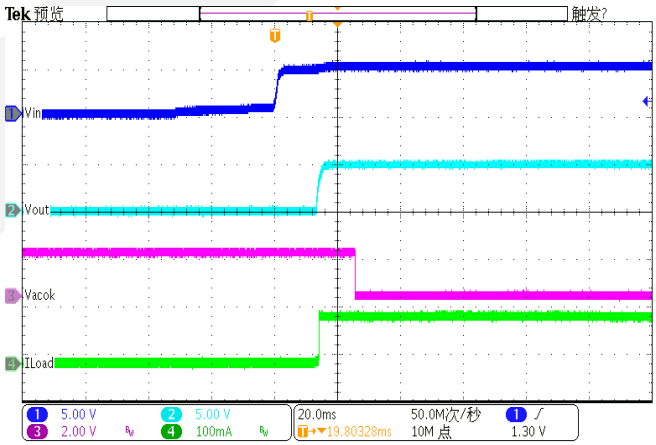


Figure 4. Power-up (C_{IN}=1uF, C_{OUT}=1uF, Load=100mA)

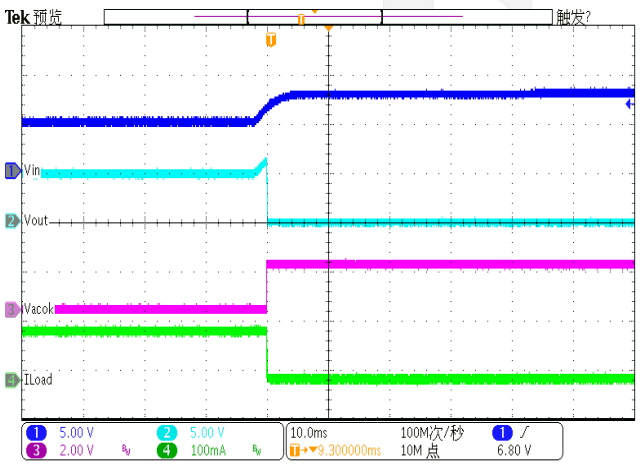


Figure 5. Internal Over voltage Protection (V_{IN} 5V to 8V step , C_{IN}=1uF , C_{OUT}=1uF)

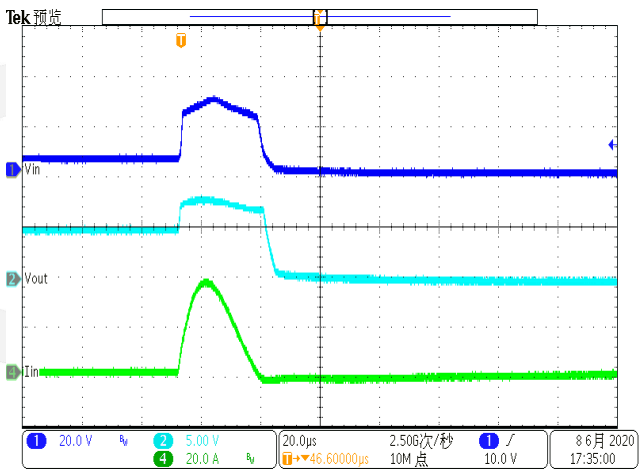


Figure 6. Surge Transient（100V）

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