
DZ001

Audio/Video Sub-system with Integrated 6dB CVBS Video Filter 3-Vrms Audio Line Driver, 0.4W Mono Audio Amplifier

Features

- Line Output:able to drive 600Ω and 10kΩ
 - 3Vrms With 5V Supply Voltage
 - No Pop/Clicks Noise at the line output when PowerON/OFF
 - No Need for Output DC-Blocking Capacitors
 - Accepting Single terminal Input and differential Input
- SD Filter: One-ch 6th-order 11MHz SD filters
 - 6dB Output Driver Gain
 - Drive Dual Video Load
 - Transparent Input Clamping
 - AC or DC Coupled Inputs/Outputs
- Optimized Frequency Response between 20Hz–20kHz
- Class AB:
 - When using a 8Ω load, the output power of more than 0.4W
 - Drivable load range
 - Fewer external components
 - Low total harmonic distortion
 - Reduce background noise function

Applications

- DVD Players
- Video Amplifiers
- Set-Top Boxes
- Personal Video Recorders
- Communications Devices

Descriptions

The DZ001 is an integrated solution for Video driver and Audio driver, with two separated modules, the Audio Line Driver module and One Channel 6th order SD Video filter driver module.

The Audio Line Driver allow for the removal of output AC-coupling capacitors. It is designed to optimize the audio driver circuit performance while reducing the BOM cost by eliminating the peripheral discrete components for noise reduction. It is able to offer 3Vrms output at 600Ω load with 5V supply.

The 6th-order SD Video filter driver provides improved image quality compared with passive LC filters and discrete driver solution, especially suited for standard definition video signals. It can be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal diode-like clamps and bias circuitry may be used if AC-coupled inputs are required. The output can also drive AC or DC coupled single (150Ω) or dual (75Ω) loads. The DC coupling capacitors can be removed.

The Class-AB driver can be a low supply voltage (minimum 3.135V) under conditions of maximum differential output drives the speaker, not need coupling capacitors open-loop gain of up to 80dB, the closed-loop gain through two peripheral resistor.

DZ001

Pin Assignment

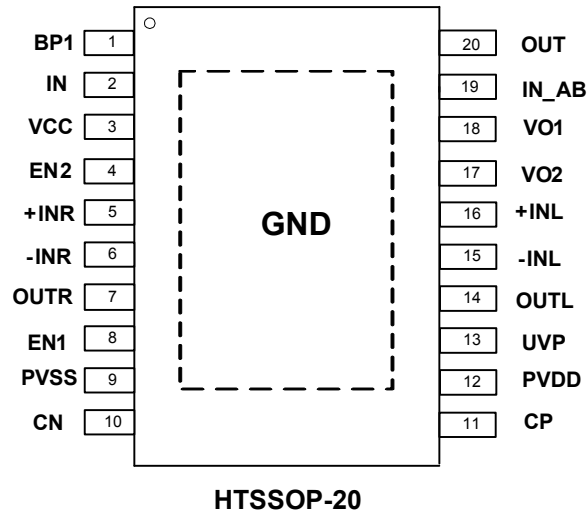


Figure 1 Pin Assignment

Pin Description

Pin Name	Description
BP1	Bypass pin with 1 μ F capacitor to GND
IN	Video filter driver Input
VCC	Video filter driver and Class AB driver power supply
EN2	Enable Class AB driver (Internal a 1.8M Ω resistor connected to GND)
+INR	Right channel Positive Input
-INR	Right channel Negative Input
OUTR	Right channel Output
EN1	Enable Audio driver
PVSS	Negative Supply Voltage
CN	Charge-pump flying capacitor negative terminal
CP	Charge-pump flying capacitor positive terminal
PVDD	Audio line driver positive supply
UVP	Under voltage protection input, Also enable Class AB driver.
OUTL	Left channel Output
-INL	Left channel Negative Input
+INL	Left channel Positive Input
VO2	Output pins to external speakers
VO1	
IN_AB	Class-AB Negative Input
OUT	Video filter driver Output

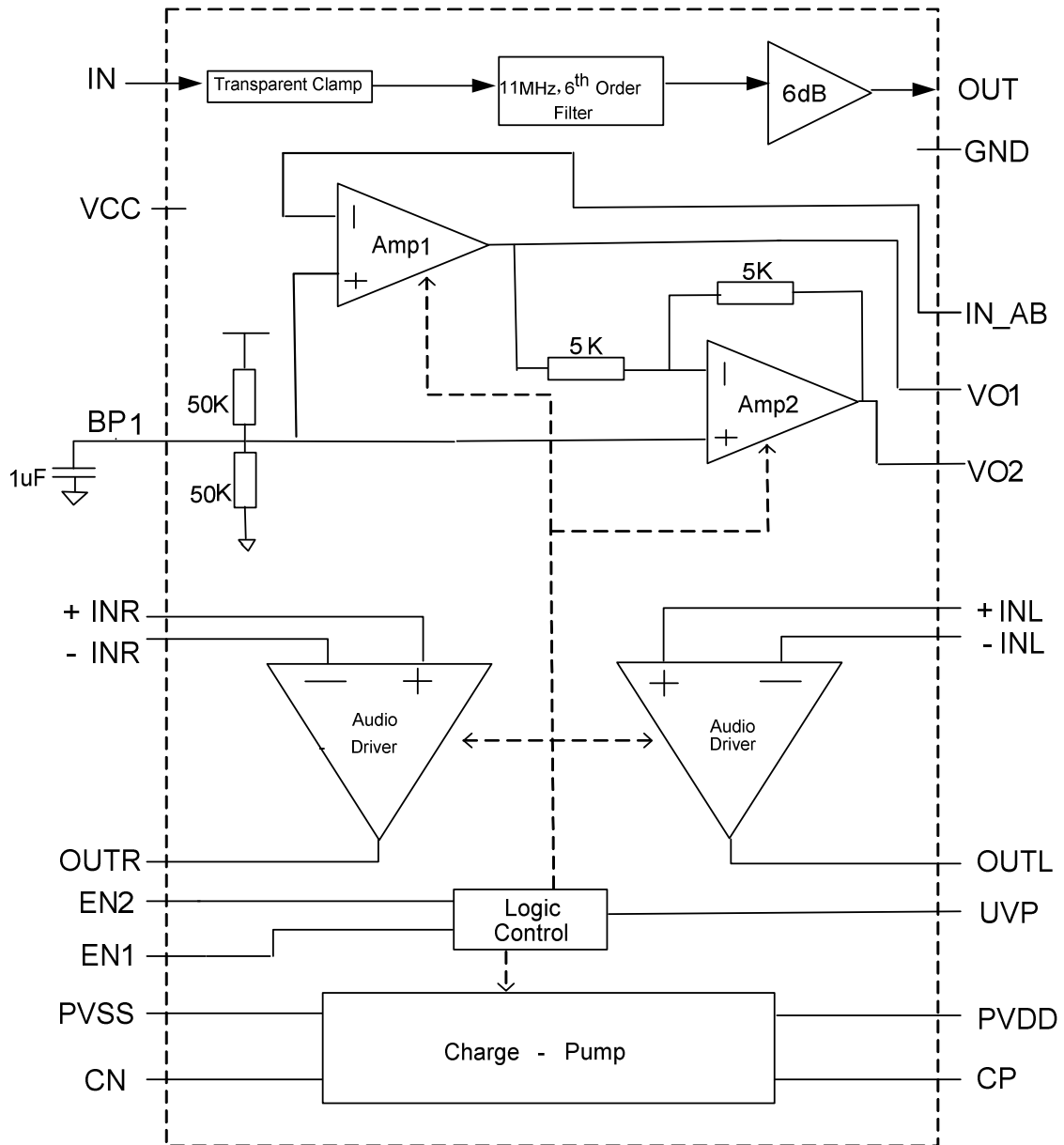
DZ001

GND

Power ground

Note: VCC and PVDD must power up together.

Block Diagram



DZ001

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter		Rating	Unit
Supply Voltage/VCC		0 to 6.0	V
Supply Voltage/PVDD		-0.3 to 7.5	V
Input Voltage/VIN		-0.3 to $V_{CC}+0.3$	V
Input Voltage(+/-INR,+/-INL)		$V_{PVSS}-0.3$ to $V_{DD}+0.3$	V
Minimum load impedance	Audio Line driver	600	Ω
	Class AB driver	8	Ω
EN1 to GND		-0.3 to $V_{DD}+0.3$	V
V_{O1}, V_{O2}		-0.3~ $V_{CC}+0.3$	V
Storage Temperature Range		-65 to 150	$^{\circ}\text{C}$
Junction Temperature		150	$^{\circ}\text{C}$
Lead Temperature Range		260	$^{\circ}\text{C}$
HBM ESD JEDEC: JESD22-A114	Output Pins	8	kV
	All Pins	5	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation to ensure optimal performance to the datasheet specifications. DIOO does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
PVDD	Supply Voltage	3.135	5	5.5	V
VCC	Supply Voltage	3.135	5	5.5	V
V_{IH}	EN1 / EN2 High level Input Voltage	1.2			V
V_{IL}	EN1/ EN2 Low level Input Voltage			0.4	V
T_A	Operating Temperature Range	-40		85	$^{\circ}\text{C}$

Notes: The items below were divided into three parts, the Audio Line driver module, the SD Video filter module and the Class AB driver module.

DZ001

Electrical Characteristics for the Audio Line Driver module

Typical value: $T_A = 25^\circ\text{C}$, $V_{DD}=5\text{V}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OS}	Input Offset Voltage	$V_{DD}=5\text{V}$, Input grounded, Gain=100	-3	0	3	mV
PSRR	Power supply rejection ratio	$V_{DD}=5\text{V}$		90		dB
V_{OH}	High level output voltage	$V_{DD}=5\text{V}$, $R_L=2.5\text{k}\Omega$	4.9			V
V_{OL}	Low level output voltage	$V_{DD}=5\text{V}$, $R_L=2.5\text{k}\Omega$			-4.80	V
I_{IH}	EN1 High level input current	$V_{DD}=5\text{V}$, $V_I=V_{DD}$			1	μA
I_{IL}	EN1 Low level input current	$V_{DD}=5\text{V}$, $V_I=0\text{V}$			1	μA
I_{DD}	Supply current	$V_{DD}=5\text{V}$, $V_I=V_{DD}$, No load		12		mA
		Shutdown mode, $V_{DD}=5\text{V}$			1	
V_O	Output Voltage	THD=1%, $V_{DD}=5\text{V}$, $f=1\text{kHz}$, $R_L=100\text{k}\Omega$	3.1			V_{RMS}
THD+N	Total harmonic distortion + noise	$V_O=3V_{RMS}$, $f=1\text{kHz}$, $R_L=10\text{k}\Omega$		0.001		%
X_{TALK}	Channel crosstalk	$V_O=3V_{RMS}$, $f=1\text{kHz}$		95		dB
I_O	Maximum output current	$V_{DD}=5\text{V}$		60		mA
SNR	Signal noise ratio	$V_O=3V_{RMS}$, $BW=22\text{kHz}$, A-weighted		112		dB
SR	Slew rate			12		$\text{V}/\mu\text{s}$
V_N	Noise output voltage	$BW=20\text{Hz}$ to 22kHz		5.1		μV_{RMS}
G_{BW}	Unity gain bandwidth			7		MHz
A_{VO}	Open loop voltage gain			140		dB
V_{UVP}	External under-voltage detection		1.08	1.11	1.14	V
I_{Hys}	External under-voltage detection hysteresis current			5		μA

Electrical Characteristics for the SD Video Filter module

Typical value: $T_A = 25^\circ\text{C}$, $V_{CC}=5\text{V}$, $R_{SOURCE}=37.5\Omega$, $R_L=150\Omega$ loads; all inputs are AC couple with $0.1\mu\text{F}$; all outputs are AC coupled with $220\mu\text{F}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC ELECTRICAL CHARACTERISTICS						
I_{CC}	Supply Current			8	12	mA
V_{IN}	Video Input Voltage Range		GND	1.4		V_{PP}
PSRR	Power Supply Rejection			50		dB
DYNAMIC PERFORMANCE						
AV	Channel Gain		5.8	6.0	6.2	dB
f_{1dB}	-1dB Bandwidth		8.0	10.5		MHz

DZ001

f _{3dB}	-3dB Bandwidth		9	11.8		MHz
	Filter Response	f=27MHz		-40		dB
DG	Differential Gain			0.2		%
DP	Differential Phase			0.36		°
THD	Output Distortion	f=1MHz		0.38		%
SNR	Signal to Noise Ratio			70		dB
	Group Delay	f=400kHz, 6.5MHz		20		ns
CLG_SD	Chroma Luma Gain	f=3.58MHz ref to SD in at 400kHz	95	100	105	%
CLD_SD	Chroma Luma Delay	f=3.58MHz ref to SD in at 400kHz		5.5		ns

Notes: SNR=20 • log (714mV / rms noise).

Electrical Characteristics for the Class AB driver module

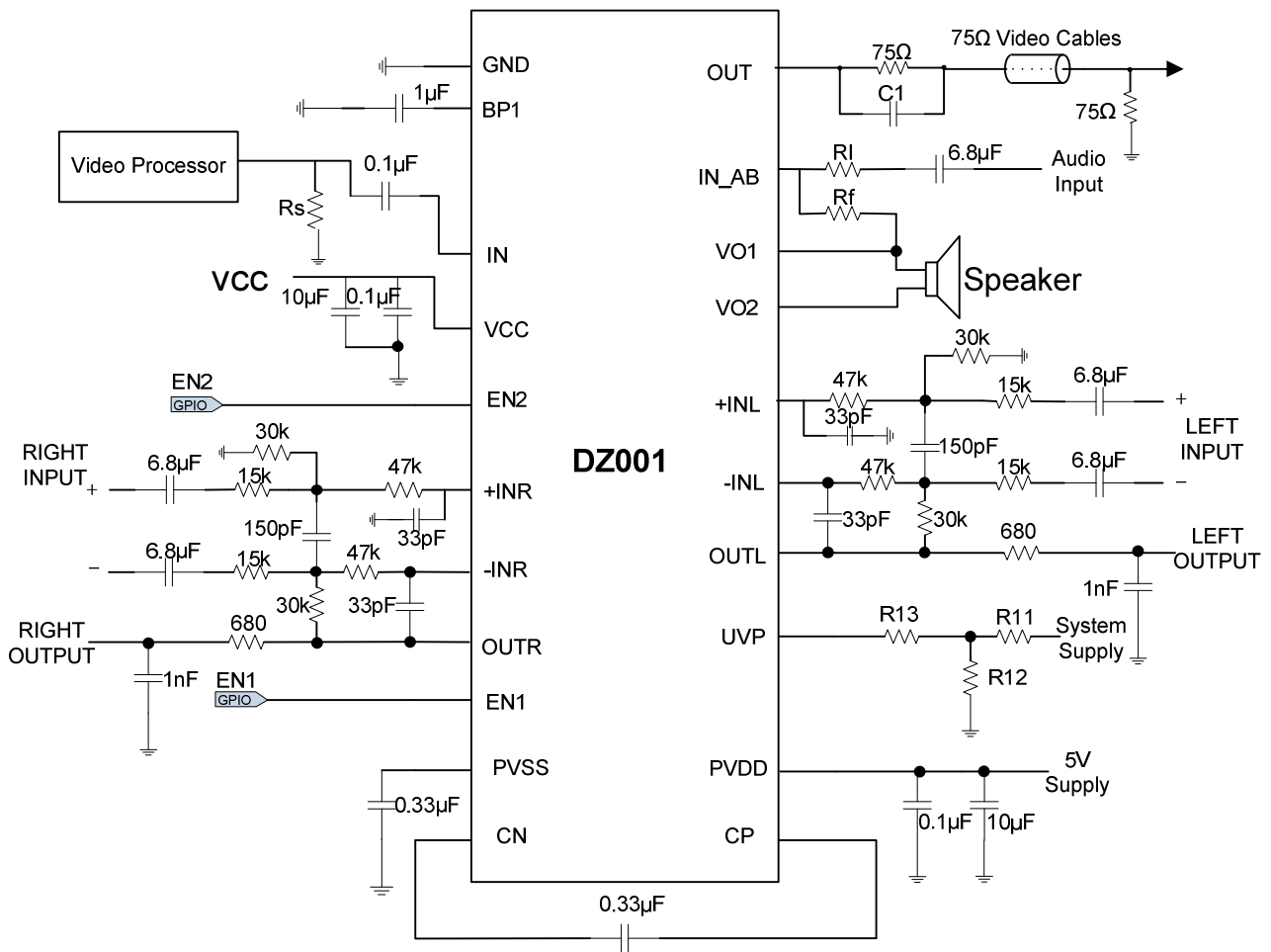
Typical value: T_A = 25°C, V_{CC}=5V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC ELECTRICAL CHARACTERISTICS						
I _{CC}	Supply Current	V _{CC} =5V, EN2=1.2V		9		mA
		V _{CC} =5V, EN2=0.4V		55	100	µA
V _O	Output Voltage	R _L =8Ω, R _f =75kΩ, V _{CC} =5V		V _{CC} /2		V
V _{OO}	Output offset voltage	R _L =8Ω, R _f =75kΩ, V _{CC} =5V	-30	0	30	mV
V _{OH}	High level output voltage	3<V _{CC} <5V, I _{out} =-500mA		V _{CC} -0.1		V
V _{OL}	Low level output voltage	3<V _{CC} <5V, I _{out} =-500mA		0.1		V
REQ	Equivalent resistance	Pin 3		50		kΩ
DYNAMIC PERFORMANCE						
G _{VO1}	Open-loop gain		80			dB
G _{VO2}	Close-loop gain	F=1kHz, R _L =8Ω	-0.35	0	0.35	dB
P _O	Output Power	V _{CC} =5V, R _L =8Ω, THD=1%	0.4			W
		V _{CC} =5V, R _L =8Ω, THD=10%	0.5			
THD	Output Distortion	V _{CC} =5V, R _L =8Ω, P _O =125mW		0.4		%
		V _{CC} =5V, R _L =8Ω, P _O =250mW		1		
GBW	Unity gain bandwidth			16		MHz
PSRR	Power Supply Rejection		50			dB
GV(EN2)		EN2=0.4V, 1kHz<f<20kHz	70			dB

Specifications subject to change without notice.

DZ001

Typical Application

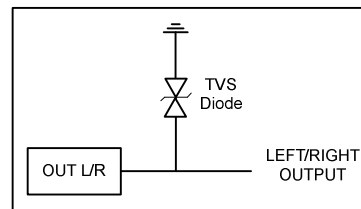


Notes:

1. In some applications, if the power supply noise needs to be filtered, the ferrite bead is recommended in a value of 600Ω@100MHz, instead of RC network. RC network normally will lower the power supply resulting in the degraded the audio performance. If the resistor is not chosen properly, which can trigger the internal UVP detection circuit and mute the output. As depicted below.



2. In order to protect the device against the power surge, transient voltage suppressor (TVS) devices are recommended at the output pins OUTL/OUTR.



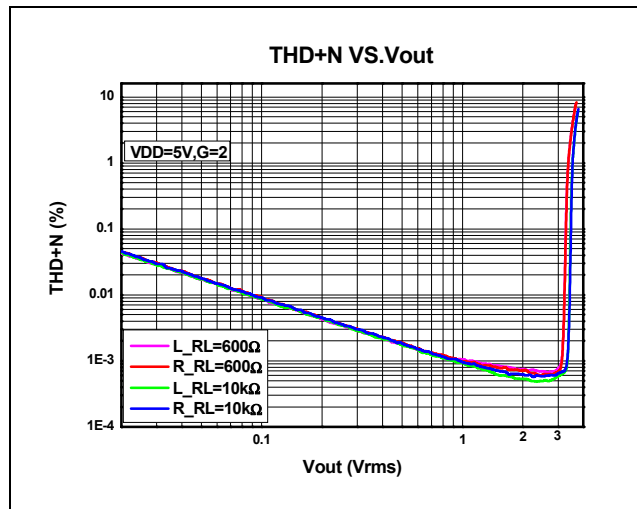
3: Class AB: $Gain = 2 \times \frac{Rf}{RI}$

DZ001

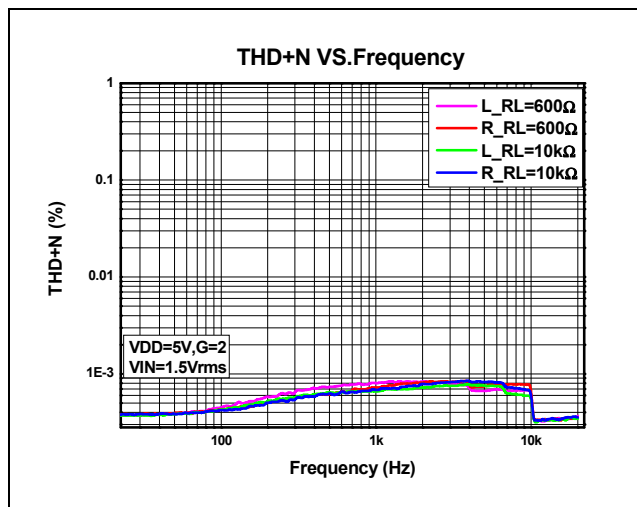
Typical Performance Characteristics

At $T_A = +25^\circ\text{C}$, $C_{\text{PUMP}}=0.33\mu\text{F}$, $C_{\text{PVSS}}=0.33\mu\text{F}$, unless otherwise noted.

THD+N vs. OUTL/OUTR



THD+N vs. Frequency



DZ001

Application Notes

Gain-Setting Resistors Ranges and Input-Blocking Capacitors

The gain-setting resistors, R_{IN} and R_{FB} , must be chosen so that noise, stability, and input capacitor size of the Audio line driver are kept within acceptable limits. Voltage gain is defined as R_{FB} divided by R_{IN} .

Table 1 lists the recommended resistor value for different gain settings. Selecting values that are too low demands a large input ac-coupling capacitor C_{IN} . Selecting values that are too high increases the noise of the amplifier.

The gain-setting resistor must be placed close to the input pins to minimize capacitive loading on these input pins and to ensure maximum stability.

Table 1 Resistor Values Recommended

Input Res./ R_{IN}	Feedback Res./ R_{fb}	Differential Gain	Inverting Gain	Non-inverting Gain
22 k Ω	22 k Ω	1 V/V	-1 V/V	2 V/V
15 k Ω	30 k Ω	2 V/V	-2 V/V	3 V/V
10 k Ω	100 k Ω	10 V/V	-10 V/V	11 V/V

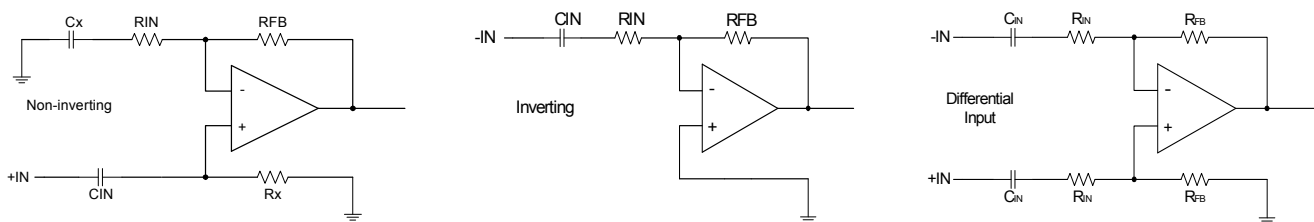


Figure 2 Differential, Inverting and Non-inverting Gain Configurations

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the Audio line driver. These capacitors block the dc portion of the audio source and allow the Audio line driver inputs to be properly biased to provide maximum performance.

These capacitors form a high-pass filter with the input resistor, R_{IN} . The cutoff frequency is calculated using the equation below. For this calculation, the capacitance used is the input-blocking capacitor, and the resistance is the input resistor chosen from Table 1; then the frequency and/or capacitance can be determined when one of the two values is given.

2nd Order Filter Typical Application

Several audio DACs used today require an external low-pass filter to remove out-of-band noise. This is possible with the Audio Line Driver, as it can be used like a standard OPAMP. Several filter topologies can be implemented, both single-ended and differential. In Figure 3, a multi-feedback (MFB) with differential input and single-ended input is shown.

DZ001

An ac-coupling capacitor to remove dc content from the source is shown; it serves to block any dc content from the source and lowers the dc-gain to 1, helping reducing the output dc-offset to minimum. The resistor values should have a low value for obtaining low noise, but should also have a high enough value to get a small size ac-coupling capacitor.

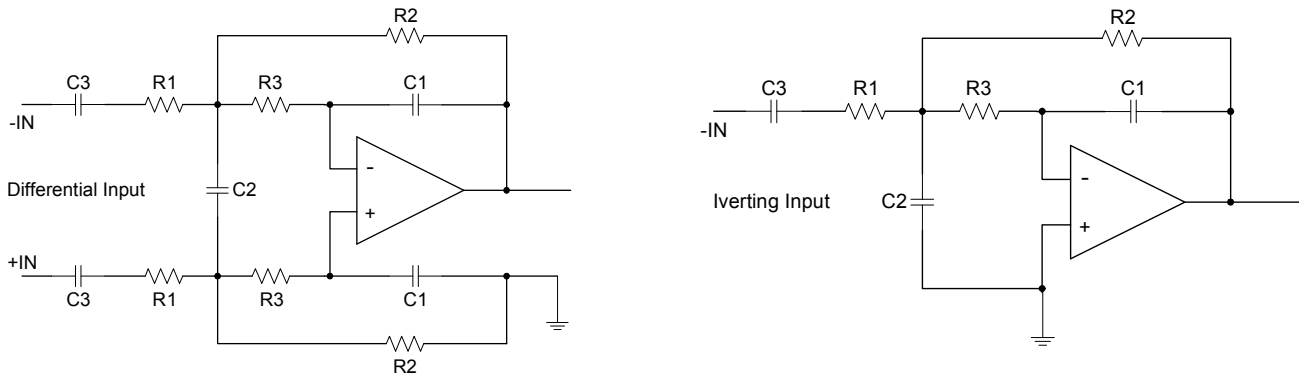


Figure 3 Second-Order Active Low-Pass Filter

Charge Pump Flying Capacitor and PVSS Capacitor

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The PVSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low ESR X5 or X7 capacitors are recommended selection, and a value of $0.33\mu\text{F}$ is typical. Capacitor values that are smaller than $0.33\mu\text{F}$ can be used, but the maximum output voltage may be reduced and the device may not operate to specifications.

Decoupling Capacitors

The Audio line driver requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically a combine of paralleled $0.1\mu\text{F}$ and $10\mu\text{F}$, placed as close as possible to the device VDD lead works best. Placing this decoupling capacitor close to the Audio line driver is important for the performance of the amplifier. For filtering lower-frequency noise signals, a $10\mu\text{F}$ or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Pop-Free Power-Up

Pop-free power up is ensured by keeping the EN1 (enable pin) low during power-supply ramp up and ramp down. The EN1 pin should be kept low until the input ac-coupling capacitors are fully charged before asserting the EN1 pin high to achieve pop-less power up. Figure 4 illustrates the preferred sequence.

DZ001

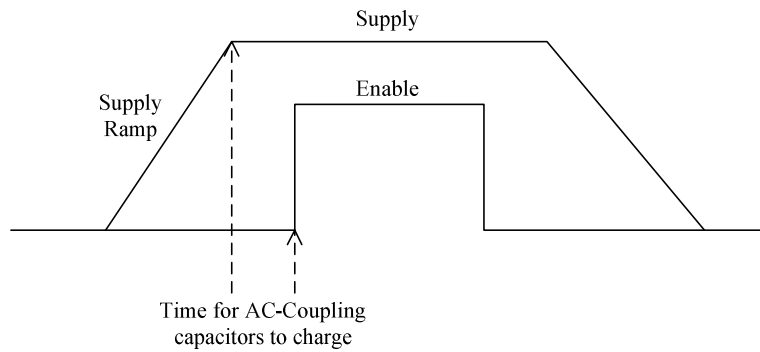


Figure 4 Power-Up Sequences

External Under-voltage Detection

External under-voltage detection can be used to mute/shut down the DZ001 before an input device can generate a pop. Although the shutdown voltage is 1.11V typically, customers need to consider the accuracy of system passive components such as resistors and associated temperature variation. Users often select a resistor divider to obtain the power-on and shutdown threshold for the specific application. The typical thresholds can be calculated as follows, respectively for VSUP_MO at 5V and 12V. Usually for best power down noise performance, 12V supply is recommended for UVP circuitry as below. Typically this 12V is the power supply which generates the 5V supply for DZ001 VDD pins.

Case 1: VSUP_MO= 12V (Recommended)

$$V_{UVP} = (1.11V - 6\mu A * R_{13}) * (R_{11} + R_{12}) / R_{12};$$

$$V_{hysteresis} = 5\mu A * R_{13} * (R_{11} + R_{12}) / R_{12};$$

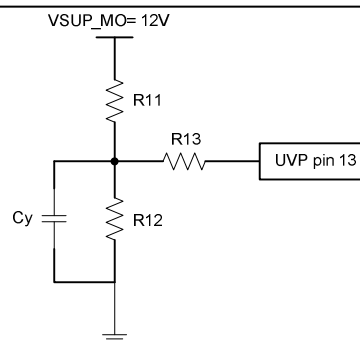
With the condition $R_{13} \gg R_{11} // R_{12}$.

For example, if $R_{11} = 11k$, $R_{12} = 1.4k$ and $R_{13} = 47k$,

Then $V_{UVP} = 7.334V$; $V_{hysteresis} = 2.081V$

Here, V_{UVP} is the shutdown threshold.

In this case, the voltage at UVP pin 13 is greater than 1.311V under worst case of VSUP_MO ripples.



Case 2: VSUP_MO= 5.0V

$$V_{UVP} = (1.11V - 6\mu A * R_{13}) * (R_{11} + R_{12}) / R_{12};$$

$$V_{hysteresis} = 5\mu A * R_{13} * (R_{11} + R_{12}) / R_{12};$$

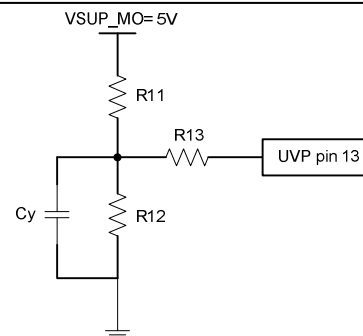
With the condition $R_{13} \gg R_{11} // R_{12}$.

For example, if $R_{11} = 5.6k$, $R_{12} = 2.2k$ and $R_{13} = 47k$,

Then $V_{UVP} = 2.936V$; $V_{hysteresis} = 0.833V$

Here, V_{UVP} is the shutdown threshold.

In this case, the voltage at UVP pin 13 is greater than 1.368V under worst case of VSUP_MO ripples.



DZ001

To minimize the system power-up and power-down threshold variations, resistors with less than 1% variations are recommended. Although some resistor value options are offered above for customer's reference or starting points, customers should always verify those resistor options in their actual design. Customer can adjust their own design to achieving the best performance between pop noise and power-on threshold by adjusting the passive resistors R11, R12 and R13.

Capacitive Load

The Audio line driver has the ability to drive a high capacitive load up to 220 pF directly. Higher capacitive loads can be accepted by adding a series resistor of 47 Ω or larger.

DZ001

CONTACT US

Dioo is a professional design and sales corporation for high-quality and performance analog semiconductors. The company focuses on industry markets, such as, cell phone, handheld products, laptop, and medical equipment and so on. Dioo's product families include analog signal processing and amplifying, LED drivers and charger IC. Go to <http://www.dioo.com> for a complete list of Dioo product families.

For additional product information, or full datasheet, please contact with our Sales Department or Representatives.