DIO8018

7-Channel LDO PMIC for Camera Applications

Features

- LDO1 and LDO2:
  - input voltage: 0.6 V ~ 2.0 V
  - output current: 1500 mA
  - output voltage:
  0.504 V ~ 1.504 V at 8 mV/step
  - dropout: 120 mV at 1.2 V, 1500 mA output
  - ±0.5% (typ) accuracy
- LDO3, LDO4 and LDO6
  - input voltage: 1.8 V ~ 5.5 V
  - output current: 300 mA
  - output voltage:
  1.500 V ~ 3.412 V at 8 mV/step
  - dropout: 100 mV at 2.8 V, 300 mA
  - ±0.5% (typ) accuracy
- LDO5 and LDO7
  - input voltage: 1.8 V ~ 5.5 V
  - output current: 600 mA
  - output voltage:
  1.500 V ~ 3.412 V at 8 mV/step
  - dropout: 135 mV at 2.8 V, 600 mA
  - ±0.5% (typ) accuracy
- Fault interrupt
- Over temperature protection
- Programmable power up sequence
- 20-Ball WLCSP package (1.61 mm × 1.96 mm), 0.35 mm pitch

Applications

- Smart phones
- IP cameras
- Camera modules

Descriptions

The DIO8018 is a PMIC with 7 integrated LDOs. The PMIC has 2 low dropout LDOs for high current DVDD and 5 high PSRR LDOs for noise-sensitive power rails. The DIO8018 has 5 independent input pins for individual LDOs; VIN12 is for LDO1 and LDO2; VIN34 is for LDO3 and LDO4; VIN5 for LDO5, VIN6 for LDO6 and VIN7 for LDO7. The DIO8018 has a separate system input, VSYS, which is the bias pin for the LDOs.

The output voltage and power-up sequence of LDOs can be set through the I²C interface. The DIO8018 also integrates the fault monitoring features with interrupt indication.

The 7-bit I²C address of the device is 011 0101 by default but can be reprogrammed so that multiple devices can be connected to the same I²C bus.

The DIO8018 is available in 1.61 mm × 1.96 mm, 20-ball WLCSP package. The device is Pb-free and halogen-free.

Block Diagram

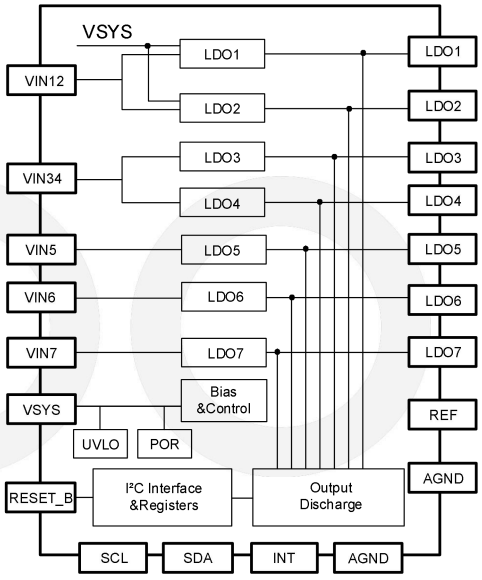


Figure 1. Application Block Diagram

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Typical Applications

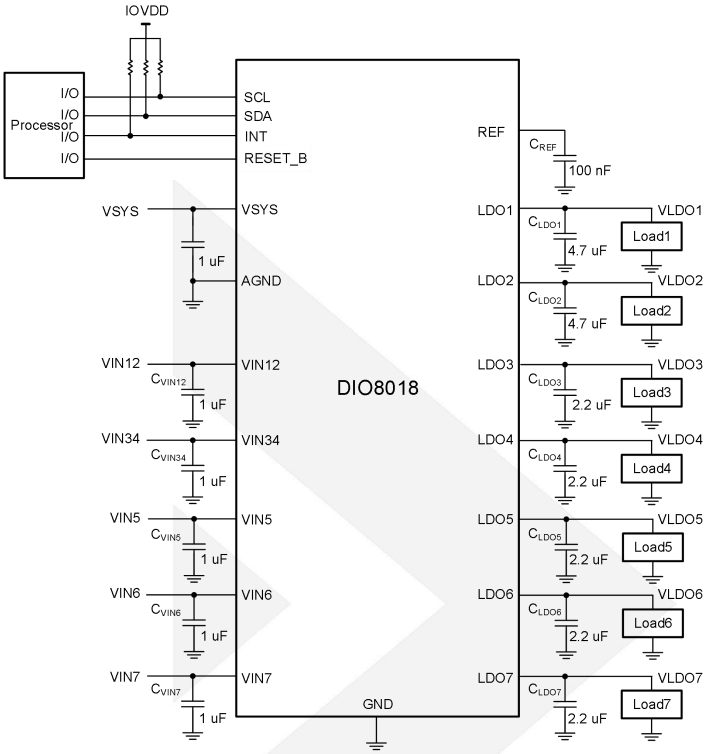


Figure 2. Typical Applications

Note:

Select a minimum effective capacitance of 3.5 μF for C_{LDO1-2}, considering capacitance changes with temperature, DC bias and package size;

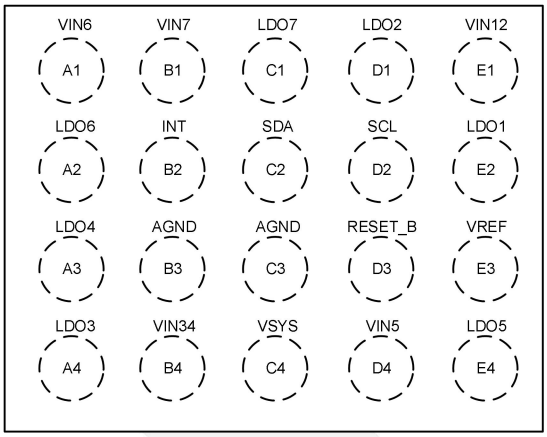
Select a minimum effective capacitance of 1.5 μF for C_{LDO3-7}, considering capacitance changes with temperature, DC bias and package size.

Ordering Information

Order Part Number	Top Marking	RoHS	T_A	Package	
DIO8018WL20	DV1H	Green	-40 to 85°C	WLCSP-20	Tape & Reel, 3000

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Pin Assignment



WLCSP-20 (Top View)

Figure 3. Pin Configuration

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Pin Descriptions

Pin	Name	Description
A1	VIN6	LDO6 input
A2	LDO6	LDO6 output
A3	LDO4	LDO4 output
A4	LDO3	LDO3 output
B1	VIN7	LDO7 input
B2	INT	The fault interrupt pin is active high, indicating that an interrupt event has occurred. Open-drain or push-pull mode selected by 0x12 bit<6>; the output voltage of push-pull can be selected to 1.2 V or 1.8 V by 0x12 bit<7>. This pin returns to low when all I^2C interrupt bits is 0.
B3	AGND	Ground
B4	VIN34	LDO3 and LDO4 input
C1	LDO7	LDO7 output
C2	SDA	I^2C data line
C3	AGND	Ground
C4	VSYS	VSYS input
D1	LDO2	LDO2 output
D2	SCL	I^2C clock
D3	RESET_B	The RESET_B pin is used to enable basic circuits that are necessary for controlling the PMIC. The pin has an internal 100 nA pull-down current and should always be connected to a logic high or low.
D4	VIN5	LDO5 input
E1	VIN12	LDO1 and LDO2 input
E2	LDO1	LDO1 output
E3	VREF	The reference bypass pin. Connect a 0.1 µF ~ 0.47 µF capacitor between this pin and analog ground.
E4	LDO5	LDO5 output

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Absolute Maximum Ratings

Stresses beyond those listed under the Absolute Maximum Rating table may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Rating	Unit
V_{IN12}	LDO1 and LDO2 input voltage	−0.5 ~ 3.0	V
V_{SYS}	Handset power-supply voltage	−0.5 ~ 6.5	V
V_{IN34}, V_{IN5}, V_{IN6}, V_{IN7}	LDO3, LDO4, LDO5, LDO6, LDO7 input voltage	−0.5 ~ 5.5	V
V_{CTRL}	Serial clock, serial data, interrupt and RESET_B pin	−0.5 ~ V_{SYS} + 0.3	V
I_{PIN_MAX}	Current on single pin	1500	mA
T_L	Lead temperature range (soldering 10 s)	260	°C
T_{STG}	Storage temperature	-55 ~ 150	°C
T_J	Operating junction temperature range	-40 to 150	°C
ESD	HBM	2000	V
	CDM	1500	V

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating	Unit
V_{IN12}	VIN12 operating supply voltage range	0.6 ~ 2.0	V
V_{IN34}, V_{IN5}, V_{IN6}, V_{IN7}	VIN3 to VIN7 operating supply voltage range	1.8 ~ V_{SYS}	V
V_{SYS}	VSYS	2.5 ~ 5.5	V
T_A	Operating temperature range	-40 ~ 85	°C
θ_{JA}(1)	Thermal resistance	40.4	°C/W

Note:

(1) Surface mounted on FR4 board using 1.5 inch*1.5 inch FR4 copper (1 $inch^2$/1 Oz)

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DC Electrical Characteristics

Minimum and maximum values are at V_{SYS} = 2.5 V or ($V_{LDO1,2}$ + 1.6 V), whichever is greater; V_{IN12} = 0.6 to 2 V and $V_{IN12} \geq V_{LDO1,2}$ + 200 mV; $V_{IN34,5,6,7}$ = 1.8 to 5.5 V and $V_{IN34,5,6,7} \geq V_{LDO3,4,5,6,7}$ + 300 mV. T_J = -40°C to + 125°C unless otherwise noted. Typical values are at T_A = 25°C; V_{SYS} = 3.8 V; V_{IN12} = 1.5 V; V_{IN34} = V_{IN5} = V_{IN6} = V_{IN7} = 3.6 V; $V_{LDO1,2}$ = 1.2 V, $V_{LDO3,4,5,6,7}$ = 2.8 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{SYS}	Input voltage range		2.5		5.5	V
V_{IN34}, V_{IN5}, V_{IN6}, V_{IN7}			1.8		5.5	
V_{IN12}			0.6		2.0	
LDO1,2	Output voltage accuracy	T_A = 25°C; $LDO_{1,2}$ = 1.2 V		±0.5		%
LDO3,4,5,6,7		T_A = 25°C; $LDO_{3,4,5,6,7}$ = 2.804 V		±0.5		
V_{SYS_UVLO}	VSYS under-voltage lockout threshold	Rising		2.35		V
		Falling		2.25		
V_{IN12_UVLO}	VIN12 under-voltage lockout threshold	Rising		0.55		V
		Falling		0.45		
V_{INH_UVLO}	VIN3,4,5,6,7 under-voltage lockout threshold	Rising		1.7		V
		Falling		1.6		
I_{GND}	Supply quiescent current	RESET_B = "1", all channels are OFF		25		μA
		LDO1 is ON		70		
		LDO1,2 are ON		115		
		LDO1,2,3 are ON		140		
		LDO1,2,3,4 are ON		160		
		LDO1,2,3,4,5 are ON		185		
		LDO1,2,3,4,5,6 are ON		210		
		LDO1,2,3,4,5,6,7 are ON		250		
		RESET_B = 5.5 V, disable IC through I^2C		2		
I_{SD}	Supply current shutdown	EN = GND, V_{IN} = 3.6 V		2		μA

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LDO1,2	Output voltage range	When V_{OUT} + 200 mV ≤ V_{IN12}, V_{SYS} ≥ 2.5 V & V_{SYS} ≥ V_{OUT} + 1.6 V	0.504		1.504	V
LDO3,4	Output voltage range	When V_{OUT} + 200 mV ≤ V_{IN34} & V_{IN34} ≥ 2 V, V_{SYS} ≥ 2.5 V & V_{SYS} ≥ V_{VIN34}	1.5		3.412	V
LDO5		When V_{OUT} + 200 mV ≤ V_{IN5} & V_{IN5} ≥ 2 V, V_{SYS} ≥ 2.5 V & V_{SYS} ≥ V_{IN5}				
LDO6		When V_{OUT} + 200 mV ≤ V_{IN6} & V_{IN6} ≥ 2 V, V_{SYS} ≥ 2.5 V & V_{SYS} ≥ V_{IN6}				
LDO7		When V_{OUT} + 200 mV ≤ V_{IN7} & V_{IN7} ≥ 2 V, V_{SYS} ≥ 2.5 V				
LDO1,2	Dropout voltage (1)	I_{OUT_TARGET} = 1500 mA, V_{OUT_TARGET} = 1.2 V, V_{SYS} = 3.6 V		120	150(2)	mV
LDO3,4,6		I_{OUT_TARGET} = 300 mA, V_{OUT_TARGET} = 2.8 V, V_{SYS} = 3.6 V		100		
LDO5,7		I_{OUT_TARGET} = 600 mA, V_{OUT_TARGET} = 2.8 V, V_{SYS} = 3.6 V		135		
LDO1,2	Max load current		1500			mA
LDO3,4,6			300			
LDO5,7			600			
$\Delta V_{OUT1,2}$	Line regulation _ V_{SYS}	V_{OUT} = 1.2 V, I_{OUT} = 1 mA, V_{IN12} = 1.5 V, V_{SYS} = 3.5 V ~ 5.5 V		0.5		mV
$\Delta V_{OUT3,4,5,6,7}$		V_{OUT} = 2.8 V, I_{OUT} = 1 mA, V_{IN_TARGET} = 3.3 V, V_{SYS} = 3.5 V ~ 5.5 V		0.1		
$\Delta V_{OUT1,2}$	Line regulation _ V_{IN}	V_{SYS} = 5.5 V, V_{OUT} = 1.2 V, I_{OUT} = 1 mA, V_{IN12} = 1.5 V ~ 3 V		0.1		mV
$\Delta V_{OUT3,4,5,6,7}$		V_{SYS} = 5.5 V, V_{OUT_TARGET} = 2.8 V, I_{OUT} = 1 mA, V_{IN_TARGET} = 3.3 V ~ 5.5 V		0.1		
$\Delta V_{OUT1,2}$	Load regulation	I_{OUT_TARGET} = 1 mA ~ 1000 mA		6		mV
$\Delta V_{OUT3,4,5,6,7}$		I_{OUT_TARGET} =1 mA ~ 250 mA		3		
LDO1,2	Output current limit	V_{OUT} = 90% $V_{OUT(NOM)}$, 0x02 [0 or 1] = 0	1000	1300		mA
LDO1,2		V_{OUT} = 90% $V_{OUT(NOM)}$, 0x02 [0 or 1] = 1	1500	1800		
LDO3,4,6		V_{OUT} = 90% $V_{OUT(NOM)}$, 0x02 [2 or 3 or 5] = 0	350	450		
LDO3,4,6		V_{OUT} = 90% $V_{OUT(NOM)}$, 0x02 [2 or 3 or 5] = 1	500	650		
LDO5,7		V_{OUT} = 90% $V_{OUT(NOM)}$, 0x02 [4 or 6] = 0	500	650		
LDO5,7		V_{OUT} = 90% $V_{OUT(NOM)}$, 0x02 [4 or 6] = 1	700	950		

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LDO1,2	Short circuit current	0x02 [0 or 1] = 0		250	350		mA
LDO1,2		0x02 [0 or 1] = 1		500	660		
LDO3,4,6		0x02 [2 or 3 or 5] = 0		180	240		
LDO3,4,6		0x02 [2 or 3 or 5] = 1		210	280		
LDO5,7		0x02 [4 or 6] = 0		260	350		
LDO5,7		0x02 [4 or 6] = 1		300	410		
LDO1,2	Turn-on time	V_{OUT_TARGET} = 1.2 V, C_{OUT_TARGET} = 4.7 µF, from assertion of enable signal to V_{OUT} start ramp up			25		µS
LDO3,4,5,6,7		V_{OUT_TARGET} = 2.8 V, C_{OUT_TARGET} = 2.2 µF, from assertion of enable signal to V_{OUT} start ramp up			25		µS
LDO1,2	Soft-start time	V_{OUT_TARGET} = 1.2 V, C_{OUT_TARGET} = 4.7 µF, V_{OUT} from 0 to 95% V_{OUT}			240		µS
LDO3,4,5,6,7		V_{OUT_TARGET} = 2.8 V, C_{OUT_TARGET} = 2.2 µF, V_{OUT} from 0 to 95% V_{OUT}			240		µS
LDO1,2	Output noise	f = 10 Hz to 100 kHz, I_{OUT_TARGET} = 20 mA			20		µVrms
LDO3,4,5,6,7		f = 10 Hz to 100 kHz, I_{OUT_TARGET} = 20 mA			10		µVrms
$PSRR_{L1,2_VIN}$	Power supply rejection ratio on VIN12	LDO1,2 (V_{IN12} to V_{OUT}), V_{IN12} = 1.5 V + 0.2 V_{PP}, V_{SYS} = 3.8 V, V_{OUT_TARGET} = 1.2 V, I_{OUT_TARGET} = 150 mA, C_{IN_TARGET} = 1 µF, C_{OUT_TARGET} = 4.7 µF	f = 100 Hz		85		dB
			f = 1 kHz		79		
			f = 10 kHz		60		
			f = 100 kHz		40		
			f = 1 MHz		40		
$PSRR_{L1,2_VSYS}$	Power supply rejection ratio on VSYS	LDO1,2 (V_{SYS} to V_{OUT}) V_{IN12} = 1.5 V, V_{SYS} = 3.8 V + 0.2 V_{PP}, V_{OUT_TARGET} = 1.2 V, I_{OUT_TARGET} = 150 mA, C_{IN_TARGET} = 1 µF, C_{OUT_TARGET} = 4.7 µF	f = 100 Hz		83		dB
			f = 1 kHz		77		
			f = 10 kHz		66		
			f = 100 kHz		33		
			f = 1 MHz		43		
$PSRR_{L3_VIN}$	Power supply rejection	LDO3 (V_{IN_TARGET} to V_{OUT})	f = 100 Hz		90		dB

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	ratio on VIN3	V_{IN_TARGET} = 3.6 V + 0.2 V_{PP}, V_{SYS} = 3.8 V, V_{OUT_TARGET} = 2.8 V, I_{OUT_TARGET} = 100 mA, C_{IN_TARGET} = 1.0 μF, C_{OUT_TARGET} = 2.2 μF	f = 1 kHz		92		
			f = 10 kHz		87		
			f = 100 kHz		68		
			f = 1 MHz		45		
$PSRR_{L4_VIN}$	Power supply rejection ratio on VIN4	LDO4 (V_{IN_TARGET} to V_{OUT}) V_{IN_TARGET} = 3.6 V + 0.2 V_{PP}, V_{SYS} = 3.8 V, V_{OUT_TARGET} = 2.8 V, I_{OUT_TARGET} = 100 mA, C_{IN_TARGET} = 1.0 μF, C_{OUT_TARGET} = 2.2 μF	f = 100 Hz		85		dB
			f = 1 kHz		92		
			f = 10 kHz		88		
			f = 100 kHz		67		
			f = 1 MHz		45		
$PSRR_{L5_VIN}$	Power supply rejection ratio on VIN5	LDO5 (V_{IN_TARGET} to V_{OUT}) V_{IN_TARGET} = 3.6 V + 0.2 V_{PP}, V_{SYS} = 3.8 V, V_{OUT_TARGET} = 2.8 V, I_{OUT_TARGET} = 100 mA, C_{IN_TARGET} = 1.0 μF, C_{OUT_TARGET} = 2.2 μF	f = 100 Hz		90		dB
			f = 1 kHz		90		
			f = 10 kHz		85		
			f = 100 kHz		73		
			f = 1 MHz		46		
$PSRR_{L6_VIN}$	Power supply rejection ratio on VIN6	LDO6 (V_{IN_TARGET} to V_{OUT}) V_{IN_TARGET} = 3.6 V + 0.2 VPP, VSYS = 3.8 V, V_{OUT_TARGET} = 2.8 V, I_{OUT_TARGET} = 100 mA, C_{IN_TARGET} = 1.0 μF, C_{OUT_TARGET} = 2.2 μF	f = 100 Hz		85		dB
			f = 1 kHz		87		
			f = 10 kHz		83		
			f = 100 kHz		65		
			f = 1 MHz		44		
$PSRR_{L7_VIN}$	Power supply rejection ratio on VIN7	LDO7 (V_{IN_TARGET} to V_{OUT}) V_{IN_TARGET} = 3.6 V + 0.2 V_{PP}, V_{SYS} = 3.8 V, V_{OUT_TARGET} = 2.8 V, I_{OUT_TARGET} = 100 mA, C_{IN_TARGET} = 1.0 μF, C_{OUT_TARGET} = 2.2 μF	f = 100 Hz		90		dB
			f = 1 kHz		85		
			f = 10 kHz		82		
			f = 100 kHz		69		
			f = 1 MHz		44		
$PSRR_{L3,4,5,6,7_VSYS}$	Power supply rejection	LDO3,4,5,6,7 (V_{SYS} to V_{OUT})	f = 100 Hz		85		dB

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	ratio on VSYS	V_{IN12} = 1.5 V, V_{IN_TARGET} = 3.6 V, V_{SYS} = 3.8 V + 0.2 V_{PP}, V_{OUT_TARGET} = 2.8 V, I_{OUT_TARGET} = 100 mA, C_{IN_TARGET} = 1.0 µF, C_{OUT_TARGET} = 2.2 µF	f = 1 kHz		92		
			f = 10 kHz		79		
			f = 100 kHz		56		
			f = 1 MHz		45		
T_{WRN}	Thermal warning				115		°C
T_{SD}	Thermal shutdown				150		°C
T_{HYS}	Thermal hysteresis for T_{SD} and T_{WRN}				25		°C
LDO1,2	Active output discharge resistance				100		Ω
LDO3,4,5,6,7					100		
LDO1,2	Line transient	V_{IN} = ($V_{OUT(NOM)}$ + 2.2 V) to ($V_{OUT(NOM)}$ + 1 V) in 10 µs, I_{OUT} = 1 mA		-1			mV
		V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to ($V_{OUT(NOM)}$ + 2 V) in 30 µs, I_{OUT} = 1 mA				1	
LDO3,4,5,6,7		V_{IN} = ($V_{OUT(NOM)}$ + 2.2 V) to ($V_{OUT(NOM)}$ + 1 V) in 10 µs, I_{OUT} = 1 mA		-1			
		V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to ($V_{OUT(NOM)}$ + 2 V) in 30 µs, I_{OUT} = 1 mA				1	
LDO1,2	Load transient	I_{OUT_TARGET} = 1 mA to 500 mA in 5 µs			-30		mV
		I_{OUT_TARGET} = 500 mA to 1 mA in 5 µs			30		
LDO3,4,5,6,7		I_{OUT_TARGET} = 1 mA to 300 mA in 5 µs			-20		
		I_{OUT_TARGET} = 300 mA to 1 mA in 5 µs			20		
RESET_B Logic Inputs							
I_{LEAK}	Input leakage				0.1	0.5	µA
V_{IH}	Input HIGH voltage			0.8			V
V_{IL}	Input LOW voltage					0.4	V
INT Logic Output							
I_{LEAK}	Input leakage				0.1	0.2	µA
V_{OH}	Output HIGH voltage	I_{OUT} = 10 mA		1.0	1.2		V

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V_{OL}	Input LOW voltage	I_{SINK} = 10 mA			0.3	V
I²C Logic						
I_{LEAK}	Input leakage			0.1	0.2	μA
V_{IH}	Input HIGH voltage	T_A = -40°C ~ 85°C	0.95			V
V_{IL}	Input LOW voltage				0.4	V
I_{OL}	SDA sink current		20			mA
F_{SCL}	SCL clock frequency		100	400	1000	kHz
t_{BUF}	Bus-free time between STOP and START conditions		0.5			us
$t_{HD;STA}$	START or repeated START hold time		260			ns
t_{LOW}	SCL LOW period		0.5			ns
t_{HIGH}	SCL HIGH period		260			ns
$t_{SU;STA}$	Repeated START setup time		260			ns
$t_{SU;DAT}$	Data setup time		50			ns
$t_{VD;DAT}$	Data valid time				450	ns
$t_{VD;ACK}$	Data valid acknowledge time				450	ns
t_R	SDA and SCL rise time				120	ns
t_F	SDA and SCL fall time		6.55		120	ns
$t_{SU;STO}$	Stop condition setup time		260			ns
Ci	SDA and SCL input capacitance		10			pF
Cb	Capacitive load for SDA and SCL		550			pF
t_{SP}	Spike pulse width that input filter must be suppress		0		50	ns

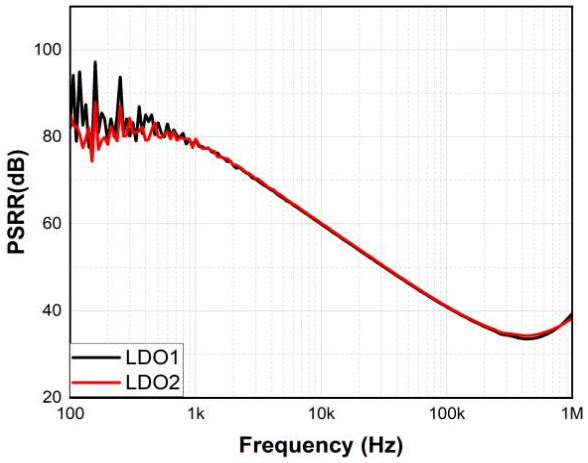
Note:

(1) Specification only guaranteed by design.

(2) Maximum dropout value is 150 mV at 25°C; maximum dropout value is 200 mV at 125°C.

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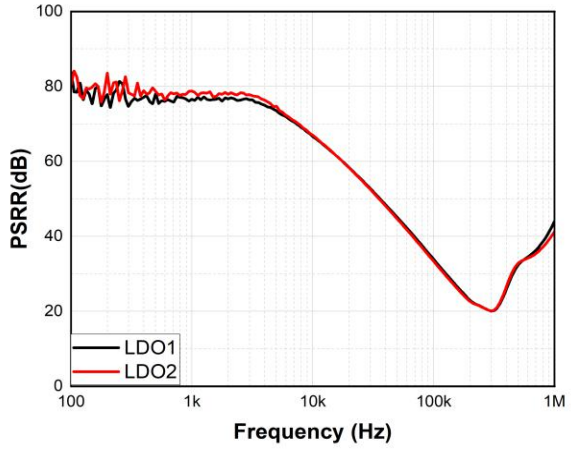
Typical Performance Characteristics



V_{IN12} to V_{OUT}, V_{IN12} = 1.5 V + 0.2 V_{PP},

V_{OUT} = 1.2 V, I_L = 150 mA, C_{OUT} = 4.7 uF

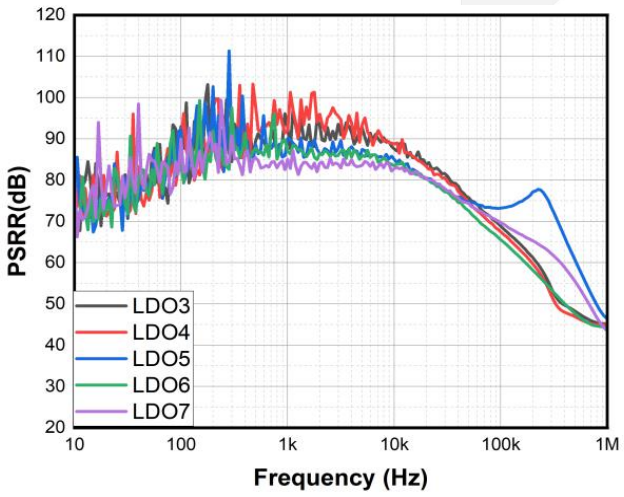
Figure 4. PSRR vs Frequency



V_{SYS} to $V_{OUT1,2}$, V_{SYS} = 3.8 V + 0.2 V_{PP}, $V_{OUT1,2}$ = 1.2 V,

I_L = 150 mA, C_{OUT} = 4.7 uF

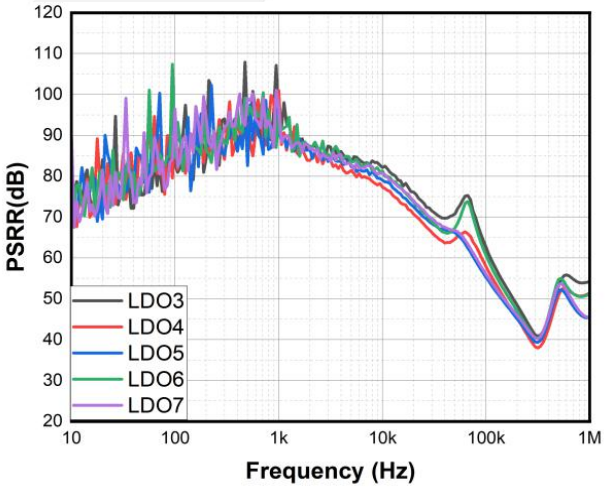
Figure 5. PSRR vs Frequency



$V_{IN3,4,5,6,7}$ to V_{OUT}, $V_{IN3,4,5,6,7}$ = 3.6 V + 0.2 V_{PP}, V_{OUT} = 2.8 V,

I_L = 100 mA, C_{OUT} = 2.2 uF

Figure 6. PSRR vs Frequency



V_{SYS} to $V_{OUT3,4,5,6,7}$, V_{SYS} = 3.8 V + 0.2 V_{PP}, $V_{OUT3,4,5,6,7}$ = 2.8 V,

I_L = 100 mA, C_{OUT} = 2.2 uF

Figure 7. PSRR vs Frequency

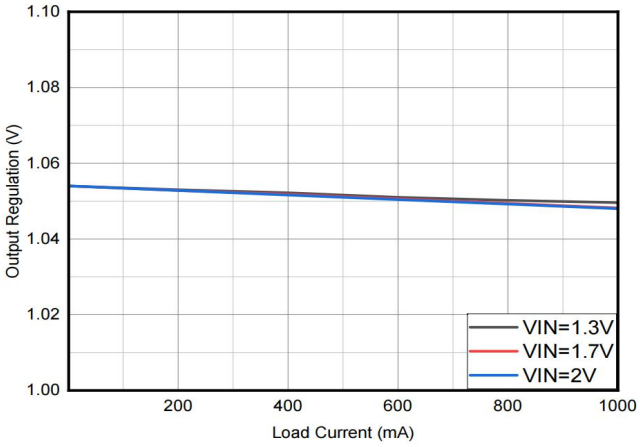


Figure 8. LDO1,2 Output Regulation vs. Load Current input Voltage, V_{OUT} = 1.05 V

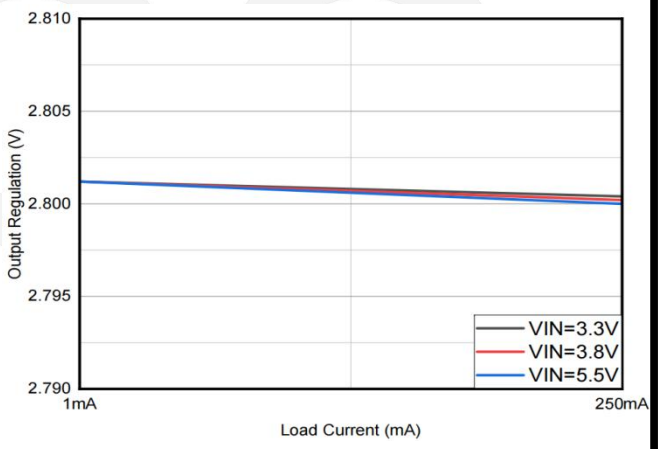


Figure 9. LDO3,4,6 Output Regulation vs. Load Current Input Voltage, V_{OUT} = 2.8 V

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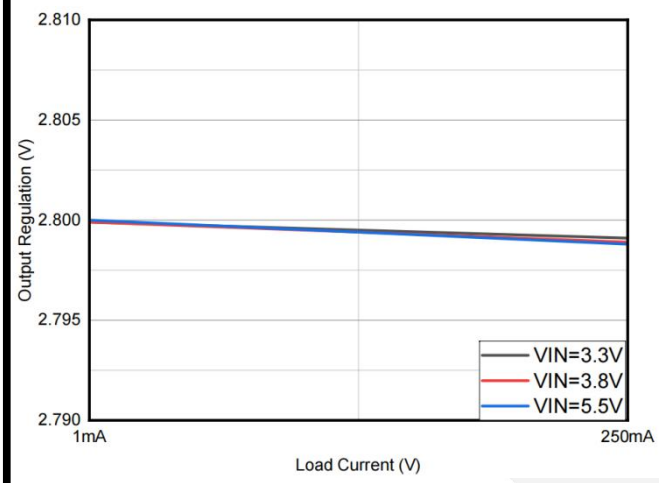


Figure 10. LDO5,7 Output Regulation vs. Load Current Input Voltage, V_{OUT} = 2.8 V

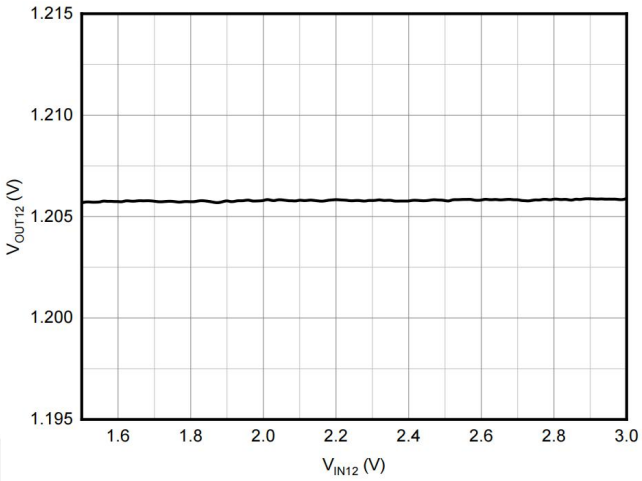


Figure 11. LDO1,2 Output Regulation vs. Input Voltage

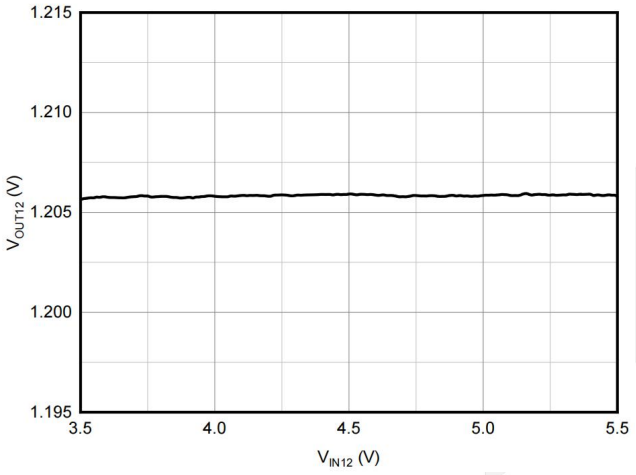


Figure 12. LDO1,2 Output Regulation vs. System Input Voltage

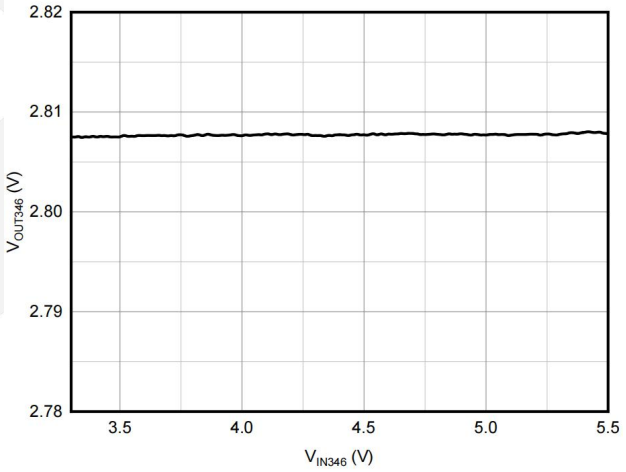


Figure 13. LDO3,4,6 Output Regulation vs. Input Voltage

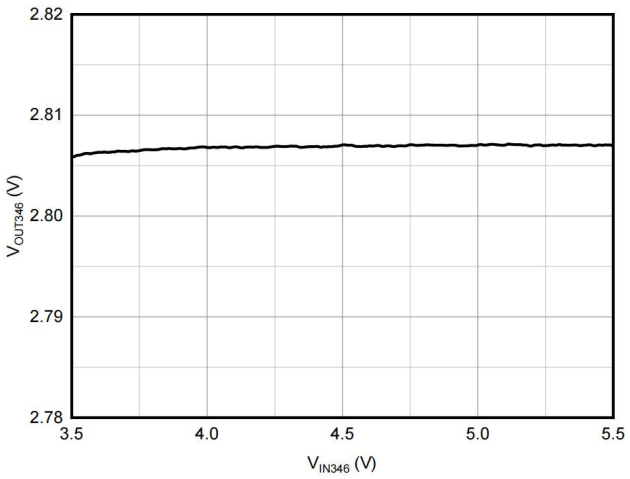


Figure 14. LDO3,4,6 Output Regulation vs. System Input Voltage

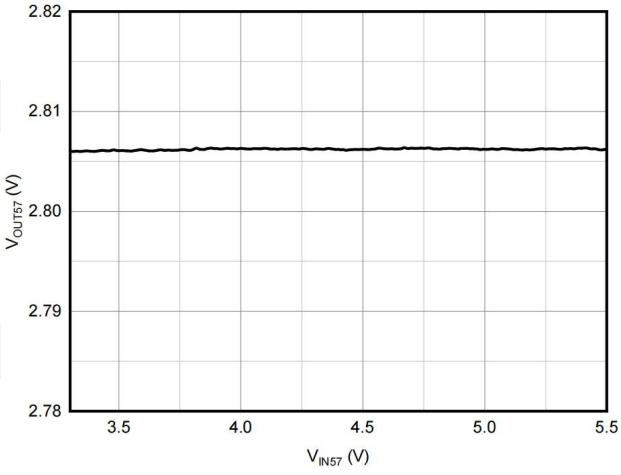


Figure 15. LDO5,7 Output Regulation vs. Input Voltage

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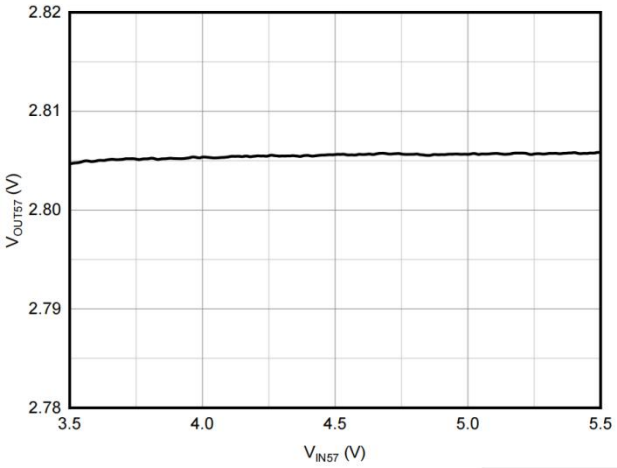


Figure 16. LDO5,7 Output Regulation vs. System Input Voltage

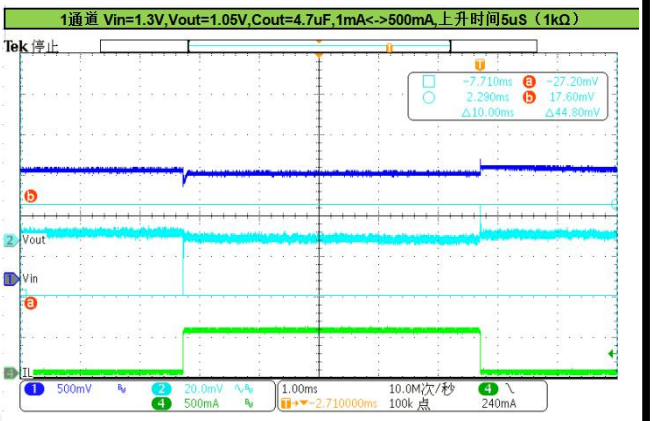


Figure 17. LDO1,2 Load Transient

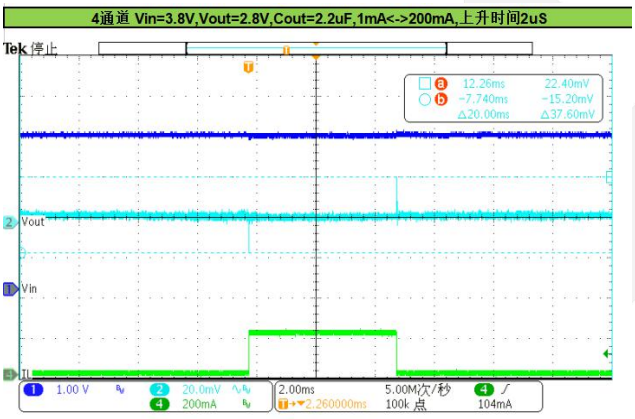


Figure 18. LDO3,4,6 Load Transient

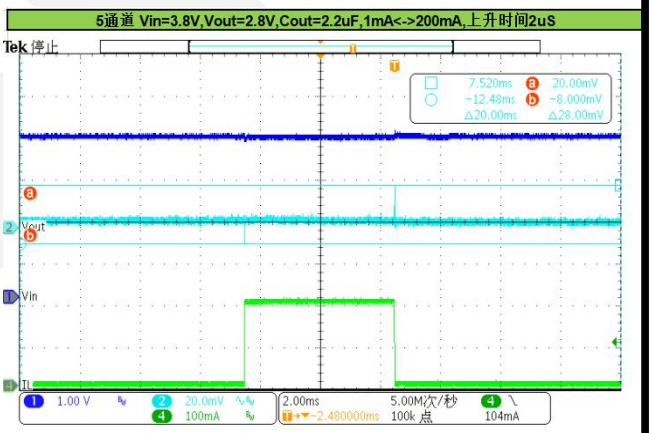


Figure 19. LDO5,7 Load Transient

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Detailed Description

Overview

The DIO8018 micro Power Management IC (PMIC) is desirable for different sub-systems of battery-powered mobile applications. The PMIC includes seven low−dropout regulators: two high current LDOs, three ultra-low noise/high PSRR LDOs, and two LDOs for general purposes. The features of the device can be programmed through an I²C interface.

Under-Voltage Lockout (UVLO)

When the RESET_B pin is pulled high, the assigned UVLO interrupt bit and UVLO status bit will be set in two conditions:

- The voltage of VSYS is higher than the power-on reset (POR) voltage but lower than VSYS UVLO rising threshold.
- The voltage of LDO VINs are lower than their UVLO rising threshold.

Meanwhile, the INT pin will be asserted high. The UVLO status bit remains set as long as the input voltage is below its UVLO rising threshold. The interrupt bit remains set to “1” unless the interrupt bit register is cleared manually.

When the voltage of VSYS or VINs fall below their UVLO falling threshold, one or more LDOs will be shut down, causing a UVLO interrupt. The UVLO status bit will not change until the input voltage rises above its UVLO rising threshold, and then one or more LDOs start up immediately.

As soon as the LDO is shut down, the suspend bits will be set. The LDOs will remain in the shutdown state for at least 20 ms and will try to restart if VSYS or VINs have risen above their UVLO rising threshold. The suspend bits are cleared as soon as the LDO restarts. The LDOs will be disabled permanently after the 4th UVLO fault.

Thermal Management

When the die temperature reaches a nominal 115°C, the Thermal Warning status bit will be set to “1” and will not change until the die temperature drops to a nominal 100°C.

When the die temperature reaches a nominal 155°C, a Thermal Shutdown event occurs, all LDOs are disabled, and the Thermal Shutdown interrupt bit is set but I²C communication continues. As long as the device is above the Thermal Warning temperature, the Thermal Shutdown status bit is also set and will remain unchanged. The chip suspend bit is set as soon as the LDO is shut down.

The Thermal Shutdown status and chip suspend bits will be cleared when the die temperature falls below the Thermal Warning threshold. And then the device will return to the operating conditions before the thermal shutdown event happens.

Enabling/Disabling

By setting the LDOx_EN bits in the ENABLE register, the DIO8018 LDOs can be enabled and disabled independently .

To enable DIO8018 LDOs, pull the RESET_B pin high and set the LDOx_EN bits to “1”. The DIO8018 LDOs have an internal soft−start that can limit the inrush current to the ILIM setting. During the first 1.5 ms at startup,

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the LDOs will ignore faults. After 1.5 ms, if the LDO output does not reach the UVP rising threshold, the device will announce a UVP fault.

Reset the LDOx_EN bits to “0” to disable the DIO8018 LDOs. The active discharge feature is enabled by default. When the LDOx_EN bits are set to “0”, a 100 Ω resistor is connected between VOUT and GND to discharge the output capacitors.

To shut down all LDOs, set the RESET_B pin low.

Over-Current Protection (OCP)

The current limit level can be set by using the I^2C interface to protect the LDOs from excessive load and short-circuit.

When an over-load event occurs, the current is automatically limited to the pre-set current limit. The detection of the current limit will set the associated OCP status bit. If the LDO remains in current limit for more than 1 ms (use the I^2C to set the OCP debounce timer), the OCP interrupt bit will be set and the INT pin will be pulled high. Then the LDO will shut down permanently and will not attempt any restart; meanwhile, the associated suspend bit is set and the status bit is cleared.

Under Voltage Protection (UVP)

The associated UVP status bit and the UVP interrupt bit will be set if the output voltage falls around 20% (10% for LDO1,2) below the target VOUT for more than 100 μs. The INT pin will be pulled high at the same time. The LDO will then be disabled, the associated status bit is cleared and the suspend bit is set. The interrupt bit will be cleared upon a read of the bit.

4-Fault Shutdown

The LDO will be shut down permanently when the device detected 4 failures to prevent repetitive starting and faulting of an LDO or of the IC itself. The entire IC will be shut down permanently if it is a system fault.

Individual LDO Fault: the LDO will be latched off after the 4th individual LDO fault (any combination of UVP, OCP, and VINx UVLO events) and the LDOx_EN bits will be cleared. Set the LDOx_EN bits to “1” to clear the latch-off and re-enable the LDOs, .

Chip Fault: all the LDOs will be latched off after the 4th chip fault (any combination of Thermal Shutdown and VSYS UVLO events) with all the LDOx_EN bits cleared. Pull the RESET_B pin low to clear the latch−off.

Reset

There are two ways to reset the IC. The first way is when the RESET_B pin is low, all registers will be reset to default values. All fault counters will be reset to 0. The second way is to write a “1011” to bit [7:4] in the RESET register to reset all the I^2C registers to their default values.

Power Up/Down Sequence

To program and control the power-up and power-down sequences, use the dedicated registers xxxx_SEQ and SEQUENCING.

If one or more LDOs have faults during a start−up sequence, the other LDOs will still start up in their assigned

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time slot. The xxxx_SEQ register bits for the faulted LDO will remain unchanged to the previous values. The system can then attempt to start the faulted LDO in another sequence by setting the SEQ_CONTROL bits to “01” or by clearing the xxxx_SEQ bits to “000” and writing a “1” to the enable bit for the faulted LDO.

No Fault Shutdown

The No Fault Shutdown feature prevents LDOs from shutting down during an OCP or UVP event. Set the FLT_SD_B bit in the RESET register to “1” to activate the feature, but this practice will not stop the LDOs from shutting down during an LDO VIN UVLO event. When FLT_SD_B = 1 and LDO VIN UVLO, OCP or OVP event occurs, the interrupt and status bits will still indicate the occurrence of faults, but the fault counter will not be incremented.

I²C Interface

The DIO8018 serial interface is compatible with Standard, Fast, and Fast Plus Mode I²C Bus specifications. The SCL line is an input and its SDA line is a bi−directional open−drain output. The SDA line only pulls low during data reads and when signaling ACK. All data is shifted in most significant bit (MSB, bit 7) first.

I²C Slave Address

Table 1 shows the default I²C slave address. The LSB of the address byte is used as the read/write bit and is not included in the 7-bit Hex, Decimal, or Binary value as shown in Table 1. Table 2 shows the location of the R/W bit. Set the I²C address by using the I²C_ADDR_SEL register.

Device	Hex	Decimal	7 bit Binary
DIO8018	35h	53d	011 0101

Table 1. I²C Slave address

7	6	5	4	3	2	1	0
0	1	1	0	1	0	1	R/W

Table 2. I²C (7 bit) Slave address byte

Bus Timing

Figure 20 shows that data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL so as to make enough time for the data to set up before the next SCL rising edge.

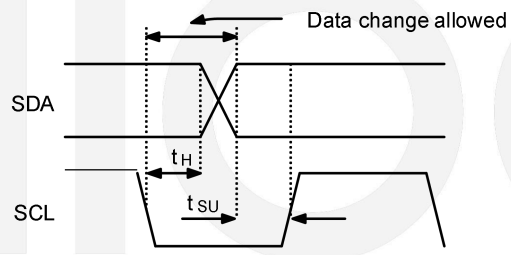


Figure 20. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition. A START condition is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 21.

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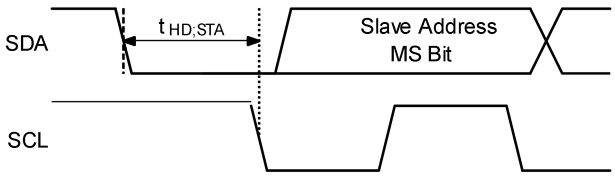


Figure 21. Data Transfer on I²C Serial Bus

Transactions end with a STOP condition. A STOP condition is defined as SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 22.

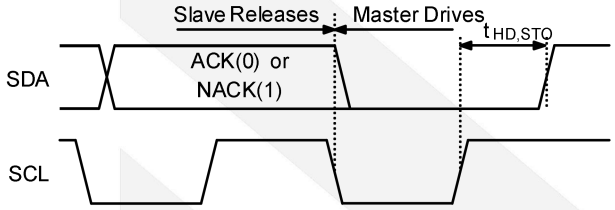


Figure 22. Stop Bit

During a read from the DIO8018, the master sends a Repeated Start after sending the register address and before resending the slave address. The Repeated Start is a 1−to−0 transition on SDA while SCL is HIGH, as shown in Figure 23.

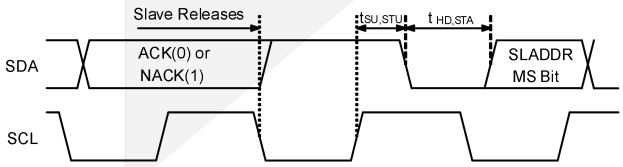


Figure 23. Repeated Start Timing

Read and Write Transactions

The figures 24 to 27 outline the sequences for data read and write. The shading of the packet signifies the bus control, which is defined as “Master Drives Bus” and “Slave Drives Bus”. All addresses and data are MSB first.

Multi−Byte (Sequential) Write Transactions (Figure 26)

Reg Addr address is the Slave Address. The first data byte are transmitted to the DIO8018 in the same way as in a single−byte write (Figure 24). However, instead of generating a Stop condition, the master transmits additional bytes that are written to consecutive sequential registers after the falling edge of the eighth bit. After the last byte is written and its ACK bit is received, the master sends a STOP bit. The IC contains an 8−bit counter that increments the address pointer after each byte is written.

Multi−Byte (Sequential) Read Transactions (Figure 27)

Sequential reads are initiated in the same way as a single-byte read (Figure 25). But as soon as the slave transmits the first data byte, the master sends an acknowledge instead of stopping the process. The acknowledgement directs I²C logic of the slave to transmit the next sequentially addressed 8-bit word. Each time a byte is read, the 8-bit counter in the DIO8018 increments the address pointer, making it possible to read the entire memory contents during a single I²C transaction.

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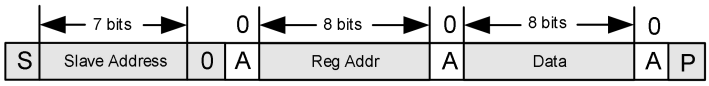


Figure 24. Single−Byte Write Transaction

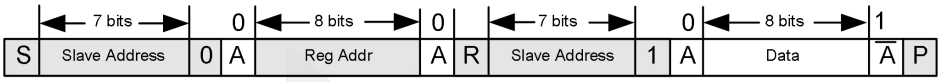


Figure 25. Single−Byte Read Transaction

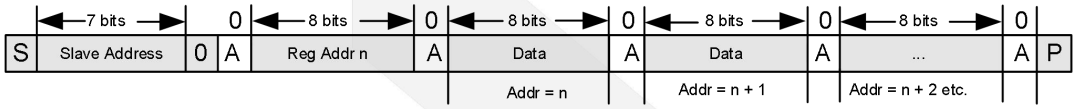


Figure 26. Multi−Byte (Sequential) Write Transaction

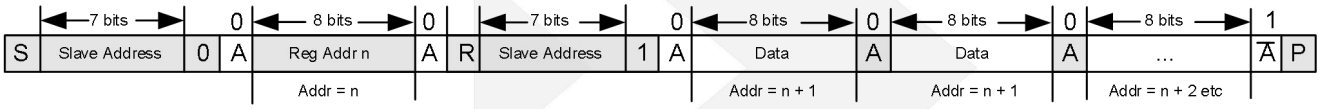


Figure 27. Multi−Byte (Sequential) Read Transaction

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Register Maps

ADDR	Register Name	Type	Default	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x00	PRODUCT ID	R	04	Device ID							
0x01	SILICON REV ID	R	01	Revision							
0x02	IOUT	R/W	53	0	LDO7_ ILIM	LDO6_ ILIM	LDO5_ ILIM	LDO4_ ILIM	LDO3_ ILIM	LDO2_ ILIM	LDO1_ ILIM
0x03	ENABLE	R/W	80	VSYS_ EN	LDO7_ EN	LDO6_ EN	LDO5_ EN	LDO4_ EN	LDO3_ EN	LDO2_ EN	LDO1_ EN
0x04	LDO1	R/W	95	LDO1_VOUT							
0x05	LDO2	R/W	95	LDO2_VOUT							
0x06	LDO3	R/W	B3	LDO3_VOUT							
0x07	LDO4	R/W	B3	LDO4_VOUT							
0x08	LDO5	R/W	B3	LDO5_VOUT							
0x09	LDO6	R/W	B3	LDO6_VOUT							
0x0A	LDO7	R/W	B3	LDO7_VOUT							
0x0B	LDO12_SEQ	R/W	00	0				LDO2_SEQ			LDO1_SEQ
0x0C	LDO34_SEQ	R/W	00	0				LDO4_SEQ			LDO3_SEQ
0x0D	LDO56_SEQ	R/W	00	0				LDO6_SEQ			LDO5_SEQ
0x0E	LDO7_SEQ	R/W	00	0				LDO7_SEQ			
0x0F	SEQUENCING	R/W	00	SEQ_SPEED		SEQ_CONTROL		SEQ_ ON		SEQ_COUNT	
0x10	DISCHARGE	R/W	7F	0	LDO1_ DIS	LDO2_ DIS	LDO3_ DIS	LDO4_ DIS	LDO5_ DIS	LDO6_ DIS	LDO7_ DIS

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0x11	**RESET**	R/W	**06**	**SOFT_RESET**		**0**		**OCP_TIMER**		**FLT_ SD_B**	
0x12	**I²C_ADDR**	R/W	**81**	**INT_LEVEL_SEL**		**INT_OutMode_SEL**		**0**		**I²C_ADDR_SEL**	
0x13	**RESERVED**	R/W	**00**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
0x14	**RESERVED**	R/W	**00**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
0x15	**INTERRUPT1**	R/C	**00**	**0**	**LDO7_UVP_INT**	**LDO6_UVP_INT**	**LDO5_UVP_INT**	**LDO4_UVP_INT**	**LDO3_UVP_INT**	**LDO2_UVP_INT**	**LDO1_UVP_INT**
0x16	**INTERRUPT2**	R/C	**00**	**0**	**LDO7_OCP_INT**	**LDO6_OCP_INT**	**LDO5_OCP_INT**	**LDO4_OCP_INT**	**LDO3_OCP_INT**	**LDO2_OCP_INT**	**LDO1_OCP_INT**
0x17	**INTERRUPT3**	R/C	**00**	**TSD_INT**	**TSD_WRN_INT**	**VSYS_UVLO_INT**	**LDO7_UVLO_INT**	**LDO6_UVLO_INT**	**LDO5_UVLO_INT**	**LDO34_UVLO_INT**	**LDO12_UVLO_INT**
0x18	**STATUS1**	R	**00**	**0**	**LDO7_UVP_STAT**	**LDO6_UVP_STAT**	**LDO5_UVP_STAT**	**LDO4_UVP_STAT**	**LDO3_UVP_STAT**	**LDO2_UVP_STAT**	**LDO1_UVP_STAT**
0x19	**STATUS2**	R	**00**	**0**	**LDO7_OCP_STAT**	**LDO6_OCP_STAT**	**LDO5_OCP_STAT**	**LDO4_OCP_STAT**	**LDO3_OCP_STAT**	**LDO2_OCP_STAT**	**LDO1_OCP_STAT**
0x1A	**STATUS3**	R	**00**	**TSD_STAT**	**TSD_WRN_STAT**	**VSYS_UVLO_STAT**	**LDO7_UVLO_STAT**	**LDO6_UVLO_STAT**	**LDO5_UVLO_STAT**	**LDO34_UVLO_STAT**	**LDO12_UVLO_STAT**
0x1B	**STATUS4**	R	**00**	**CHIP_SUSD**	**LDO7_SUSD**	**LDO6_SUSD**	**LDO5_SUSD**	**LDO4_SUSD**	**LDO3_SUSD**	**LDO2_SUSD**	**LDO1_SUSD**
0x1C	**MINT1**	R/W	**00**	**0**	**MASK_LDO7_UVP**	**MASK_LDO6_UVP**	**MASK_LDO5_UVP**	**MASK_LDO4_UVP**	**MASK_LDO3_UVP**	**MASK_LDO2_UVP**	**MASK_LDO1_UVP**
0x1D	**MINT2**	R/W	**00**	**0**	**MASK_LDO7_OCP**	**MASK_LDO6_OCP**	**MASK_LDO5_OCP**	**MASK_LDO4_OCP**	**MASK_LDO3_OCP**	**MASK_LDO2_OCP**	**MASK_LDO1_OCP**
0x1E	**MINT3**	R/W	**00**	**MASK_TSD**	**MASK_TSD_WRN**	**MASK_VSYS_UVLO**	**MASK_LDO7_UVLO**	**MASK_LDO6_UVLO**	**MASK_LDO5_UVLO**	**MASK_LDO34_UVLO**	**MASK_LDO12_UVLO**

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REGISTER DETAILS – 0x00 PRODUCT ID

Default = 00000100

Bits	Name	Default	Type	Description	
7:0	Product ID	0000 0100	Read	Identifies vendor and device type	
				Code	**Product**
				00000100	DIO8018

REGISTER DETAILS – 0x01 SILICON REV ID

Default = 00000001

Bits	Name	Default	Type	Description
7:0	Revision	0000 0001	Read	Identifies silicon revision

REGISTER DETAILS – 0x02 IOUT

Default = 01010011

Bits	Name	Default	Type	Description	
7	UNUSED	0	R/W		
6	LDO7_ILIM	1	R/W	**Code**	**Current Limit**
				0	650 mA
				1	950 mA
5	LDO6_ILIM	0	R/W	**Code**	**Current Limit**
				0	450 mA
				1	650 mA
4	LDO5_ILIM	1	R/W	**Code**	**Current Limit**
				0	650 mA
				1	950 mA
3	LDO4_ILIM	0	R/W	**Code**	**Current Limit**
				0	450 mA
				1	650 mA
2	LDO3_ILIM	0	R/W	**Code**	**Current Limit**
				0	450 mA
				1	650 mA
1	LDO2_ILIM	1	R/W	**Code**	**Current Limit**
				0	1300 mA
				1	1800 mA
0	LDO1_ILIM	1	R/W	**Code**	**Current Limit**
				0	1300 mA
				1	1800 mA

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REGISTER DETAILS – 0x03 ENABLE

Default = 10000000

Bits	Name	Default	Type	Description	
7	VSYS_EN	1	R/W	Enable bit for system. The system bias will be getting ready for enabling individual LDO if bit7 = 1 and RESET_N is pulled high.	
				Code	**Status of SYS**
				0	Disabled
				1	Enabled
6	LDO7_EN	0	R/W	Enable bit for LDO7. This bit only controls the state of LDO7 if LDO7_SEQ = 000.	
				Code	**Status of LDO**
				0	Disabled
				1	Enabled
5	LDO6_EN	0	R/W	Enable bit for LDO6. This bit only controls the state of LDO6 if LDO6_SEQ = 000.	
				Code	**Status of LDO**
				0	Disabled
				1	Enabled
4	LDO5_EN	0	R/W	Enable bit for LDO5. This bit only controls the state of LDO5 if LDO5_SEQ = 000.	
				Code	**Status of LDO**
				0	Disabled
				1	Enabled
3	LDO4_EN	0	R/W	Enable bit for LDO4. This bit only controls the state of LDO4 if LDO4_SEQ = 000.	
				Code	**Status of LDO**
				0	Disabled
				1	Enabled
2	LDO3_EN	0	R/W	Enable bit for LDO3. This bit only controls the state of LDO3 if LDO3_SEQ = 000.	
				Code	**Status of LDO**
				0	Disabled
				1	Enabled
1	LDO2_EN	0	R/W	Enable bit for LDO2. This bit only controls the state of LDO2 if LDO2_SEQ = 000.	
				Code	**Status of LDO**
				0	Disabled
				1	Enabled
0	LDO1_EN	0	R/W	Enable bit for LDO1. This bit only controls the state of LDO1 if LDO1_SEQ = 000.	
				Code	**Status of LDO**
				0	Disabled
				1	Enabled

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REGISTER DETAILS – 0x04 LDO1

Default = 10010101

Bits	Name	Size	Type	Description
7:0	LDO1_ VOUT	0000 0000	R/W	Sets LDO1 regulation target voltage. Equation: V_{OUT} = 0.800 V + [(d − 99) x 8 mV], where d is the decimal value of the register.

Hex	VOUT	Hex	VOUT	Hex	VOUT	Hex	VOUT
00	Reserved	40	0.520 V	80	1.032 V	C0	Reserved
01	Reserved	41	0.528 V	81	1.040 V	C1	Reserved
02	Reserved	42	0.536 V	82	1.048 V	C2	Reserved
03	Reserved	43	0.544 V	83	1.056 V	C3	Reserved
04	Reserved	44	0.552 V	84	1.064 V	C4	Reserved
05	Reserved	45	0.560 V	85	1.072 V	C5	Reserved
06	Reserved	46	0.568 V	86	1.080 V	C6	Reserved
07	Reserved	47	0.576 V	87	1.088 V	C7	Reserved
08	Reserved	48	0.584 V	88	1.096 V	C8	Reserved
09	Reserved	49	0.592 V	89	1.104 V	C9	Reserved
0A	Reserved	4A	0.600 V	8A	1.112 V	CA	Reserved
0B	Reserved	4B	0.608 V	8B	1.120 V	CB	Reserved
0C	Reserved	4C	0.616 V	8C	1.128 V	CC	Reserved
0D	Reserved	4D	0.624 V	8D	1.136 V	CD	Reserved
0E	Reserved	4E	0.632 V	8E	1.144 V	CE	Reserved
0F	Reserved	4F	0.640 V	8F	1.152 V	CF	Reserved
10	Reserved	50	0.648 V	90	1.160 V	D0	Reserved
11	Reserved	51	0.656 V	91	1.168 V	D1	Reserved
12	Reserved	52	0.664 V	92	1.176 V	D2	Reserved
13	Reserved	53	0.672 V	93	1.184 V	D3	Reserved
14	Reserved	54	0.680 V	94	1.192 V	D4	Reserved
15	Reserved	55	0.688 V	**95**	**1.200 V**	D5	Reserved
16	Reserved	56	0.696 V	96	1.208 V	D6	Reserved
17	Reserved	57	0.704 V	97	1.216 V	D7	Reserved
18	Reserved	58	0.712 V	98	1.224 V	D8	Reserved
19	Reserved	59	0.720 V	99	1.232 V	D9	Reserved
1A	Reserved	5A	0.728 V	9A	1.240 V	DA	Reserved
1B	Reserved	5B	0.736 V	9B	1.248 V	DB	Reserved
1C	Reserved	5C	0.744 V	9C	1.256 V	DC	Reserved
1D	Reserved	5D	0.752 V	9D	1.264 V	DD	Reserved

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7:0	LDO1_ VOUT	0000 0000	R/W	1E	Reserved	5E	0.760 V	9E	1.272 V	DE	Reserved
				1F	Reserved	5F	0.768 V	9F	1.280 V	DF	Reserved
				20	Reserved	60	0.776 V	A0	1.288 V	E0	Reserved
				21	Reserved	61	0.784 V	A1	1.296 V	E1	Reserved
				22	Reserved	62	0.792 V	A2	1.304 V	E2	Reserved
				23	Reserved	63	0.800 V	A3	1.312 V	E3	Reserved
				24	Reserved	64	0.808 V	A4	1.320 V	E4	Reserved
				25	Reserved	65	0.816 V	A5	1.328 V	E5	Reserved
				26	Reserved	66	0.824 V	A6	1.336 V	E6	Reserved
				27	Reserved	67	0.832 V	A7	1.344 V	E7	Reserved
				28	Reserved	68	0.840 V	A8	1.352 V	E8	Reserved
				29	Reserved	69	0.848 V	A9	1.360 V	E9	Reserved
				2A	Reserved	6A	0.856 V	AA	1.368 V	EA	Reserved
				2B	Reserved	6B	0.864 V	AB	1.376 V	EB	Reserved
				2C	Reserved	6C	0.872 V	AC	1.384 V	EC	Reserved
				2D	Reserved	6D	0.880 V	AD	1.392 V	ED	Reserved
				2E	Reserved	6E	0.888 V	AE	1.400 V	EE	Reserved
				2F	Reserved	6F	0.896 V	AF	1.408 V	EF	Reserved
				30	Reserved	70	0.904 V	B0	1.416 V	F0	Reserved
				31	Reserved	71	0.912 V	B1	1.424 V	F1	Reserved
				32	Reserved	72	0.920 V	B2	1.432 V	F2	Reserved
				33	Reserved	73	0.928 V	B3	1.440 V	F3	Reserved
				34	Reserved	74	0.936 V	B4	1.448 V	F4	Reserved
				35	Reserved	75	0.944 V	B5	1.456 V	F5	Reserved
				36	Reserved	76	0.952 V	B6	1.464 V	F6	Reserved
				37	Reserved	77	0.960 V	B7	1.472 V	F7	Reserved
				38	Reserved	78	0.968 V	B8	1.480 V	F8	Reserved
				39	Reserved	79	0.976 V	B9	1.488 V	F9	Reserved
				3A	Reserved	7A	0.984 V	BA	1.496 V	FA	Reserved
				3B	Reserved	7B	0.992 V	BB	1.504 V	FB	Reserved
				3C	Reserved	7C	1.000 V	BC	Reserved	FC	Reserved
				3D	Reserved	7D	1.008 V	BD	Reserved	FD	Reserved
				3E	0.504 V	7E	1.016 V	BE	Reserved	FE	Reserved
				3F	0.512 V	7F	1.024 V	BF	Reserved	FF	Reserved

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REGISTER DETAILS – 0x05 LDO2

Default = 10010101

Bits	Name	Default	Type	Description
7:0	LDO2_ VOUT	0000 0000	R/W	Sets LDO2 regulation target voltage. Equation: V_{OUT} = 0.800 V + [(d − 99) x 8 mV], where d is the decimal value of the register.

Hex	VOUT	Hex	VOUT	Hex	VOUT	Hex	VOUT
00	Reserved	40	0.520 V	80	1.032 V	C0	Reserved
01	Reserved	41	0.528 V	81	1.040 V	C1	Reserved
02	Reserved	42	0.536 V	82	1.048 V	C2	Reserved
03	Reserved	43	0.544 V	83	1.056 V	C3	Reserved
04	Reserved	44	0.552 V	84	1.064 V	C4	Reserved
05	Reserved	45	0.560 V	85	1.072 V	C5	Reserved
06	Reserved	46	0.568 V	86	1.080 V	C6	Reserved
07	Reserved	47	0.576 V	87	1.088 V	C7	Reserved
08	Reserved	48	0.584 V	88	1.096 V	C8	Reserved
09	Reserved	49	0.592 V	89	1.104 V	C9	Reserved
0A	Reserved	4A	0.600 V	8A	1.112 V	CA	Reserved
0B	Reserved	4B	0.608 V	8B	1.120 V	CB	Reserved
0C	Reserved	4C	0.616 V	8C	1.128 V	CC	Reserved
0D	Reserved	4D	0.624 V	8D	1.136 V	CD	Reserved
0E	Reserved	4E	0.632 V	8E	1.144 V	CE	Reserved
0F	Reserved	4F	0.640 V	8F	1.152 V	CF	Reserved
10	Reserved	50	0.648 V	90	1.160 V	D0	Reserved
11	Reserved	51	0.656 V	91	1.168 V	D1	Reserved
12	Reserved	52	0.664 V	92	1.176 V	D2	Reserved
13	Reserved	53	0.672 V	93	1.184 V	D3	Reserved
14	Reserved	54	0.680 V	94	1.192 V	D4	Reserved
15	Reserved	55	0.688 V	**95**	**1.200 V**	D5	Reserved
16	Reserved	56	0.696 V	96	1.208 V	D6	Reserved
17	Reserved	57	0.704 V	97	1.216 V	D7	Reserved
18	Reserved	58	0.712 V	98	1.224 V	D8	Reserved
19	Reserved	59	0.720 V	99	1.232 V	D9	Reserved
1A	Reserved	5A	0.728 V	9A	1.240 V	DA	Reserved
1B	Reserved	5B	0.736 V	9B	1.248 V	DB	Reserved
1C	Reserved	5C	0.744 V	9C	1.256 V	DC	Reserved
1D	Reserved	5D	0.752 V	9D	1.264 V	DD	Reserved

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7:0	LDO2_ VOUT	0000 0000	R/W	1E	Reserved	5E	0.760 V	9E	1.272 V	DE	Reserved
				1F	Reserved	5F	0.768 V	9F	1.280 V	DF	Reserved
				20	Reserved	60	0.776 V	A0	1.288 V	E0	Reserved
				21	Reserved	61	0.784 V	A1	1.296 V	E1	Reserved
				22	Reserved	62	0.792 V	A2	1.304 V	E2	Reserved
				23	Reserved	63	0.800 V	A3	1.312 V	E3	Reserved
				24	Reserved	64	0.808 V	A4	1.320 V	E4	Reserved
				25	Reserved	65	0.816 V	A5	1.328 V	E5	Reserved
				26	Reserved	66	0.824 V	A6	1.336 V	E6	Reserved
				27	Reserved	67	0.832 V	A7	1.344 V	E7	Reserved
				28	Reserved	68	0.840 V	A8	1.352 V	E8	Reserved
				29	Reserved	69	0.848 V	A9	1.360 V	E9	Reserved
				2A	Reserved	6A	0.856 V	AA	1.368 V	EA	Reserved
				2B	Reserved	6B	0.864 V	AB	1.376 V	EB	Reserved
				2C	Reserved	6C	0.872 V	AC	1.384 V	EC	Reserved
				2D	Reserved	6D	0.880 V	AD	1.392 V	ED	Reserved
				2E	Reserved	6E	0.888 V	AE	1.400 V	EE	Reserved
				2F	Reserved	6F	0.896 V	AF	1.408 V	EF	Reserved
				30	Reserved	70	0.904 V	B0	1.416 V	F0	Reserved
				31	Reserved	71	0.912 V	B1	1.424 V	F1	Reserved
				32	Reserved	72	0.920 V	B2	1.432 V	F2	Reserved
				33	Reserved	73	0.928 V	B3	1.440 V	F3	Reserved
				34	Reserved	74	0.936 V	B4	1.448 V	F4	Reserved
				35	Reserved	75	0.944 V	B5	1.456 V	F5	Reserved
				36	Reserved	76	0.952 V	B6	1.464 V	F6	Reserved
				37	Reserved	77	0.960 V	B7	1.472 V	F7	Reserved
				38	Reserved	78	0.968 V	B8	1.480 V	F8	Reserved
				39	Reserved	79	0.976 V	B9	1.488 V	F9	Reserved
				3A	Reserved	7A	0.984 V	BA	1.496 V	FA	Reserved
				3B	Reserved	7B	0.992 V	BB	1.504 V	FB	Reserved
				3C	Reserved	7C	1.000 V	BC	Reserved	FC	Reserved
				3D	Reserved	7D	1.008 V	BD	Reserved	FD	Reserved
				3E	0.504 V	7E	1.016 V	BE	Reserved	FE	Reserved
				3F	0.512 V	7F	1.024 V	BF	Reserved	FF	Reserved

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REGISTER DETAILS – 0x06 LDO3

Default = 10110011

Bits	Name	Default	Type	Description
7:0	LDO3_ VOUT	0000 0000	R/W	Sets LDO3 regulation target voltage. Equation: V_{OUT} = 1.500 V + [(d − 16) x 8 mV], where d is the decimal value of the register.

Hex	VOUT	Hex	VOUT	Hex	VOUT	Hex	VOUT
0	Reserved	40	1.884 V	80	2.396 V	C0	2.908 V
1	Reserved	41	1.892 V	81	2.404 V	C1	2.916 V
2	Reserved	42	1.900 V	82	2.412 V	C2	2.924 V
3	Reserved	43	1.908 V	83	2.420 V	C3	2.932 V
4	Reserved	44	1.916 V	84	2.428 V	C4	2.940 V
5	Reserved	45	1.924 V	85	2.436 V	C5	2.948 V
6	Reserved	46	1.932 V	86	2.444 V	C6	2.956 V
7	Reserved	47	1.940 V	87	2.452 V	C7	2.964 V
8	Reserved	48	1.948 V	88	2.460 V	C8	2.972 V
9	Reserved	49	1.956 V	89	2.468 V	C9	2.980 V
0A	Reserved	4A	1.964 V	8A	2.476 V	CA	2.988 V
0B	Reserved	4B	1.972 V	8B	2.484 V	CB	2.996 V
0C	Reserved	4C	1.980 V	8C	2.492 V	CC	3.004 V
0D	Reserved	4D	1.988 V	8D	2.500 V	CD	3.012 V
0E	Reserved	4E	1.996 V	8E	2.508 V	CE	3.020 V
0F	Reserved	4F	2.004 V	8F	2.516 V	CF	3.028 V
10	1.500 V	50	2.012 V	90	2.524 V	D0	3.036 V
11	1.508 V	51	2.020 V	91	2.532 V	D1	3.044 V
12	1.516 V	52	2.028 V	92	2.540 V	D2	3.052 V
13	1.524 V	53	2.036 V	93	2.548 V	D3	3.060 V
14	1.532 V	54	2.044 V	94	2.556 V	D4	3.068 V
15	1.540 V	55	2.052 V	95	2.564 V	D5	3.076 V
16	1.548 V	56	2.060 V	96	2.572 V	D6	3.084 V
17	1.556 V	57	2.068 V	97	2.580 V	D7	3.092 V
18	1.564 V	58	2.076 V	98	2.588 V	D8	3.100 V
19	1.572 V	59	2.084 V	99	2.596 V	D9	3.108 V
1A	1.580 V	5A	2.092 V	9A	2.604 V	DA	3.116 V
1B	1.588 V	5B	2.100 V	9B	2.612 V	DB	3.124 V
1C	1.596 V	5C	2.108 V	9C	2.620 V	DC	3.132 V
1D	1.604 V	5D	2.116 V	9D	2.628 V	DD	3.140 V

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7:0	LDO3_ VOUT	0000 0000	R/W	1E	1.612 V	5E	2.124 V	9E	2.636 V	DE	3.148 V
				1F	1.620 V	5F	2.132 V	9F	2.644 V	DF	3.156 V
				20	1.628 V	60	2.140 V	A0	2.652 V	E0	3.164 V
				21	1.636 V	61	2.148 V	A1	2.660 V	E1	3.172 V
				22	1.644 V	62	2.156 V	A2	2.668 V	E2	3.180 V
				23	1.652 V	63	2.164 V	A3	2.676 V	E3	3.188 V
				24	1.660 V	64	2.172 V	A4	2.684 V	E4	3.196 V
				25	1.668 V	65	2.180 V	A5	2.692 V	E5	3.204 V
				26	1.676 V	66	2.188 V	A6	2.700 V	E6	3.212 V
				27	1.684 V	67	2.196 V	A7	2.708 V	E7	3.220 V
				28	1.692 V	68	2.204 V	A8	2.716 V	E8	3.228 V
				29	1.700 V	69	2.212 V	A9	2.724 V	E9	3.236 V
				2A	1.708 V	6A	2.220 V	AA	2.732 V	EA	3.244 V
				2B	1.716 V	6B	2.228 V	AB	2.740 V	EB	3.252 V
				2C	1.724 V	6C	2.236 V	AC	2.748 V	EC	3.260 V
				2D	1.732 V	6D	2.244 V	AD	2.756 V	ED	3.268 V
				2E	1.740 V	6E	2.252 V	AE	2.764 V	EE	3.276 V
				2F	1.748 V	6F	2.260 V	AF	2.772 V	EF	3.284 V
				30	1.756 V	70	2.268 V	B0	2.780 V	F0	3.292 V
				31	1.764 V	71	2.276 V	B1	2.788 V	F1	3.300 V
				32	1.772 V	72	2.284 V	B2	2.796 V	F2	3.308 V
				33	1.780 V	73	2.292 V	**B3**	**2.804 V**	F3	3.316 V
				34	1.788 V	74	2.300 V	B4	2.812 V	F4	3.324 V
				35	1.796 V	75	2.308 V	B5	2.820 V	F5	3.332 V
				36	1.804 V	76	2.316 V	B6	2.828 V	F6	3.340 V
				37	1.812 V	77	2.324 V	B7	2.836 V	F7	3.348 V
				38	1.820 V	78	2.332 V	B8	2.844 V	F8	3.356 V
				39	1.828 V	79	2.340 V	B9	2.852 V	F9	3.364 V
				3A	1.836 V	7A	2.348 V	BA	2.860 V	FA	3.372 V
				3B	1.844 V	7B	2.356 V	BB	2.868 V	FB	3.380 V
				3C	1.852 V	7C	2.364 V	BC	2.876 V	FC	3.388 V
				3D	1.860 V	7D	2.372 V	BD	2.884 V	FD	3.396 V
				3E	1.868 V	7E	2.380 V	BE	2.892 V	FE	3.404 V
				3F	1.876 V	7F	2.388 V	BF	2.900 V	FF	3.412 V

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REGISTER DETAILS – 0x07 LDO4

Default = 10110011

Bits	Name	Default	Type	Description
7:0	LDO4_ VOUT	0000 0000	R/W	Sets LDO4 regulation target voltage. Equation: V_{OUT} = 1.500 V + [(d − 16) x 8 mV], where d is the decimal value of the register.

Hex	VOUT	Hex	VOUT	Hex	VOUT	Hex	VOUT
0	Reserved	40	1.884 V	80	2.396 V	C0	2.908 V
1	Reserved	41	1.892 V	81	2.404 V	C1	2.916 V
2	Reserved	42	1.900 V	82	2.412 V	C2	2.924 V
3	Reserved	43	1.908 V	83	2.420 V	C3	2.932 V
4	Reserved	44	1.916 V	84	2.428 V	C4	2.940 V
5	Reserved	45	1.924 V	85	2.436 V	C5	2.948 V
6	Reserved	46	1.932 V	86	2.444 V	C6	2.956 V
7	Reserved	47	1.940 V	87	2.452 V	C7	2.964 V
8	Reserved	48	1.948 V	88	2.460 V	C8	2.972 V
9	Reserved	49	1.956 V	89	2.468 V	C9	2.980 V
0A	Reserved	4A	1.964 V	8A	2.476 V	CA	2.988 V
0B	Reserved	4B	1.972V	8B	2.484 V	CB	2.996 V
0C	Reserved	4C	1.980 V	8C	2.492 V	CC	3.004 V
0D	Reserved	4D	1.988 V	8D	2.500 V	CD	3.012 V
0E	Reserved	4E	1.996 V	8E	2.508 V	CE	3.020 V
0F	Reserved	4F	2.004 V	8F	2.516 V	CF	3.028 V
10	1.500 V	50	2.012 V	90	2.524 V	D0	3.036 V
11	1.508 V	51	2.020 V	91	2.532 V	D1	3.044 V
12	1.516 V	52	2.028 V	92	2.540 V	D2	3.052 V
13	1.524 V	53	2.036 V	93	2.548 V	D3	3.060 V
14	1.532 V	54	2.044 V	94	2.556 V	D4	3.068 V
15	1.540 V	55	2.052 V	95	2.564 V	D5	3.076 V
16	1.548 V	56	2.060 V	96	2.572 V	D6	3.084 V
17	1.556 V	57	2.068 V	97	2.580 V	D7	3.092 V
18	1.564 V	58	2.076 V	98	2.588 V	D8	3.100 V
19	1.572 V	59	2.084 V	99	2.596 V	D9	3.108 V
1A	1.580 V	5A	2.092 V	9A	2.604 V	DA	3.116 V
1B	1.588 V	5B	2.100 V	9B	2.612 V	DB	3.124 V
1C	1.596 V	5C	2.108 V	9C	2.620 V	DC	3.132 V
1D	1.604 V	5D	2.116 V	9D	2.628 V	DD	3.140 V

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7:0	LDO4_ VOUT	0000 0000	R/W	1E	1.612 V	5E	2.124 V	9E	2.636 V	DE	3.148 V
				1F	1.620 V	5F	2.132 V	9F	2.644 V	DF	3.156 V
				20	1.628 V	60	2.140 V	A0	2.652 V	E0	3.164 V
				21	1.636 V	61	2.148 V	A1	2.660 V	E1	3.172 V
				22	1.644 V	62	2.156 V	A2	2.668 V	E2	3.180 V
				23	1.652 V	63	2.164 V	A3	2.676 V	E3	3.188 V
				24	1.660 V	64	2.172 V	A4	2.684 V	E4	3.196 V
				25	1.668 V	65	2.180 V	A5	2.692 V	E5	3.204 V
				26	1.676 V	66	2.188 V	A6	2.700 V	E6	3.212 V
				27	1.684 V	67	2.196 V	A7	2.708 V	E7	3.220 V
				28	1.692 V	68	2.204 V	A8	2.716 V	E8	3.228 V
				29	1.700 V	69	2.212 V	A9	2.724 V	E9	3.236 V
				2A	1.708 V	6A	2.220 V	AA	2.732 V	EA	3.244 V
				2B	1.716 V	6B	2.228 V	AB	2.740 V	EB	3.252 V
				2C	1.724 V	6C	2.236 V	AC	2.748 V	EC	3.260 V
				2D	1.732 V	6D	2.244 V	AD	2.756 V	ED	3.268 V
				2E	1.740 V	6E	2.252 V	AE	2.764 V	EE	3.276 V
				2F	1.748 V	6F	2.260 V	AF	2.772 V	EF	3.284 V
				30	1.756 V	70	2.268 V	B0	2.780 V	F0	3.292 V
				31	1.764 V	71	2.276 V	B1	2.788 V	F1	3.300 V
				32	1.772 V	72	2.284 V	B2	2.796 V	F2	3.308 V
				33	1.780 V	73	2.292 V	**B3**	**2.804 V**	F3	3.316 V
				34	1.788 V	74	2.300 V	B4	2.812 V	F4	3.324 V
				35	1.796 V	75	2.308 V	B5	2.820 V	F5	3.332 V
				36	1.804 V	76	2.316 V	B6	2.828 V	F6	3.340 V
				37	1.812 V	77	2.324 V	B7	2.836 V	F7	3.348 V
				38	1.820 V	78	2.332 V	B8	2.844 V	F8	3.356 V
				39	1.828 V	79	2.340 V	B9	2.852 V	F9	3.364 V
				3A	1.836 V	7A	2.348 V	BA	2.860 V	FA	3.372 V
				3B	1.844 V	7B	2.356 V	BB	2.868 V	FB	3.380 V
				3C	1.852 V	7C	2.364 V	BC	2.876 V	FC	3.388 V
				3D	1.860 V	7D	2.372 V	BD	2.884 V	FD	3.396 V
				3E	1.868 V	7E	2.380 V	BE	2.892 V	FE	3.404 V
				3F	1.876 V	7F	2.388 V	BF	2.900 V	FF	3.412 V

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REGISTER DETAILS – 0x08 LDO5

Default = 10110011

Bits	Name	Default	Type	Description
7:0	LDO5_ VOUT	0000 0000	R/W	Sets LDO5 regulation target voltage. Equation: V_{OUT} = 1.500 V + [(d − 16) x 8 mV], where d is the decimal value of the register.

Hex	VOUT	Hex	VOUT	Hex	VOUT	Hex	VOUT
0	Reserved	40	1.884 V	80	2.396 V	C0	2.908 V
1	Reserved	41	1.892 V	81	2.404 V	C1	2.916 V
2	Reserved	42	1.900 V	82	2.412 V	C2	2.924 V
3	Reserved	43	1.908 V	83	2.420 V	C3	2.932 V
4	Reserved	44	1.916 V	84	2.428 V	C4	2.940 V
5	Reserved	45	1.924 V	85	2.436 V	C5	2.948 V
6	Reserved	46	1.932 V	86	2.444 V	C6	2.956 V
7	Reserved	47	1.940 V	87	2.452 V	C7	2.964 V
8	Reserved	48	1.948 V	88	2.460 V	C8	2.972 V
9	Reserved	49	1.956 V	89	2.468 V	C9	2.980 V
0A	Reserved	4A	1.964 V	8A	2.476 V	CA	2.988 V
0B	Reserved	4B	1.972 V	8B	2.484 V	CB	2.996 V
0C	Reserved	4C	1.980 V	8C	2.492 V	CC	3.004 V
0D	Reserved	4D	1.988 V	8D	2.500 V	CD	3.012 V
0E	Reserved	4E	1.996 V	8E	2.508 V	CE	3.020 V
0F	Reserved	4F	2.004 V	8F	2.516 V	CF	3.028 V
10	1.500 V	50	2.012 V	90	2.524 V	D0	3.036 V
11	1.508 V	51	2.020 V	91	2.532 V	D1	3.044 V
12	1.516 V	52	2.028 V	92	2.540 V	D2	3.052 V
13	1.524 V	53	2.036 V	93	2.548 V	D3	3.060 V
14	1.532 V	54	2.044 V	94	2.556 V	D4	3.068 V
15	1.540 V	55	2.052 V	95	2.564 V	D5	3.076 V
16	1.548 V	56	2.060 V	96	2.572 V	D6	3.084 V
17	1.556 V	57	2.068 V	97	2.580 V	D7	3.092 V
18	1.564 V	58	2.076 V	98	2.588 V	D8	3.100 V
19	1.572 V	59	2.084 V	99	2.596 V	D9	3.108 V
1A	1.580 V	5A	2.092 V	9A	2.604 V	DA	3.116 V
1B	1.588 V	5B	2.100 V	9B	2.612 V	DB	3.124 V
1C	1.596 V	5C	2.108 V	9C	2.620 V	DC	3.132 V
1D	1.604 V	5D	2.116 V	9D	2.628 V	DD	3.140 V

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7:0	LDO5_ VOUT	0000 0000	R/W	1E	1.612 V	5E	2.124 V	9E	2.636 V	DE	3.148 V
				1F	1.620 V	5F	2.132 V	9F	2.644 V	DF	3.156 V
				20	1.628 V	60	2.140 V	A0	2.652 V	E0	3.164 V
				21	1.636 V	61	2.148 V	A1	2.660 V	E1	3.172 V
				22	1.644 V	62	2.156 V	A2	2.668 V	E2	3.180 V
				23	1.652 V	63	2.164 V	A3	2.676 V	E3	3.188 V
				24	1.660 V	64	2.172 V	A4	2.684 V	E4	3.196 V
				25	1.668 V	65	2.180 V	A5	2.692 V	E5	3.204 V
				26	1.676 V	66	2.188 V	A6	2.700 V	E6	3.212 V
				27	1.684 V	67	2.196 V	A7	2.708 V	E7	3.220 V
				28	1.692 V	68	2.204 V	A8	2.716 V	E8	3.228 V
				29	1.700 V	69	2.212 V	A9	2.724 V	E9	3.236 V
				2A	1.708 V	6A	2.220 V	AA	2.732 V	EA	3.244 V
				2B	1.716 V	6B	2.228 V	AB	2.740 V	EB	3.252 V
				2C	1.724 V	6C	2.236 V	AC	2.748 V	EC	3.260 V
				2D	1.732 V	6D	2.244 V	AD	2.756 V	ED	3.268 V
				2E	1.740 V	6E	2.252 V	AE	2.764 V	EE	3.276 V
				2F	1.748 V	6F	2.260 V	AF	2.772 V	EF	3.284 V
				30	1.756 V	70	2.268 V	B0	2.780 V	F0	3.292 V
				31	1.764 V	71	2.276 V	B1	2.788 V	F1	3.300 V
				32	1.772 V	72	2.284 V	B2	2.796 V	F2	3.308 V
				33	1.780 V	73	2.292 V	**B3**	**2.804 V**	F3	3.316 V
				34	1.788 V	74	2.300 V	B4	2.812 V	F4	3.324 V
				35	1.796 V	75	2.308 V	B5	2.820 V	F5	3.332 V
				36	1.804 V	76	2.316 V	B6	2.828 V	F6	3.340 V
				37	1.812 V	77	2.324 V	B7	2.836 V	F7	3.348 V
				38	1.820 V	78	2.332 V	B8	2.844 V	F8	3.356 V
				39	1.828 V	79	2.340 V	B9	2.852 V	F9	3.364 V
				3A	1.836 V	7A	2.348 V	BA	2.860 V	FA	3.372 V
				3B	1.844 V	7B	2.356 V	BB	2.868 V	FB	3.380 V
				3C	1.852 V	7C	2.364 V	BC	2.876 V	FC	3.388 V
				3D	1.860 V	7D	2.372 V	BD	2.884 V	FD	3.396 V
				3E	1.868 V	7E	2.380 V	BE	2.892 V	FE	3.404 V
				3F	1.876 V	7F	2.388 V	BF	2.900 V	FF	3.412 V

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REGISTER DETAILS – 0x09 LDO6

Default = 10110011

Bits	Name	Default	Type	Description
7:0	LDO6_ VOUT	0000 0000	R/W	Sets LDO6 regulation target voltage. Equation: V_{OUT} = 1.500 V + [(d − 16) x 8 mV], where d is the decimal value of the register

Hex	VOUT	Hex	VOUT	Hex	VOUT	Hex	VOUT
0	Reserved	40	1.884 V	80	2.396 V	C0	2.908 V
1	Reserved	41	1.892 V	81	2.404 V	C1	2.916 V
2	Reserved	42	1.900 V	82	2.412 V	C2	2.924 V
3	Reserved	43	1.908 V	83	2.420 V	C3	2.932 V
4	Reserved	44	1.916 V	84	2.428 V	C4	2.940 V
5	Reserved	45	1.924 V	85	2.436 V	C5	2.948 V
6	Reserved	46	1.932 V	86	2.444 V	C6	2.956 V
7	Reserved	47	1.940 V	87	2.452 V	C7	2.964 V
8	Reserved	48	1.948 V	88	2.460 V	C8	2.972 V
9	Reserved	49	1.956 V	89	2.468 V	C9	2.980 V
0A	Reserved	4A	1.964 V	8A	2.476 V	CA	2.988 V
0B	Reserved	4B	1.972 V	8B	2.484 V	CB	2.996 V
0C	Reserved	4C	1.980 V	8C	2.492 V	CC	3.004 V
0D	Reserved	4D	1.988 V	8D	2.500 V	CD	3.012 V
0E	Reserved	4E	1.996 V	8E	2.508 V	CE	3.020 V
0F	Reserved	4F	2.004 V	8F	2.516 V	CF	3.028 V
10	1.500 V	50	2.012 V	90	2.524 V	D0	3.036 V
11	1.508 V	51	2.020 V	91	2.532 V	D1	3.044 V
12	1.516 V	52	2.028 V	92	2.540 V	D2	3.052 V
13	1.524 V	53	2.036 V	93	2.548 V	D3	3.060 V
14	1.532 V	54	2.044 V	94	2.556 V	D4	3.068 V
15	1.540 V	55	2.052 V	95	2.564 V	D5	3.076 V
16	1.548 V	56	2.060 V	96	2.572 V	D6	3.084 V
17	1.556 V	57	2.068 V	97	2.580 V	D7	3.092 V
18	1.564 V	58	2.076 V	98	2.588 V	D8	3.100 V
19	1.572 V	59	2.084 V	99	2.596 V	D9	3.108 V
1A	1.580 V	5A	2.092 V	9A	2.604 V	DA	3.116 V
1B	1.588 V	5B	2.100 V	9B	2.612 V	DB	3.124 V
1C	1.596 V	5C	2.108 V	9C	2.620 V	DC	3.132 V
1D	1.604 V	5D	2.116 V	9D	2.628 V	DD	3.140 V

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7:0	LDO6_ VOUT	0000 0000	R/W	1E	1.612 V	5E	2.124 V	9E	2.636 V	DE	3.148 V
				1F	1.620 V	5F	2.132 V	9F	2.644 V	DF	3.156 V
				20	1.628 V	60	2.140 V	A0	2.652 V	E0	3.164 V
				21	1.636 V	61	2.148 V	A1	2.660 V	E1	3.172 V
				22	1.644 V	62	2.156 V	A2	2.668 V	E2	3.180 V
				23	1.652 V	63	2.164 V	A3	2.676 V	E3	3.188 V
				24	1.660 V	64	2.172 V	A4	2.684 V	E4	3.196 V
				25	1.668 V	65	2.180 V	A5	2.692 V	E5	3.204 V
				26	1.676 V	66	2.188 V	A6	2.700 V	E6	3.212 V
				27	1.684 V	67	2.196 V	A7	2.708 V	E7	3.220 V
				28	1.692 V	68	2.204 V	A8	2.716 V	E8	3.228 V
				29	1.700 V	69	2.212 V	A9	2.724 V	E9	3.236 V
				2A	1.708 V	6A	2.220 V	AA	2.732 V	EA	3.244 V
				2B	1.716 V	6B	2.228 V	AB	2.740 V	EB	3.252 V
				2C	1.724 V	6C	2.236 V	AC	2.748 V	EC	3.260 V
				2D	1.732 V	6D	2.244 V	AD	2.756 V	ED	3.268 V
				2E	1.740 V	6E	2.252 V	AE	2.764 V	EE	3.276 V
				2F	1.748 V	6F	2.260 V	AF	2.772 V	EF	3.284 V
				30	1.756 V	70	2.268 V	B0	2.780 V	F0	3.292 V
				31	1.764 V	71	2.276 V	B1	2.788 V	F1	3.300 V
				32	1.772 V	72	2.284 V	B2	2.796 V	F2	3.308 V
				33	1.780 V	73	2.292 V	**B3**	**2.804 V**	F3	3.316 V
				34	1.788 V	74	2.300 V	B4	2.812 V	F4	3.324 V
				35	1.796 V	75	2.308 V	B5	2.820 V	F5	3.332 V
				36	1.804 V	76	2.316 V	B6	2.828 V	F6	3.340 V
				37	1.812 V	77	2.324 V	B7	2.836 V	F7	3.348 V
				38	1.820 V	78	2.332 V	B8	2.844 V	F8	3.356 V
				39	1.828 V	79	2.340 V	B9	2.852 V	F9	3.364 V
				3A	1.836 V	7A	2.348 V	BA	2.860 V	FA	3.372 V
				3B	1.844 V	7B	2.356 V	BB	2.868 V	FB	3.380 V
				3C	1.852 V	7C	2.364 V	BC	2.876 V	FC	3.388 V
				3D	1.860 V	7D	2.372 V	BD	2.884 V	FD	3.396 V
				3E	1.868 V	7E	2.380 V	BE	2.892 V	FE	3.404 V
				3F	1.876 V	7F	2.388 V	BF	2.900 V	FF	3.412 V

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REGISTER DETAILS – 0x0A LDO7

Default = 10110011

Bits	Name	Default	Type	Description
7:0	LDO7_ VOUT	0000 0000	R/W	Sets LDO7 regulation target voltage. Equation: V_{OUT} = 1.500 V + [(d − 16) x 8 mV], where d is the decimal value of the register.

Hex	VOUT	Hex	VOUT	Hex	VOUT	Hex	VOUT
0	Reserved	40	1.884 V	80	2.396 V	C0	2.908 V
1	Reserved	41	1.892 V	81	2.404 V	C1	2.916 V
2	Reserved	42	1.900 V	82	2.412 V	C2	2.924 V
3	Reserved	43	1.908 V	83	2.420 V	C3	2.932 V
4	Reserved	44	1.916 V	84	2.428 V	C4	2.940 V
5	Reserved	45	1.924 V	85	2.436 V	C5	2.948 V
6	Reserved	46	1.932 V	86	2.444 V	C6	2.956 V
7	Reserved	47	1.940 V	87	2.452 V	C7	2.964 V
8	Reserved	48	1.948 V	88	2.460 V	C8	2.972 V
9	Reserved	49	1.956 V	89	2.468 V	C9	2.980 V
0A	Reserved	4A	1.964 V	8A	2.476 V	CA	2.988 V
0B	Reserved	4B	1.972 V	8B	2.484 V	CB	2.996 V
0C	Reserved	4C	1.980 V	8C	2.492 V	CC	3.004 V
0D	Reserved	4D	1.988 V	8D	2.500 V	CD	3.012 V
0E	Reserved	4E	1.996 V	8E	2.508 V	CE	3.020 V
0F	Reserved	4F	2.004 V	8F	2.516 V	CF	3.028 V
10	1.500 V	50	2.012 V	90	2.524 V	D0	3.036 V
11	1.508 V	51	2.020 V	91	2.532 V	D1	3.044 V
12	1.516 V	52	2.028 V	92	2.540 V	D2	3.052 V
13	1.524 V	53	2.036 V	93	2.548 V	D3	3.060 V
14	1.532 V	54	2.044 V	94	2.556 V	D4	3.068 V
15	1.540 V	55	2.052 V	95	2.564 V	D5	3.076 V
16	1.548 V	56	2.060 V	96	2.572 V	D6	3.084 V
17	1.556 V	57	2.068 V	97	2.580 V	D7	3.092 V
18	1.564 V	58	2.076 V	98	2.588 V	D8	3.100 V
19	1.572 V	59	2.084 V	99	2.596 V	D9	3.108 V
1A	1.580 V	5A	2.092 V	9A	2.604 V	DA	3.116 V
1B	1.588 V	5B	2.100 V	9B	2.612 V	DB	3.124 V
1C	1.596 V	5C	2.108 V	9C	2.620 V	DC	3.132 V
1D	1.604 V	5D	2.116 V	9D	2.628 V	DD	3.140 V

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7:0	LDO7_ VOUT	0000 0000	R/W	1E	1.612 V	5E	2.124 V	9E	2.636 V	DE	3.148 V
				1F	1.620 V	5F	2.132 V	9F	2.644 V	DF	3.156 V
				20	1.628 V	60	2.140 V	A0	2.652 V	E0	3.164 V
				21	1.636 V	61	2.148 V	A1	2.660 V	E1	3.172 V
				22	1.644 V	62	2.156 V	A2	2.668 V	E2	3.180 V
				23	1.652 V	63	2.164 V	A3	2.676 V	E3	3.188 V
				24	1.660 V	64	2.172 V	A4	2.684 V	E4	3.196 V
				25	1.668 V	65	2.180 V	A5	2.692 V	E5	3.204 V
				26	1.676 V	66	2.188 V	A6	2.700 V	E6	3.212 V
				27	1.684 V	67	2.196 V	A7	2.708 V	E7	3.220 V
				28	1.692 V	68	2.204 V	A8	2.716 V	E8	3.228 V
				29	1.700 V	69	2.212 V	A9	2.724 V	E9	3.236 V
				2A	1.708 V	6A	2.220 V	AA	2.732 V	EA	3.244 V
				2B	1.716 V	6B	2.228 V	AB	2.740 V	EB	3.252 V
				2C	1.724 V	6C	2.236 V	AC	2.748 V	EC	3.260 V
				2D	1.732 V	6D	2.244 V	AD	2.756 V	ED	3.268 V
				2E	1.740 V	6E	2.252 V	AE	2.764 V	EE	3.276 V
				2F	1.748 V	6F	2.260 V	AF	2.772 V	EF	3.284 V
				30	1.756 V	70	2.268 V	B0	2.780 V	F0	3.292 V
				31	1.764 V	71	2.276 V	B1	2.788 V	F1	3.300 V
				32	1.772 V	72	2.284 V	B2	2.796 V	F2	3.308 V
				33	1.780 V	73	2.292 V	**B3**	**2.804 V**	F3	3.316 V
				34	1.788 V	74	2.300 V	B4	2.812 V	F4	3.324 V
				35	1.796 V	75	2.308 V	B5	2.820 V	F5	3.332 V
				36	1.804 V	76	2.316 V	B6	2.828 V	F6	3.340 V
				37	1.812 V	77	2.324 V	B7	2.836 V	F7	3.348 V
				38	1.820 V	78	2.332 V	B8	2.844 V	F8	3.356 V
				39	1.828 V	79	2.340 V	B9	2.852 V	F9	3.364 V
				3A	1.836 V	7A	2.348 V	BA	2.860 V	FA	3.372 V
				3B	1.844 V	7B	2.356 V	BB	2.868 V	FB	3.380 V
				3C	1.852 V	7C	2.364 V	BC	2.876 V	FC	3.388 V
				3D	1.860 V	7D	2.372 V	BD	2.884 V	FD	3.396 V
				3E	1.868 V	7E	2.380 V	BE	2.892 V	FE	3.404 V
				3F	1.876 V	7F	2.388 V	BF	2.900 V	FF	3.412 V

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REGISTER DETAILS – 0x0B LDO12_SEQ

Default = 00000000

Bits	Name	Default	Type	Description
7:6	UNUSED			
5:3	LDO2_SEQ	000	R/W	The LDO2 sequencing is selected by setting bits [5:3].
				Code / **Slot Selected**
				000 – Controlled through I²C by setting the LDO2_EN bit.
				001 – Selects slot 1 for the LDO2 to be enabled at power up.
				010 – Selects slot 2 for the LDO2 to be enabled at power up.
				011 – Selects slot 3 for the LDO2 to be enabled at power up.
				100 – Selects slot 4 for the LDO2 to be enabled at power up.
				101 – Selects slot 5 for the LDO2 to be enabled at power up.
				110 – Selects slot 6 for the LDO2 to be enabled at power up.
				111 – Selects slot 7 for the LDO2 to be enabled at power up.
2:0	LDO1_SEQ	000	R/W	The LDO1 sequencing is selected by setting bits [2:0].
				Code / **Slot Selected**
				000 – Controlled through I²C by setting the LDO1_EN bit.
				001 – Selects slot 1 for the LDO1 to be enabled at power up.
				010 – Selects slot 2 for the LDO1 to be enabled at power up.
				011 – Selects slot 3 for the LDO1 to be enabled at power up.
				100 – Selects slot 4 for the LDO1 to be enabled at power up.
				101 – Selects slot 5 for the LDO1 to be enabled at power up.
				110 – Selects slot 6 for the LDO1 to be enabled at power up.
				111 – Selects slot 7 for the LDO1 to be enabled at power up.

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REGISTER DETAILS – 0x0C LDO34_SEQ

Default = 00000000

Bits	Name	Default	Type	Description
7:6	UNUSED			
5:3	LDO4_SEQ	000	R/W	The LDO4 sequencing is selected by setting bits [5:3]. **Code** – **Slot Selected** 000 – Controlled through I²C by setting the LDO4_EN bit. 001 – Selects slot 1 for the LDO4 to be enabled at power up. 010 – Selects slot 2 for the LDO4 to be enabled at power up. 011 – Selects slot 3 for the LDO4 to be enabled at power up. 100 – Selects slot 4 for the LDO4 to be enabled at power up. 101 – Selects slot 5 for the LDO4 to be enabled at power up. 110 – Selects slot 6 for the LDO4 to be enabled at power up. 111 – Selects slot 7 for the LDO4 to be enabled at power up.
2:0	LDO3_SEQ	000	R/W	The LDO3 sequencing is selected by setting bits [2:0]. **Code** – **Slot Selected** 000 – Controlled through I²C by setting the LDO3_EN bit. 001 – Selects slot 1 for the LDO3 to be enabled at power up. 010 – Selects slot 2 for the LDO3 to be enabled at power up. 011 – Selects slot 3 for the LDO3 to be enabled at power up. 100 – Selects slot 4 for the LDO3 to be enabled at power up. 101 – Selects slot 5 for the LDO3 to be enabled at power up. 110 – Selects slot 6 for the LDO3 to be enabled at power up. 111 – Selects slot 7 for the LDO3 to be enabled at power up.

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REGISTER DETAILS – 0x0D LDO56_SEQ

Default = 00000000

Bits	Name	Default	Type	Description
7:6	UNUSED			
5:3	LDO6_SEQ	000	R/W	The LDO6 sequencing is selected by setting bits [5:3]. **Code** – **Slot Selected** 000 – Controlled through I²C by setting the LDO6_EN bit 001 – Selects slot 1 for the LDO6 to be enabled in at power up 010 – Selects slot 2 for the LDO6 to be enabled in at power up 011 – Selects slot 3 for the LDO6 to be enabled in at power up 100 – Selects slot 4 for the LDO6 to be enabled in at power up 101 – Selects slot 5 for the LDO6 to be enabled in at power up 110 – Selects slot 6 for the LDO6 to be enabled in at power up 111 – Selects slot 7 for the LDO6 to be enabled in at power up
2:0	LDO5_SEQ	000	R/W	The LDO5 sequencing is selected by setting bits [2:0]. **Code** – **Slot Selected** 000 – Controlled through I²C by setting the LDO5_EN bit 001 – Selects slot 1 for the LDO5 to be enabled in at power up 010 – Selects slot 2 for the LDO5 to be enabled in at power up 011 – Selects slot 3 for the LDO5 to be enabled in at power up 100 – Selects slot 4 for the LDO5 to be enabled in at power up 101 – Selects slot 5 for the LDO5 to be enabled in at power up 110 – Selects slot 6 for the LDO5 to be enabled in at power up 111 – Selects slot 7 for the LDO5 to be enabled in at power up

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REGISTER DETAILS – 0x0E LDO7_SEQ

Default = 00000000

Bits	Name	Default	Type	Description	
7:6	UNUSED				
5:3	LDO7_SEQ	000	R/W	The LDO7 sequencing is selected by setting bits [5:3].	
				Code	**Slot Selected**
				000	Controlled through I²C by setting the LDO7_EN bit.
				001	Selects slot 1 for the LDO7 to be enabled at power up.
				010	Selects slot 2 for the LDO7 to be enabled at power up.
				011	Selects slot 3 for the LDO7 to be enabled at power up.
				100	Selects slot 4 for the LDO7 to be enabled at power up.
				101	Selects slot 5 for the LDO7 to be enabled at power up.
				110	Selects slot 6 for the LDO7 to be enabled at power up.
				111	Selects slot 7 for the LDO7 to be enabled at power up.

REGISTER DETAILS – 0x0F SEQUENCING

Default = 00000000

Bits	Name	Default	Type	Description	
7:6	SEQ_SPEED	00	R/W	**Code**	**Period per Slot**
				00	500 µs
				01	1.0 ms
				10	1.5 ms
				11	2.0 ms
5:4	SEQ_CONTROL	00	W/CLR	**Code**	**Initialize Power-Up or Power-Down**
				00	Default
				01	Starts an LDO power-up sequence.
				10	Starts an LDO shutdown sequence.
				11	Bit configuration is ignored.
3	SEQ_ON	0	Read	**Code**	**The indicator of the sequencer status. Read only.**
				0	Shut down
				1	Power up
2:0	SEQ_COUNT	000	Read	**Code**	**Present Slot**
				000	Indicates sequencing has completed or not started.
				001	Indicates sequencing is in slot 1 during register read.
				010	Indicates sequencing is in slot 2 during register read.
				011	Indicates sequencing is in slot 3 during register read.
				100	Indicates sequencing is in slot 4 during register read.
				101	Indicates sequencing is in slot 5 during register read.
				110	Indicates sequencing is in slot 6 during register read.
				111	Indicates sequencing is in slot 7 during register read.

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REGISTER DETAILS – 0x10 DISCHARGE

Default = 01111111

Bits	Name	Default	Type	Description	
7	UNUSED	0			
6	LDO1_DIS	1	R/W	**Code**	**Discharge Enabled/Disabled**
				0	LDO1 Active Discharge feature is disabled. Pull−down will not be activated when LDO1 is disabled by any event.
				1	LDO1 Active Discharge feature is enabled. Pull−down will be activated when LDO1 is disabled by RESET_B going low or LDO1_EN = 0 or a sequenced shutdown or in a UVP event.
5	LDO2_DIS	1	R/W	**Code**	**Discharge Enabled/Disabled**
				0	LDO2 Active Discharge feature is disabled. Pull−down will not be activated when LDO2 is disabled by any event.
				1	LDO2 Active Discharge feature is enabled. Pull−down will be activated when LDO2 is disabled by RESET_B going low or LDO2_EN = 0 or a sequenced shutdown or in a UVP event.
4	LDO3_DIS	1	R/W	**Code**	**Discharge Enabled/Disabled**
				0	LDO3 Active Discharge feature is disabled. Pull−down will not be activated when LDO3 is disabled by any event.
				1	LDO3 Active Discharge feature is enabled. Pull−down will be activated when LDO3 is disabled by RESET_B going low or LDO3_EN = 0 or a sequenced shutdown or in a UVP event.
3	LDO4_DIS	1	R/W	**Code**	**Discharge Enabled/Disabled**
				0	LDO4 Active Discharge feature is disabled. Pull−down will not be activated when LDO4 is disabled by any event.
				1	LDO4 Active Discharge feature is enabled. Pull−down will be activated when LDO4 is disabled by RESET_B going low or LDO4_EN = 0 or a sequenced shutdown or in a UVP event.
2	LDO5_DIS	1	R/W	**Code**	**Discharge Enabled/Disabled**
				0	LDO5 Active Discharge feature is disabled. Pull−down will not be activated when LDO5 is disabled by any event.
				1	LDO5 Active Discharge feature is enabled. Pull−down will be activated when LDO5 is disabled by RESET_B going low or LDO5_EN = 0 or a sequenced shutdown or in a UVP event.
1	LDO6_DIS	1	R/W	**Code**	**Discharge Enabled/Disabled**
				0	LDO6 Active Discharge feature is disabled. Pull−down will not be activated when LDO6 is disabled by any event.
				1	LDO6 Active Discharge feature is enabled. Pull−down will be activated when LDO6 is disabled by RESET_B going low or LDO6_EN = 0 or a sequenced shutdown or in a UVP event.

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0	LDO7_DIS	1	R/W	**Code**	**Discharge Enabled/Disabled**
				0	LDO7 Active Discharge feature is disabled. Pull−down will not be activated when LDO7 is disabled by any event.
				1	LDO7 Active Discharge feature is enabled. Pull−down will be activated when LDO7 is disabled by RESET_B going low or LDO7_EN = 0 or a sequenced shutdown or in a UVP event.

REGISTER DETAILS – 0x11 RESET

Default = 00000110

Bits	Name	Default	Type	Description	
7:4	SOFT_RESET	0000	Write	**Code**	**Software Reset**
				1011	Writing a “1011” begins a soft reset of the device I²C registers to their default values. This bit is cleared upon the execution of the reset function.
					Any other value than “1011” will be ignored.
3	UNUSED				
2:1	OCP_TIMER	11	R/W	Option bits to control the length of the deglitch timer for the current limit on all LDOs before a fault is triggered.	
				Code	**Deglitch Timer**
				00	125 µs
				01	250 µs
				10	500 µs
				11	1 ms
0	FLT_SD_B	0	R/W	**Code**	**Prevents shutdown when a fault occurs**
				0	LDO shuts down if a UVP or OCP event occurs or if the LDO’s input VIN12, VIN34, VIN5, VIN6 or VIN7 have a UVLO event.
				1	LDO does not shut down if a UVP or OCP event occurs. If the LDO’s input VIN12, VIN34, VIN5, VIN6 or VIN7 have a UVLO event, the associated LDO will shut down until the supply returns, but the fault will not be counted.
				Note: If this bit function is desired, FLT_SD_B should be set to “1” prior to enabling any LDOs after a Power−on−Reset.	

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REGISTER DETAILS – 0x12 12C_ADDR

Default = 10000001

Bits	Name	Default	Type	Description	
7	INT_LEVEL_SEL	0	R/W	**Code**	**INT PUSH-PULL Output Level Select**
				0	Output 1.8 V when INT high
				1	Cutout 1.2 V when INT high
6	INT_OutMode_SEL	0	R/W	**Code**	**INT Output Mode Select**
				0	Using PUSH-PULL for output
				1	Using OPEN-DRAIN for output
5:2	UNUSED		R/W		
1:0	I²C_ADDR_SEL	01	R/W	**Code**	**I²C Address Settings**
				00	0x20
				01	0x35
				10	0x61
				11	0x72

REGISTER DETAILS – 0x13, 0x14 RESERVED

REGISTER DETAILS – 0x15 INTERRUPT1

Default = 00000000

Bits	Name	Default	Type	Description	
7	UNUSED				
6	LDO7_UVP_INT	0	R/CLR	**Code**	**LDO7 UVP Interrupt**
				0	Clear
				1	Under−voltage event occurred on LDO7 output.
5	LDO6_UVP_INT	0	R/CLR	**Code**	**LDO6 UVP Interrupt**
				0	Clear
				1	Under−voltage event occurred on LDO6 output.
4	LDO5_UVP_INT	0	R/CLR	**Code**	**LDO5 UVP Interrupt**
				0	Clear
				1	Under−voltage event occurred on LDO5 output.
3	LDO4_UVP_INT	0	R/CLR	**Code**	**LDO4 UVP Interrupt**
				0	Clear
				1	Under−voltage event occurred on LDO4 output.
2	LDO3_UVP_INT	0	R/CLR	**Code**	**LDO3 UVP Interrupt**
				0	Clear
				1	Under−voltage event occurred on LDO3 output.

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1	LDO2_UVP_INT	0	R/CLR	**Code**	**LDO2 UVP Interrupt**
				0	Clear
				1	Under−voltage event occurred on LDO2 output.
0	LDO1_UVP_INT	0	R/CLR	**Code**	**LDO1 UVP Interrupt**
				0	Clear
				1	Under−voltage event occurred on LDO1 output.

REGISTER DETAILS – 0x16 INTERRUPT2

Default = 00000000

Bits	Name	Default	Type	Description	
7	UNUSED				
6	LDO7_OCP_INT	0	R/CLR	**Code**	**LDO7 OCP Interrupt**
				0	Clear
				1	Over−current event detected on LDO7 output.
5	LDO6_OCP_INT	0	R/CLR	**Code**	**LDO6 OCP Interrupt**
				0	Clear
				1	Over−current event detected on LDO6 output.
4	LDO5_OCP_INT	0	R/CLR	**Code**	**LDO5 OCP Interrupt**
				0	Clear
				1	Over−current event detected on LDO5 output.
3	LDO4_OCP_INT	0	R/CLR	**Code**	**LDO4 OCP Interrupt**
				0	Clear
				1	Over−current event detected on LDO4 output.
2	LDO3_OCP_INT	0	R/CLR	**Code**	**LDO3 OCP Interrupt**
				0	Clear
				1	Over−current event detected on LDO3 output.
1	LDO2_OCP_INT	0	R/CLR	**Code**	**LDO2 OCP Interrupt**
				0	Clear
				1	Over−current event detected on LDO2 output.
0	LDO1_OCP_INT	0	R/CLR	**Code**	**LDO1 OCP Interrupt**
				0	Clear
				1	Over−current event detected on LDO1 output.

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REGISTER DETAILS – 0x17 INTERRUPT3

Default = 00000000

Bits	Name	Default	Type	Description	
7	TSD_INT	0	R/CLR	**Code**	**Thermal Shutdown Interrupt**
				0	Clear
				1	A Thermal Shutdown event is detected or the temperature has fallen below the hysteresis level.
6	TSD_WRN_INT	0	R/CLR	**Code**	**Thermal Warning Interrupt**
				0	Clear
				1	The Thermal Shutdown Warning threshold was surpassed or the temperature has fallen below the hysteresis level.
5	VSYS_UVLO_INT	0	R/CLR	**Code**	**VSYS Under−Voltage−Lock−Out Interrupt**
				0	Clear
				1	VSYS fell below the UVLO falling threshold or that VSYS have risen above the UVLO rising threshold after a UVLO fault.
				Reading the associated status bit provides the present state of the input voltage.	
4	LDO7_UVLO_INT	0	R/CLR	**Code**	**VIN7 Under−Voltage−Lock−Out Interrupt**
				0	Clear
				1	VIN7 fell below the UVLO falling threshold while LDO7 was enabled or VIN7 has risen above the UVLO rising threshold after a UVLO fault.
				Reading the associated status bit provides the present state of the input voltage.	
3	LDO6_UVLO_INT	0	R/CLR	**Code**	**VIN6 Under−Voltage−Lock−Out Interrupt**
				0	Clear
				1	VIN6 fell below the UVLO falling threshold while LDO6 was enabled or VIN6 has risen above the UVLO rising threshold after a UVLO fault.
				Reading the associated status bit provides present state of the input voltage.	
2	LDO5_UVLO_INT	0	R/CLR	**Code**	**VIN5 Under−Voltage−Lock−Out Interrupt**
				0	Clear
				1	VIN5 fell below the UVLO falling threshold while LDO5 was enabled or VIN5 has risen above the UVLO rising threshold after a UVLO fault.
				Reading the associated status bit provides the present state of the input voltage.	
1	LDO34_UVLO_INT	0	R/CLR	**Code**	**VIN34 Under−Voltage−Lock−Out Interrupt**
				0	Clear
				1	VIN34 fell below the UVLO falling threshold while LDO3 and/or LDO4 were enabled or VIN34 has risen above the rising UVLO

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					thresholds after a UVLO fault.
				Reading the associated status bit provides the present state of the input voltage.	
0	LDO12_UVLO_INT	0	R/CLR	**Code**	**VIN12 Under−Voltage−Lock−Out Interrupt**
				0	Clear
				1	VIN12 fell below the UVLO falling threshold while LDO1 and/or LDO2 were enabled or VIN12 has risen above the UVLO rising threshold after a UVLO fault.
				Reading the associated status bit provides the present state of the input voltage.	

REGISTER DETAILS – 0x18 STATUS1

Default = 00000000

Bits	Name	Default	Type	Description	
7	UNUSED				
6	LDO7_UVP_STAT	0	Read	**Code**	**LDO7 UVP Status**
				0	Normal operation
				1	An under−voltage condition exists on LDO7 output.
5	LDO6_UVP_STAT	0	Read	**Code**	**LDO6 UVP Status**
				0	Normal operation
				1	An under−voltage condition exists on LDO6 output.
4	LDO5_UVP_STAT	0	Read	**Code**	**LDO5 UVP Status**
				0	Normal operation
				1	An under−voltage condition exists on LDO5 output.
3	LDO4_UVP_STAT	0	Read	**Code**	**LDO4 UVP Status**
				0	Normal operation
				1	An under−voltage condition exists on LDO4 output.
2	LDO3_UVP_STAT	0	Read	**Code**	**LDO3 UVP Status**
				0	Normal operation
				1	An under−voltage condition exists on LDO3 output.
1	LDO2_UVP_STAT	0	Read	**Code**	**LDO2 UVP Status**
				0	Normal operation
				1	An under−voltage condition exists on LDO2 output.
0	LDO1_UVP_STAT	0	Read	**Code**	**LDO1 UVP Status**
				0	Normal operation
				1	An under−voltage condition exists on LDO1 output.

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REGISTER DETAILS – 0x19 STATUS2

Default = 00000000

Bits	Name	Default	Type	Description	
7	UNUSED				
6	LDO7_OCP_STAT	0	Read	**Code**	**LDO7 OCP Status**
				0	Normal operation
				1	An over−current condition exists on LDO7 output.
5	LDO6_OCP_STAT	0	Read	**Code**	**LDO6 OCP Status**
				0	Normal operation
				1	An over−current condition exists on LDO6 output.
4	LDO5_OCP_STAT	0	Read	**Code**	**LDO5 OCP Status**
				0	Normal operation
				1	An over−current condition exists on LDO5 output.
3	LDO4_OCP_STAT	0	Read	**Code**	**LDO4 OCP Status**
				0	Normal operation
				1	An over−current condition exists on LDO4 output.
2	LDO3_OCP_STAT	0	Read	**Code**	**LDO3 OCP Status**
				0	Normal operation
				1	An over−current condition exists on LDO3 output.
1	LDO2_OCP_STAT	0	Read	**Code**	**LDO2 OCP Status**
				0	Normal operation
				1	An over−current condition exists on LDO2 output.
0	LDO1_OCP_STAT	0	Read	**Code**	**LDO1 OCP Status**
				0	Normal operation
				1	An over−current condition exists on LDO1 output.

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REGISTER DETAILS – 0x1A STATUS3

Default = 00000000

Bits	Name	Default	Type	Description	
7	TSD_STAT	0	Read	**Code**	**Thermal Shutdown Status**
				0	Normal operation
				1	Device is in Thermal Shutdown.
6	TSD_WRN_STAT	0	Read	**Code**	**Thermal Warning Status**
				0	Normal operation
				1	The temperature is above the Thermal Warning level and shutdown is impending.
5	VSYS_UVLO_STAT	0	Read	**Code**	**VSYS Under−Voltage−Lock−Out Status**
				0	Normal operation
				1	VSYS is below the UVLO threshold.
4	LDO7_UVLO_STAT	0	Read	**Code**	**VIN7 Under−Voltage−Lock−Out Status**
				0	Normal operation
				1	VIN7 is below the UVLO threshold while LDO7 is enabled.
3	LDO6_UVLO_STAT	0	Read	**Code**	**VIN6 Under−Voltage−Lock−Out Status**
				0	Normal operation
				1	VIN6 is below the UVLO threshold while LDO6 is enabled.
2	LDO5_UVLO_STAT	0	Read	**Code**	**VIN5 Under−Voltage−Lock−Out Status**
				0	Normal operation
				1	VIN5 is below the UVLO threshold while LDO5 is enabled.
1	LDO34_UVLO_STAT	0	Read	**Code**	**VIN34 Under−Voltage−Lock−Out Status**
				0	Normal operation
				1	VIN34 is below the UVLO threshold while LDO3 and/or LDO4 are enabled.
0	LDO12_UVLO_STAT	0	Read	**Code**	**VIN12 Under−Voltage−Lock−Out Status**
				0	Normal operation
				1	VIN12 is below the UVLO threshold while LDO1 and/or LDO2 are enabled.

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REGISTER DETAILS – 0x1B STATUS4

Default = 00000000

Bits	Name	Default	Type	Description	
7	CHIP_SUSD	0	Read	**Code**	**Chip Suspension**
				0	Chip in normal state
				1	The entire chip has been suspended due to a global fault condition.
6	LDO7_SUSD	0	Read	**Code**	**LDO7 Output Suspended**
				0	LDO7 in normal state
				1	LDO7 has been suspended due to a fault condition.
5	LDO6_SUSD	0	Read	**Code**	**LDO6 Output Suspended**
				0	LDO6 in normal state
				1	LDO6 has been suspended due to a fault condition.
4	LDO5_SUSD	0	Read	**Code**	**LDO5 Output Suspended**
				0	LDO5 in normal state
				1	LDO5 has been suspended due to a fault condition.
3	LDO4_SUSD	0	Read	**Code**	**LDO4 Output Suspended**
				0	LDO4 in normal state
				1	LDO4 has been suspended due to a fault condition.
2	LDO3_SUSD	0	Read	**Code**	**LDO3 Output Suspended**
				0	LDO3 in normal state
				1	LDO3 has been suspended due to a fault condition.
1	LDO2_SUSD	0	Read	**Code**	**LDO2 Output Suspended**
				0	LDO2 in normal state
				1	LDO2 has been suspended due to a fault condition.
0	LDO1_SUSD	0	Read	**Code**	**LDO1 Output Suspended**
				0	LDO1 in normal state
				1	LDO1 has been suspended due to a fault condition.

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REGISTER DETAILS – 0x1C MINT1

Default = 00000000

Bits	Name	Default	Type	Description	
7	UNUSED				
6	MASK_LDO7 _UVP	0	R/W	**Code**	**LDO7 UVP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO7 under−voltage interrupt occurs.
5	MASK_LDO6 _UVP	0	R/W	**Code**	**LDO6 UVP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO6 under−voltage interrupt occurs.
4	MASK_LDO5 _UVP	0	R/W	**Code**	**LDO5 UVP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO5 under−voltage interrupt occurs.
3	MASK_LDO4 _UVP	0	R/W	**Code**	**LDO4 UVP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO4 under−voltage interrupt occurs.
2	MASK_LDO3 _UVP	0	R/W	**Code**	**LDO3 UVP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO3 under−voltage interrupt occurs.
1	MASK_LDO2 _UVP	0	R/W	**Code**	**LDO2 UVP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO2 under−voltage interrupt occurs.
0	MASK_LDO1 _UVP	0	R/W	**Code**	**LDO1 UVP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO1 under−voltage interrupt occurs.

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REGISTER DETAILS – 0x1D MINT2

Default = 00000000

Bits	Name	Default	Type	Description	
7	UNUSED				
6	MASK_LDO7 _OCP	0	R/W	**Code**	**LDO7 OCP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO7 over−current interrupt occurs.
5	MASK_LDO6 _OCP	0	R/W	**Code**	**LDO6 OCP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO6 over−current interrupt occurs.
4	MASK_LDO5 _OCP	0	R/W	**Code**	**LDO5 OCP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO5 over−current interrupt occurs.
3	MASK_LDO4 _OCP	0	R/W	**Code**	**LDO4 OCP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO4 over−current interrupt occurs.
2	MASK_LDO3 _OCP	0	R/W	**Code**	**LDO3 OCP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO3 over−current interrupt occurs.
1	MASK_LDO2 _OCP	0	R/W	**Code**	**LDO2 OCP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO2 over−current interrupt occurs.
0	MASK_LDO1 _OCP	0	R/W	**Code**	**LDO1 OCP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO1 over−current interrupt occurs.

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REGISTER DETAILS – 0x1E MINT3

Default = 00000000

Bits	Name	Default	Type	Description	
7	MASK_TSD	0	R/W	**Code**	**Thermal Shutdown MASK**
				0	No masking of interrupt
				1	INT pin will not change states when a Thermal Shutdown interrupt occurs.
6	MASK_TSD_WRN	0	R/W	**Code**	**Thermal Warning MASK**
				0	No masking of interrupt
				1	INT pin will not change states when a Thermal Warning interrupt occurs.
5	MASK_VSYS_UVLO	0	R/W	**Code**	**VSYS UVLO MASK**
				0	No masking of interrupt
				1	INT pin will not change states when VSYS input power under−voltage interrupt occurs.
4	MASK_LDO7_UVLO	0	R/W	**Code**	**LDO7 UVLO MASK**
				0	No masking of interrupt
				1	INT pin will not change states when VIN7 input power under−voltage interrupt occurs.
3	MASK_LDO6_UVLO	0	R/W	**Code**	**VIN6 UVLO MASK**
				0	No masking of interrupt
				1	INT pin will not change states when VIN6 input power under−voltage interrupt occurs.
2	MASK_LDO5_UVLO	0	R/W	**Code**	**VIN5 UVLO MASK**
				0	No masking of interrupt
				1	INT pin will not change states when VIN5 input power under−voltage interrupt occurs.
1	MASK_LDO34_UVLO	0	R/W	**Code**	**VIN34 UVLO MASK**
				0	No masking of interrupt
				1	INT pin will not change states when VIN34 input power under−voltage interrupt occurs.
0	MASK_LDO12_UVLO	0	R/W	**Code**	**VIN12 UVLO MASK**
				0	No masking of interrupt
				1	INT pin will not change states when VIN12 input power under−voltage interrupt occurs.

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CONTACT US

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