DIO2399A/B

Voltage Output, High or Low Side Measurement, Bi-Directional Zero-Drift Series Current Shunt Monitor

Features

- Wide common-mode range: -0.3V to 26V
- Offset voltage: 150μV (Max)
  (Enable shunt drops of 10mV full-scale)
- Accuracy
  - ±1.5% Gain error (Max over temperature)
  - 0.5μV/℃ Offset drift (Typ)
  - 10ppm/℃ Gain drift (Max)
- Choice of Gains:
  - DIO2399A: 50V/V
  - DIO2399B: 100V/V
- Quiescent current: 100μA (Max)
- Packages: SC70-6, thin DQFN-10

Descriptions

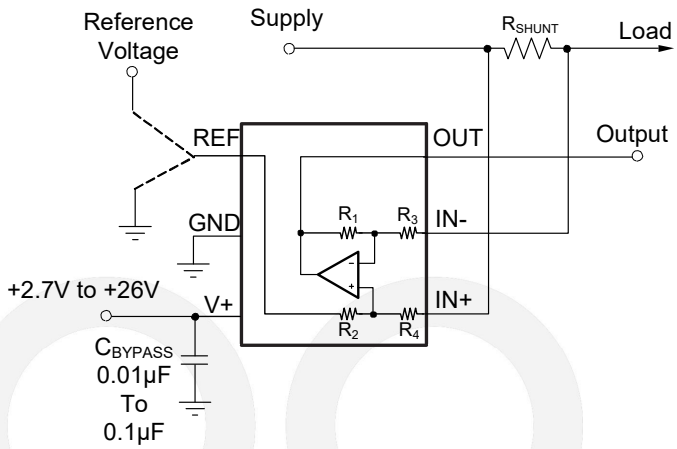
The DIO2399x series of voltage output current shunt monitors can sense drops across shunts at common-mode voltages from -0.3V to 26V, independent of the supply voltage. Two fixed gains are available: 50V/V and 100V/V. The low offset of the Zero-Drift architecture enables current sensing with maximum drops across the shunt as low as 10mV full-scale.

These devices operate from a single +2.7V to +26V power supply, drawing a maximum of 100μA of supply current. All versions are specified from -40℃ to +105℃, and offered in both SC70-6 and thin DQFN-10 packages.

Applications

- Notebook Computers
- Cell Phones
- Telecom Equipment
- Power Management
- Battery Chargers
- Welding Equipment

Block Diagram



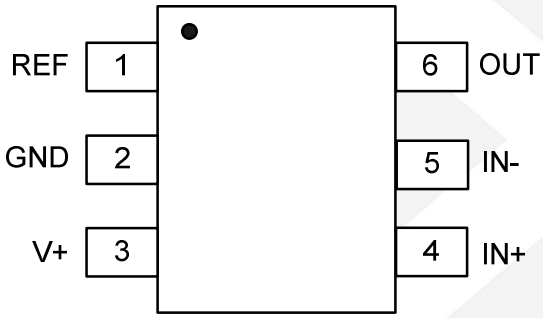
Ordering Information

Order Part Number	Top Marking		T_A	Package	
DIO2399ASC6	YWZX	Green	-40 to +85°C	SC70-6	Tape & Reel, 3000
DIO2399BSC6	YWZX	Green	-40 to +85°C	SC70-6	Tape & Reel, 3000
DIO2399ALP10	YW ZX	Green	-40 to +85°C	DQFN-10	Tape & Reel, 3000
DIO2399BLP10	YW ZX	Green	-40 to +85°C	DQFN-10	Tape & Reel, 3000

Marking Definition

Pin Assignments

SC70-6



DQFN-10

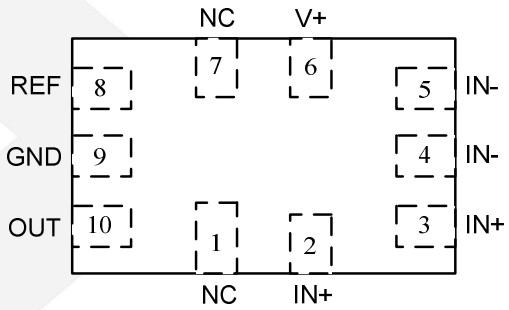


Figure 1 Pin Assignment (Top View)

Pin Description

Pin name	Description
REF	Reference voltage
GND	Ground
V+	Positive supply
IN+	Positive Input
IN-	Negative Input
OUT	Output
NC	No connection

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maxim rating conditions for extended periods may affect device reliability.

Parameter		Rating	Unit
Supply Voltage		+26	V
Analogy Inputs, V_{IN+}, V_{IN-}	Differential (V_{IN+}) – (V_{IN-})	-26 to +26	V
	Common-mode	GND-0.3 to +26	V
ERF Input		GND-0.3 to (V+)+0.3	V
Output		GND-0.3 to (V+)+0.3	V
Input Current Into All Pins		5	mA
Operating Temperature		-40 to +105	℃
Storage Temperature		-65 to +150	℃
Junction Temperature		+150	℃
Thermal Resistance θ_{JA}	SC70-6	250	℃/W
	DQFN-10	80	℃/W
ESD	HBM	3000	V

Electrical Characteristics

Typical value: T_A = 25°C, V_S=+5V, V_{IN+}=12V, V_{SENSE}=V_{IN+}-V_{IN-}, and V_{REF}=V_S/2, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input						
V_{CM}	Common-Mode Input Range		-0.3		26	V
CMR	Common-Mode Rejection	V_{IN+}=0V to +26V, V_{SENSE}=0mV		90		dB
V_{OS}	Offset Voltage, RTI	V_{SENSE}=0mV, Vcom=VS/2		±5	±30	μV
		V_{SENSE}=0mV, Vcom=8V		±5	±150	μV
dV_{OS}/dT	Input vs Temperature			0.5		μV/℃
PSR	Input vs Power Supply	V_S=+2.7V to +18V, V_{IN+}=+18V, V_{SENSE}=0mV		120		dB
I_B	Input Bias Current	V_{SENSE}=0mV		28		μA
I_{OS}	Input Offset Current	V_{SENSE}=0mV		±0.02		μA

Output						
G	Gain	DIO2399A		50		V/V
		DIO2399B		100		
	Gain Error	V_{SENSE}=-8mV to 8mV		±0.03	±1.5	%
Voltage Output						
	Swing to V+ Power-Supply Rail	R_L=10kΩ to GND		(V+) - 0.05	(V+) - 0.2	V
	Swing to GND	R_L=10kΩ to GND		(V_{GND}) + 0.005	(V_{GND}) + 0.05	V
Frequency Response						
BW	f (-3dB) Bandwidth	C_{LOAD}=10pF, DIO2399A		5		kHz
		C_{LOAD}=10pF, DIO2399B		5		
SR	Slew Rate			0.007		V/μs
Power Supply						
V_S	Operating Voltage Range		+2.7		+26	V
I_Q	Quiescent Current	V_{SENSE}=0mV		65	100	μA
	Over Temperature				125	μA

Notes: RTI = Referred-to-input

Specifications subject to change without notice.

Typical Performance Characteristics

Typical value: T_A = 25°C, V_S=+5V, V_{IN+}=12V, V_{SENSE}=V_{IN+}-V_{IN-}, and V_{REF}=V_S/2, unless otherwise specified.

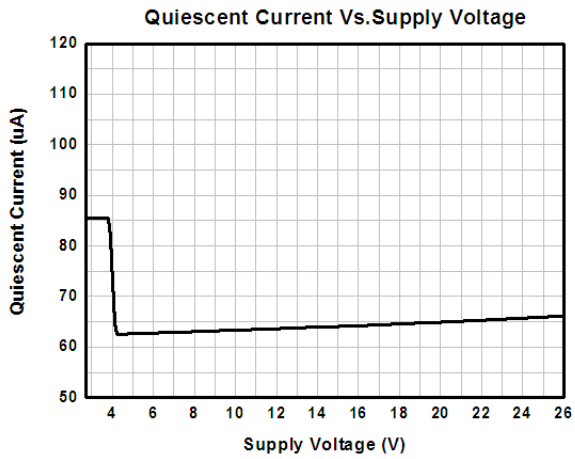


Figure 2. Quiescent Current Vs. Supply Voltage

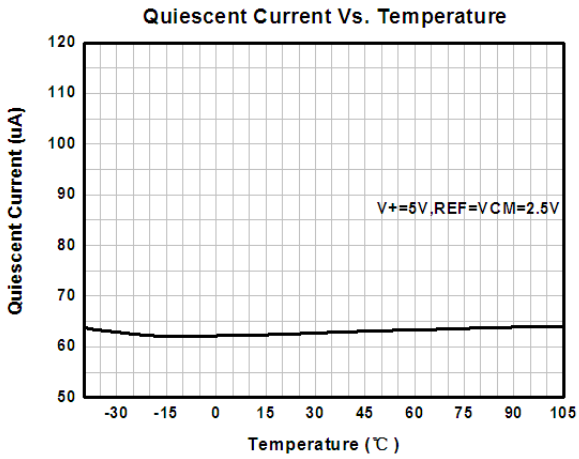


Figure 3. Quiescent Current Vs. Temperature

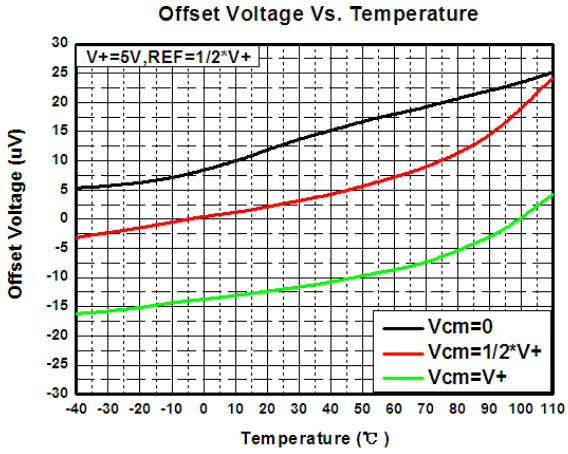


Figure 4. Offset Voltage Vs. Temperature
（DIO2399A: 50V/V）

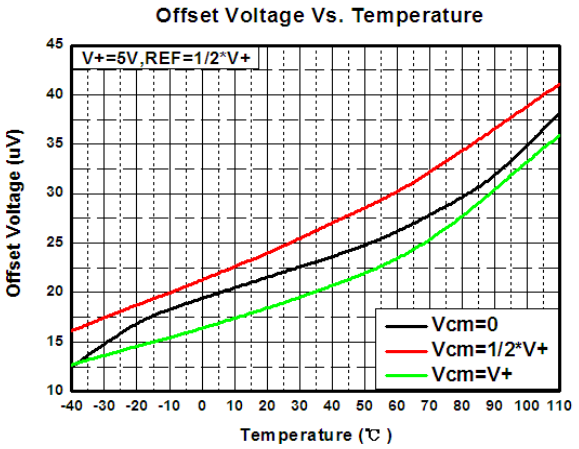


Figure 5. Offset Voltage Vs. Temperature
（DIO2399B: 100V/V）

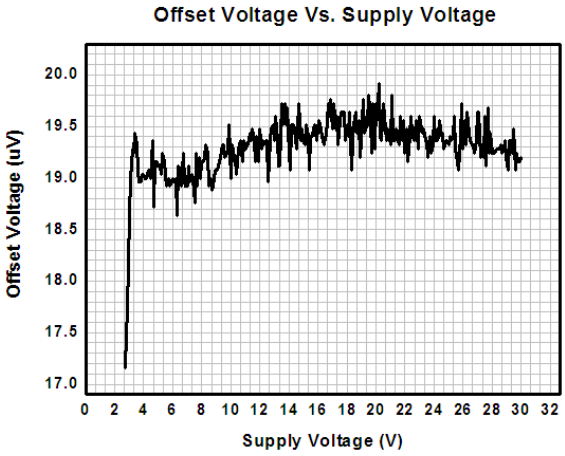


Figure 6. Offset Voltage Vs. Supply Voltage

Typical Application

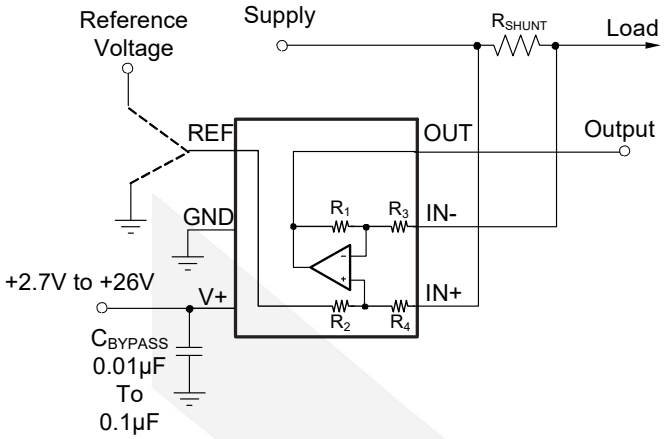


Figure 7. Input and Output AC-Coupling Application

Figure 7 shows the basic connections for the DIO2399x. The input pins, IN+ and IN–, should be connected as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

On the DQFN-10 package, two pins are provided for each input. These pins should be tied together (that is, tie IN+ to IN+ and tie IN– to IN–).

Power Supply

The input circuitry of the DIO2399x can accurately measure beyond its power-supply voltage, V+. For example, the V+ power supply can be 5V, whereas the load power-supply voltage can be as high as +26V. However, the output voltage range of the OUT terminal is limited by the voltages on the power-supply pin.

Selecting R_S

The zero-drift offset performance of the DIO2399x offers several benefits. Most often, the primary advantage of the low offset characteristic enables lower full-scale drops across the shunt. For example, non-zero-drift current shunt monitors typically require a full-scale range of 100mV.

The DIO2399x series of current-shunt monitors give equivalent accuracy at a full-scale range on the order of 10mV. This accuracy reduces shunt dissipation by an order of magnitude with many additional benefits.

Alternatively, there are applications that must measure current over a wide dynamic range that can take advantage of the low offset on the low end of the measurement. Most often, these applications can use the lower gain of 100 to accommodate larger shunt drops on the upper end of the scale.

Unidirectional Operation

Unidirectional operation allows the DIO2399x to measure currents through a resistive shunt in one direction. The most frequent case of unidirectional operation sets the output at ground by connecting the REF pin to ground. In unidirectional applications where the highest possible accuracy is desirable at very low inputs, bias the REF pin to a convenient value above 50mV to get the device output swing into the linear range for zero inputs.

A less frequent case of unipolar output biasing is to bias the output by connecting the REF pin to the supply; in this case, the quiescent output for zero input is at quiescent supply. This configuration would only respond to

negative currents (inverted voltage polarity at the device input).

Bidirectional Operation

Bidirectional operation allows the DIO2399x to measure currents through a resistive shunt in two directions. In this case, the output can be set anywhere within the limits of what the reference inputs allow (that is, between 0V to V+). Typically, it is set at half-scale for equal range in both directions. In some cases, however, it is set at a voltage other than half-scale when the bidirectional current is nonsymmetrical.

The quiescent output voltage is set by applying voltage to the reference input. Under zero differential input conditions the output assumes the same voltage that is applied to the reference input.

Input Filtering

An obvious and straightforward filtering location is at the device output. However, this location negates the advantage of the low output impedance of the internal buffer. The only other filtering option is at the device input pins. This location, though, does require consideration of the ±30% tolerance of the internal resistances. Figure 8 shows a filter placed at the inputs pins.

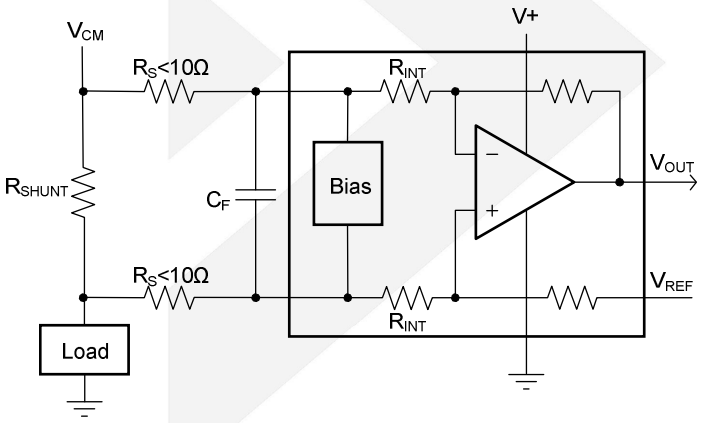


Figure 8. Filter at Input Pins

The addition of external series resistance, however, creates an additional error in the measurement so the value of these series resistors should be kept to 10Ω or less if possible to reduce impact to accuracy. The internal bias network shown in Figure 8 present at the input pins creates a mismatch in input bias currents when a differential voltage is applied between the input pins. If additional external series filter resistors are added to the circuit, the mismatch in bias currents results in a mismatch of voltage drops across the filter resistors. This mismatch creates a differential error voltage that subtracts from the voltage developed at the shunt resistor. This error results in a voltage at the device input pins that is different than the voltage developed across the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has little effect on device operation. The amount of error these external filter resistor add to the measurement can be calculated using Equation 2 where the gain error factor is calculated using Equation 1.

The amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance value as well as the internal input resistors, R3 and R4 (or R_{INT} as shown in Figure 8). The reduction of the shunt voltage reaching the device input pins appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance. The equation used to calculate the expected deviation from the shunt voltage to what is seen at the device input pins is given in Equation 1:

Gain Error $Factor = \frac{(1250 \times R_{INT})}{(1250 \times R_S) + (1250 \times R_{INT}) + (R_S \times R_{INT})}$ (1)

Where:

R_{INT} is the internal input resistor (R3 and R4), and

R_S is the external series resistance.

With the adjustment factor equation including the device internal input resistance, this factor varies with each gain version, as shown in Table1. Each individual device gain error factor is shown in Table 2.

Table 1. Input Resistance

Product	Gain	R_{INT}(kΩ)
DIO2399A	50	20
DIO2399B	100	10

Table 2. Device Gain Error Factor

Product	Simplified Gain Error Factor
DIO2399A	$\frac{20{,}000}{(17 \times R_S) + 20{,}000}$
DIO2399B	$\frac{10{,}000}{(9 \times R_S) + 10{,}000}$

The gain error that can be expected from the addition of the external series resistors can then be calculated based on Equation 2:

Gain Error (%)= 100-(100∗Gain Error Factor) (2)

REF Input Impedance Effects

As with any difference amplifier, the DIO2399x series common-mode rejection ratio is affected by any impedance present at the REF input. This concern is not a problem when the REF pin is connected directly to most references or power supplies. When using resistive dividers from the power supply or a reference voltage, the REF pin should be buffered by an op amp.

In systems where the DIO2399x output can be sensed differentially, such as by a differential input analog-to-digital converter (ADC) or by using two separate ADC inputs, the effects of external impedance on the REF input can be cancelled. Figure 9 depicts a method of taking the output from the DIO2399x by using the REF pin as a reference.

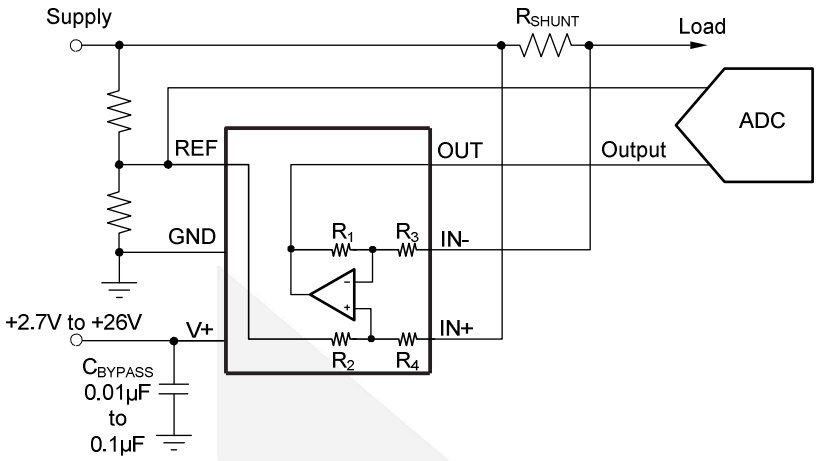


Figure 9. Sensing DIO2399x to Cancel Effects of Impedance on the REF Input

Using the DIO2399x with common-mode transients above 26V

With a small amount of additional circuitry, the DIO2399x series can be used in circuits subject to transients higher than 26V, such as automotive applications. Use only zener diode or zener-type transient absorbers (sometimes referred to as *Transzorbs*); any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors as shown in Figure 10 as a working impedance for the zener. It is desirable to keep these resistors as small as possible, most often around 10Ω. Larger values can be used with an effect on gain that is discussed in the section on input filtering. Because this circuit limits only short-term transients, many applications are satisfied with a 10Ω resistor along with conventional zener diodes of the lowest power rating that can be found. This combination uses the least amount of board space.

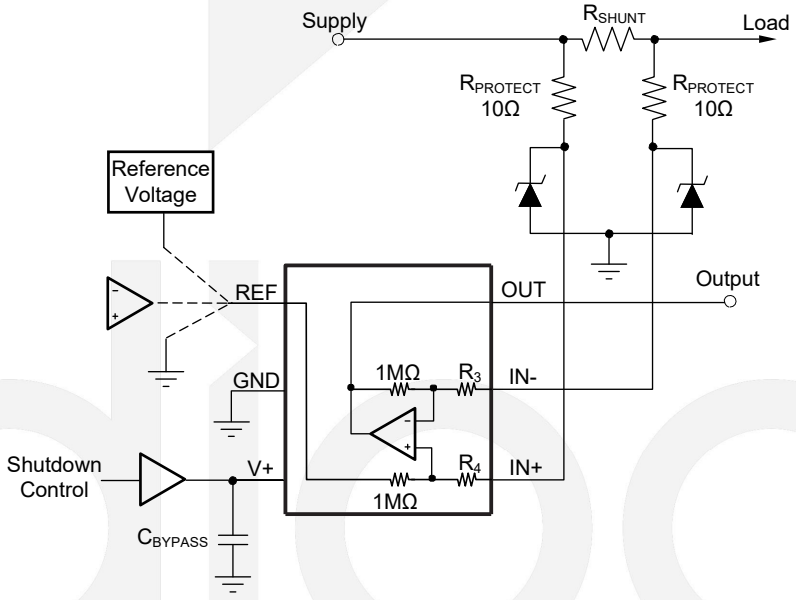


Figure 10. DIO2399x Transient Protection Using Dual Zener Diodes

In the event that low-power zeners do not have sufficient transient absorption capability and a higher power transzorb must be used, the most package-efficient solution then involves using a single transzorb and back-to-back diodes between the device inputs. This method is shown in Figure 11. The most space-efficient solutions are dual series-connected diodes in a single SOT-523 or SOD-523 package. In both examples shown in Figure 10 and Figure 11, the total board area required by the DIO2399x with all protective components is less than that of an SO-8 package, and only slightly greater than that of an MSOP-8 package.

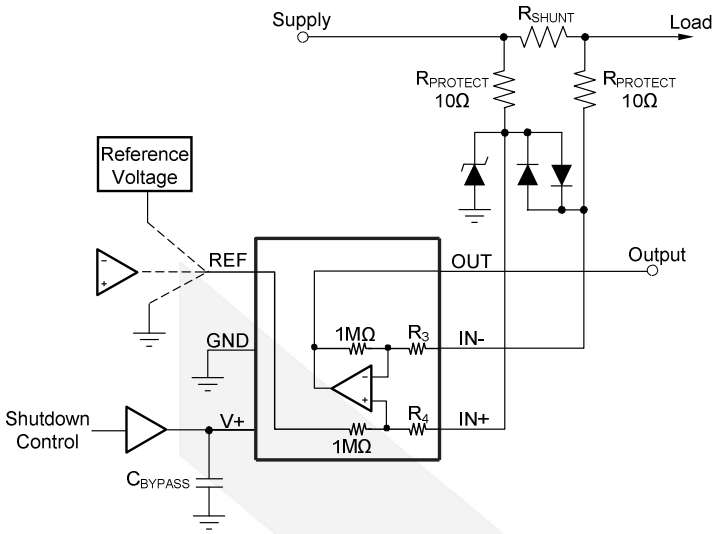


Figure 11. DIO2399x Transient Protection Using a Single Transzorb and Input Clamps

Improving transient robustness

Applications involving large input transients with excessive dV/dt above 2kV per microsecond present at the device input pins may cause damage to the internal ESD structures on version A devices. This potential damage is a result of the internal latching of the ESD structure to ground when this transient occurs at the input. With significant current available in most current-sensing applications, the large current flowing through the input transient-triggered, ground-shorted ESD structure quickly results in damage to the silicon. External filtering can be used to attenuate the transient signal prior to reaching the inputs to avoid the latching condition. Care must be taken to ensure that external series input resistance does not significantly impact gain error accuracy. For accuracy purposes, these resistances should be kept under 10Ω if possible. Ferrite beads are recommended for this filter because of their inherently low dc ohmic value. Ferrite beads with less than 10Ω of resistance at dc and over 600Ω of resistance at 100MHz to 200MHz are recommended. The recommended capacitor values for this filter are between 0.01μF and 0.1μF to ensure adequate attenuation in the high-frequency region. This protection scheme is shown in Figure 12. (Note: Capacitors used in high voltage applications should be greater than or equal to 30V)

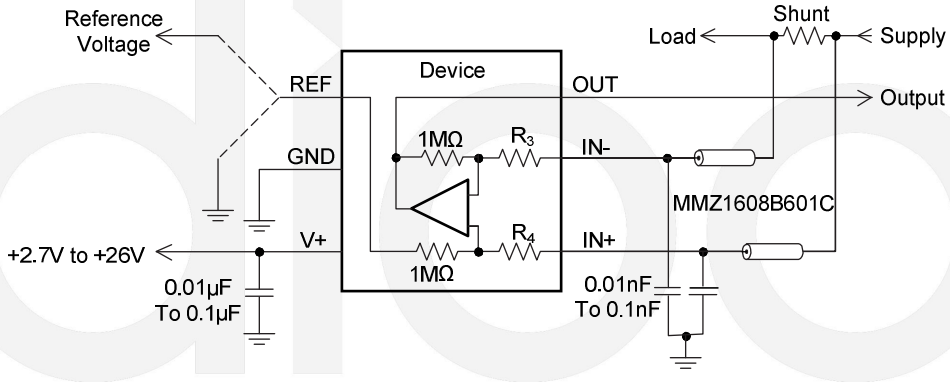


Figure 12. Transient Protection

To minimize the cost of adding these external components to protect the device in applications where large transient signals may be present, version B devices are now available with new ESD structures that are not susceptible to this latching condition. Version B devices are incapable of sustaining these damage causing latched conditions so they do not have the same sensitivity to the transients that the version A devices have, thus making the version B devices a better fit for these applications.

CONTACT US

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