

High-Efficiency, Extremely Small, 600 mA, Synchronous Step-Down Converter

■ Features

- 2.5 V to 5.5 V input voltage range
- Output voltage application:
0.9 V to 1.8 V ($\pm 2\%$)
- 600 mA output current capability
- Low operating quiescent current:
14 μ A (DIO62820)
- Efficiency ($f_{osc} = 5$ MHz): 88% ($V_{OUT} = 1.2$ V)
- Oscillation frequency: 4 MHz, 5 MHz
- Operation mode:
 - DIO62810: PWM control
 - DIO62820: PWM/PFM auto

■ Applications

- Camera modules
- Wearable devices
- Smart phones / mobile phones
- Wireless earphones / headsets
- Various small power sources

■ Package Information

Part Number	Package	Body Size
DIO62810	DFN-6	1.2 mm $\times$ 1.2 mm
DIO62820	WLCSP-5	0.77 mm $\times$ 0.93 mm

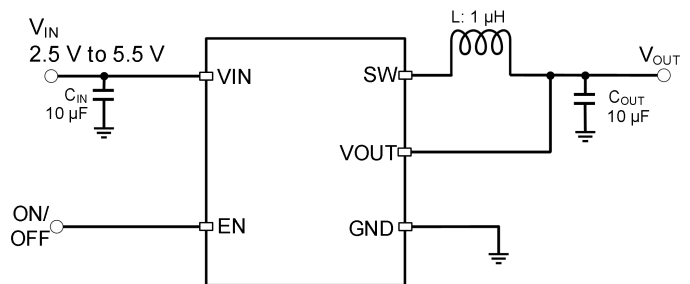
■ Description

The DIO62810/DIO62820 are high-efficiency, high-frequency synchronous step-down DC-DC regulator ICs, capable of delivering up to 5 MHz oscillation frequency, which allows using 1 μ H coil with a size of 2.0 mm $\times$ 1.6 mm and 1.0 mm $\times$ 0.5 mm ceramic capacitors for the input capacitance (C_{IN}) and the output capacitance (C_{OUT}).

The DIO62810 operates in continuous conduction mode under PWM (Pulse Width Modulation) control, and operates at a stable oscillation frequency regardless of load. Under the PWM/PFM automatic switching control, the DIO62820 works in discontinuous conduction mode under light load to reduce the oscillation frequency at light load.

The device adopts high-frequency switch control, which reduces the size of peripheral devices. It is available in the packages of DFN-6 (1.2 mm $\times$ 1.2 mm) and WLCSP-5 (0.77 mm $\times$ 0.93 mm).

■ Simplified Schematic



■ Ordering Information

Ordering Part No.	Top Marking	MSL	RoHS	T _A	Package	
DIO62810ADaaED6	AXYW	1	Green	-40 to 105°C	DFN1.2*1.2-6	Tape & Reel, 5000
DIO62810AEaaED6	BXYW	1	Green	-40 to 105°C	DFN1.2*1.2-6	Tape & Reel, 5000
DIO62810ADaaWL5	WAX	1	Green	-40 to 105°C	WLCSP-5	Tape & Reel, 5000
DIO62810AEaaWL5	WBX	1	Green	-40 to 105°C	WLCSP-5	Tape & Reel, 5000
DIO62810BDaaED6	CXYW	1	Green	-40 to 105°C	DFN1.2*1.2-6	Tape & Reel, 5000
DIO62810BEaaED6	DXYW	1	Green	-40 to 105°C	DFN1.2*1.2-6	Tape & Reel, 5000
DIO62810BDaaWL5	WCX	1	Green	-40 to 105°C	WLCSP-5	Tape & Reel, 5000
DIO62810BEaaWL5	WDX	1	Green	-40 to 105°C	WLCSP-5	Tape & Reel, 5000
DIO62820ADaaED6	EXYW	1	Green	-40 to 105°C	DFN1.2*1.2-6	Tape & Reel, 5000
DIO62820AEaaED6	FXYW	1	Green	-40 to 105°C	DFN1.2*1.2-6	Tape & Reel, 5000
DIO62820ADaaWL5	WEX	1	Green	-40 to 105°C	WLCSP-5	Tape & Reel, 5000
DIO62820AEaaWL5	WFX	1	Green	-40 to 105°C	WLCSP-5	Tape & Reel, 5000
DIO62820BDaaED6	GXYW	1	Green	-40 to 105°C	DFN1.2*1.2-6	Tape & Reel, 5000
DIO62820BEaaED6	HXYW	1	Green	-40 to 105°C	DFN1.2*1.2-6	Tape & Reel, 5000
DIO62820BDaaWL5	WGX	1	Green	-40 to 105°C	WLCSP-5	Tape & Reel, 5000
DIO62820BEaaWL5	WHX	1	Green	-40 to 105°C	WLCSP-5	Tape & Reel, 5000

Part Number	Operation Mode	Type	Oscillation Frequency
DIO62810AD	PWM	A	4 MHz
DIO62810AE			5 MHz
DIO62810BD		B (C _L Auto-Discharge)	4 MHz
DIO62810BE			5 MHz
DIO62820AD	PWM/PFM AUTO	A	4 MHz
DIO62820AE			5 MHz
DIO62820BD		B (C _L Auto-Discharge)	4 MHz
DIO62820BE			5 MHz

Output Voltage Options

Option Code "aa"	09	95	10	05	11	12	13	18
Voltage	0.9 V	0.95 V	1.0 V	1.05 V	1.1 V	1.2 V	1.3 V	1.8 V
Marking Code "X"	9	5	0	6	1	2	3	8

If you encounter any issue in the process of using the device, please contact our customer service at marketing@dioo.com or phone us at (+86)-21-62116882. If you have any improvement suggestions regarding the datasheet, we encourage you to contact our technical writing team at docs@dioo.com. Your feedback is invaluable for us to provide a better user experience.

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1.Pin Assignment and Functions

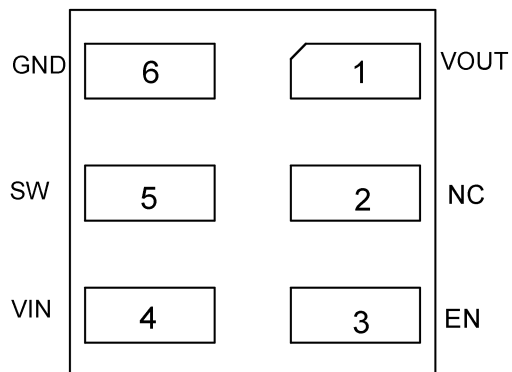


Figure 1. DFN1.2*1.2-6 (Bottom view)

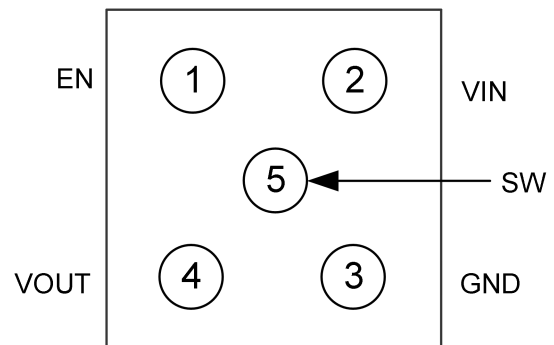


Figure 2. WLCSP-5 (Bottom view)

Name	Description
VOUT	Output voltage monitor
EN	Enable pin. When the EN pin is Low, the device enters stand-by; when the EN pin is High, the device enters active. (Please do not leave the EN pin open.)
VIN	Power input
SW	Switching output
GND	Ground
NC	No connection

2. Absolute Maximum Ratings

Exceeding the maximum ratings listed under Absolute Maximum Ratings when designing is likely to damage the device permanently. Do not design to the maximum limits because long-time exposure to them might impact the device's reliability. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter		Rating	Unit
V_{IN}	VIN pin voltage		-0.3 to 6.2	V
V_{SW}	SW pin voltage		-0.3 to $V_{IN} + 0.3$ or 6.2 ⁽¹⁾	V
V_{OUT}	VOUT pin voltage		-0.3 to $V_{IN} + 0.3$ or 4.0 ⁽²⁾	V
V_{EN}	EN pin voltage		-0.3 to 6.2	V
P_D	Power dissipation	DFN 1.2*1.2-6	760 ⁽³⁾	mW
		WLCSP-5	500 ⁽³⁾	mW
T_J	Junction temperature		-40 to 150	°C
T_{STG}	Storage temperature		-55 to 125	°C

Note:

- (1) The maximum value should be either $V_{IN} + 0.3$ V or 6.2 V in the lowest.
- (2) The maximum value should be either $V_{IN} + 0.3$ V or 4.0 V in the lowest.
- (3) The power dissipation figure shown is PCB mounted and is for reference only.
- (4) All voltages are described based on the GND pin.

3. Recommended Operating Conditions

Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Rating	Unit
V_{IN}	VIN pin voltage	2.5 to 5.5	V
T_A	Operating ambient temperature	-40 to 105	°C

4. ESD Ratings

When a statically-charged person or object touches an electrostatic discharge sensitive device, the electrostatic charge might be drained through sensitive circuitry in the device. If the electrostatic discharge possesses sufficient energy, damage might occur to the device due to localized overheating.

Model	Condition	Value	Unit
Human-body model	ANSI/ESDA/JEDEC JS-001	±2000	V

5. Electrical Characteristics

$V_{IN} = 3.3\text{ V}$, $V_{EN} = 3.3\text{ V}$, $V_{OUT(T)} = \text{nominal value}$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Operating voltage range		2.5		5.5	V
V_{OUT}	Output voltage	$V_{OUT} = 0.9\text{ V}$	0.882	0.900	0.918	V
		$V_{OUT} = 0.95\text{ V}$	0.931	0.950	0.969	V
		$V_{OUT} = 1.0\text{ V}$	0.980	1.000	1.020	V
		$V_{OUT} = 1.05\text{ V}$	1.029	1.050	1.071	V
		$V_{OUT} = 1.1\text{ V}$	1.078	1.100	1.122	V
		$V_{OUT} = 1.2\text{ V}$	1.176	1.200	1.224	V
		$V_{OUT} = 1.3\text{ V}$	1.274	1.300	1.326	V
		$V_{OUT} = 1.8\text{ V}$	1.764	1.800	1.836	V
I_{OUTMAX}	Maximum output current	Connected to external components	600			mA
I_Q	Quiescent current (DIO62810)	$V_{OUT} = 4.0\text{ V}$		590		μA
	Quiescent current (DIO62820)	$V_{OUT} = 4.0\text{ V}$		14		μA
I_{SD}	Shut down current	$V_{IN} = 3.3\text{ V}$, $V_{EN} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$, $V_{SW} = 0\text{ V}$		0.0	0.6	μA
$R_{DS(ON)H}$	Top FET R_{ON} ⁽²⁾	$V_{IN} = 3.3\text{ V}$, $I_{SW} = 300\text{ mA}$ ⁽³⁾		0.30		Ω
$R_{DS(ON)L}$	Bottom FET R_{ON} ⁽²⁾	$V_{IN} = 3.3\text{ V}$, $I_{SW} = 300\text{ mA}$ ⁽³⁾		0.13		Ω
I_{LeakH}	Top FET leakage current	$V_{IN} = 3.3\text{ V}$, $V_{EN} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$, $V_{SW} = 3.3\text{ V}$		0.0	10.0	μA
I_{LeakL}	Bottom FET leakage current	$V_{IN} = 3.3\text{ V}$, $V_{EN} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$, $V_{SW} = 0\text{ V}$		0.0	0.3	μA
I_{LIMH}	Current limit ⁽⁴⁾	$V_{IN} = 3.3\text{ V}$, $V_{OUT} = 0\text{ V}$, I_{SW} until SW pin oscillates		1000		mA

t_{ON}	ON time	When connected to external components, $I_{OUT} = 1 \text{ mA}$, $f_{OSC} = 5 \text{ MHz}$	$V_{IN} = 2.9 \text{ V}$, $V_{OUT} = 0.9 \text{ V}$		92		ns
			$V_{IN} = 2.95 \text{ V}$, $V_{OUT} = 0.95 \text{ V}$		94		ns
			$V_{IN} = 3.0 \text{ V}$, $V_{OUT} = 1.0 \text{ V}$		97		ns
			$V_{IN} = 3.05 \text{ V}$, $V_{OUT} = 1.05 \text{ V}$		99		ns
			$V_{IN} = 3.1 \text{ V}$, $V_{OUT} = 1.1 \text{ V}$		102		ns
			$V_{IN} = 3.2 \text{ V}$, $V_{OUT} = 1.2 \text{ V}$		107		ns
			$V_{IN} = 3.3 \text{ V}$, $V_{OUT} = 1.3 \text{ V}$		112		ns
			$V_{IN} = 3.8 \text{ V}$, $V_{OUT} = 1.8 \text{ V}$		137		ns
V_{ENH}	EN rising voltage	$V_{IN} = 3.3 \text{ V}$, $V_{OUT} = 0 \text{ V}$, V_{EN} voltage which SW pin holding "H" level ⁽⁵⁾	1.20		5.50		V
V_{ENL}	EN falling voltage	$V_{IN} = 3.3 \text{ V}$, $V_{OUT} = 0 \text{ V}$, V_{EN} voltage which SW pin holding "L" level ⁽⁵⁾	GND		0.30		V
I_{ENH}	EN rising current	$V_{EN} = 3.3 \text{ V}$, $V_{OUT} = 3.3 \text{ V}$	-0.1	0.0	0.1		μA
I_{ENL}	EN falling current	$V_{IN} = 3.3 \text{ V}$, $V_{EN} = 0 \text{ V}$, $V_{OUT} = 0 \text{ V}$	-0.1	0.0	0.1		μA
f_{OSC}	Oscillator frequency	$V_{IN} = 3.3 \text{ V}$, $I_{OUT} = 600 \text{ mA}$ (only for DIO62820AE, DIO62820BE, DIO62810AE, and DIO62810BE)		5			MHz
V_{UVLO}	UVLO voltage		2.2	2.3	2.4		V
V_{hys}	UVLO hysteresis			300			mV
t_{SS}	Soft-start time	$V_{IN} = 3.3 \text{ V}$, $V_{EN} = 0 \text{ V} \rightarrow 3.3 \text{ V}$, $V_{OUT} = V_{OUT(T)} \times 0.9$. After "H" is fed to EN, the time by when clocks are generated at SW pin.		300			μs
R_{DIS}	C_L discharge resistance (B type)	$V_{EN} = 0 \text{ V}$, $V_{OUT} = 1.0 \text{ V}$		145			Ω
T_{SD}	Thermal shutdown threshold			150			$^{\circ}\text{C}$
T_{SD_hys}	Thermal shutdown hysteresis			30			$^{\circ}\text{C}$

Note:

- (1) For PWM control.
- (2) Design value for WLCSP-5.
- (3) $R_{DS(ON)H} = (V_{IN} - \text{SW pin measurement voltage}) / 300 \text{ mA}$, $R_{DS(ON)L} = \text{SW pin measurement voltage} / 300 \text{ mA}$.
- (4) Current limit denotes the level of detection at peak of coil current.
- (5) "H" = $V_{IN} - 1.2 \text{ V} \sim V_{IN}$, "L" = $-0.1 \text{ V} \sim 0.1 \text{ V}$.
- (6) Specifications subject to change without notice.

6. Typical Performance Characteristic

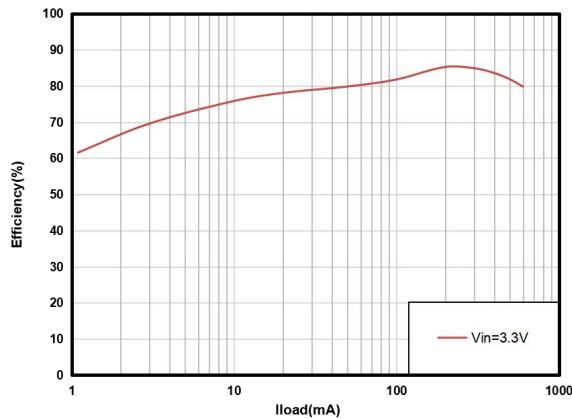


Figure 3. Efficiency vs. I_{load} at $V_{OUT} = 0.9\text{ V}$

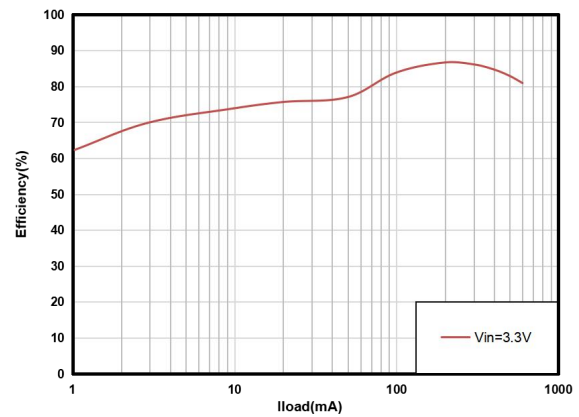


Figure 4. Efficiency vs. I_{load} at $V_{OUT} = 1.0\text{ V}$

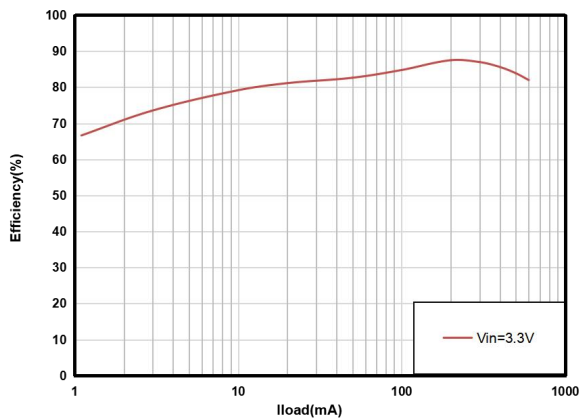


Figure 5. Efficiency vs. I_{load} at $V_{OUT} = 1.1\text{ V}$

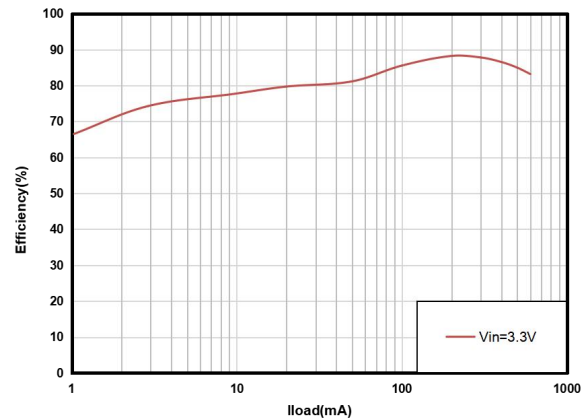


Figure 6. Efficiency vs. I_{load} at $V_{OUT} = 1.2\text{ V}$

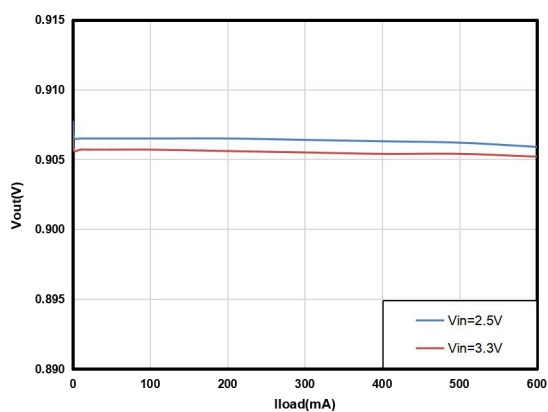


Figure 7. Output voltage vs. Output current

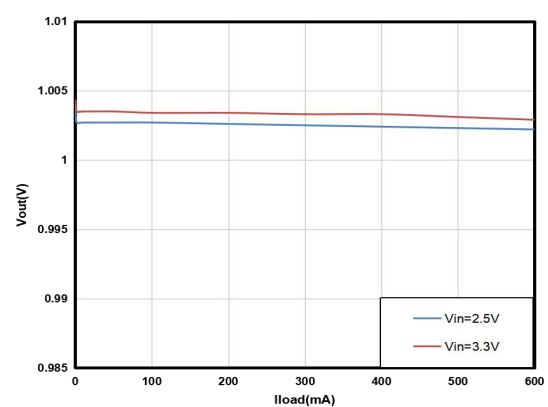


Figure 8. Output voltage vs. Output current

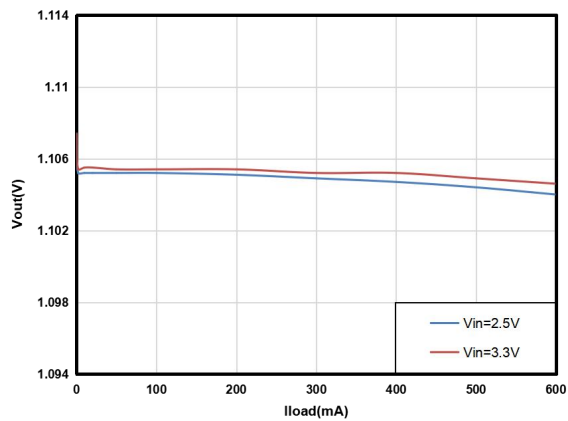


Figure 9. Output voltage vs. Output current

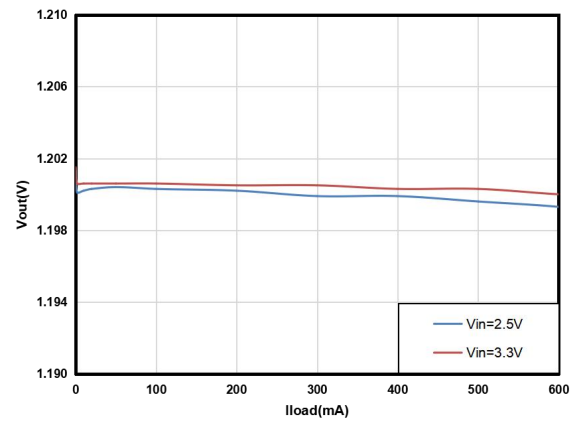


Figure 10. Output voltage vs. Output current

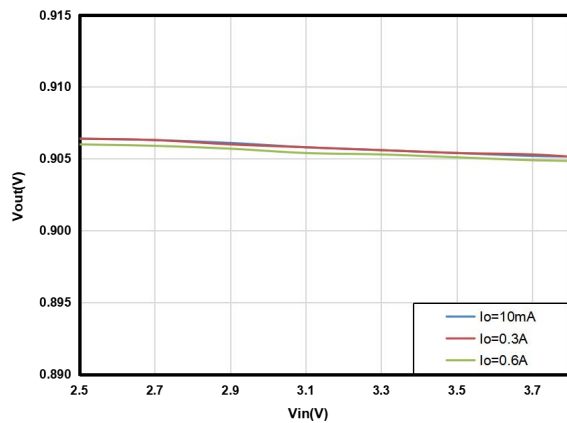


Figure 11. Output voltage vs. Input voltage

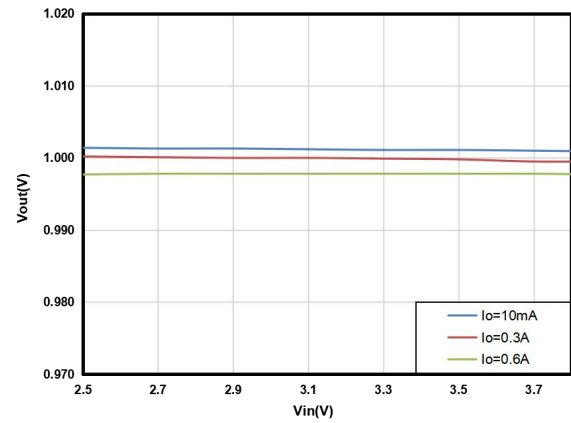


Figure 12. Output voltage vs. Input voltage

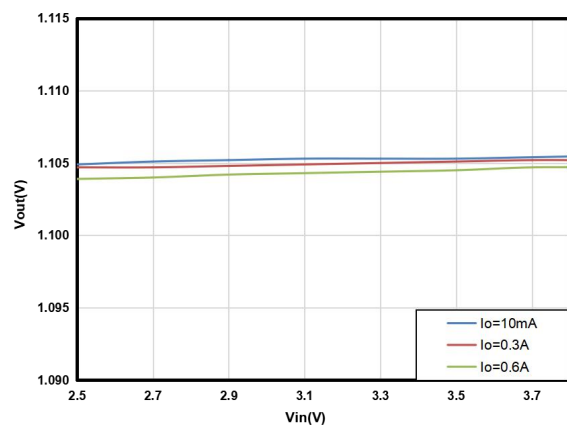


Figure 13. Output voltage vs. Input voltage

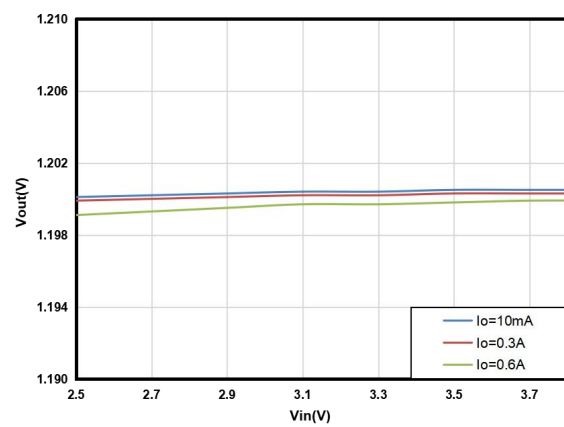


Figure 14. Output voltage vs. Input voltage

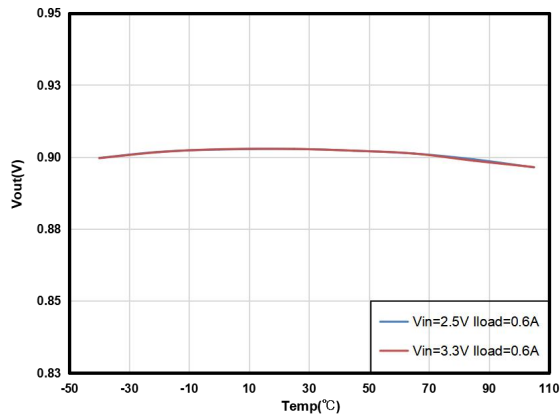


Figure 15. Output voltage vs. Ambient temperature

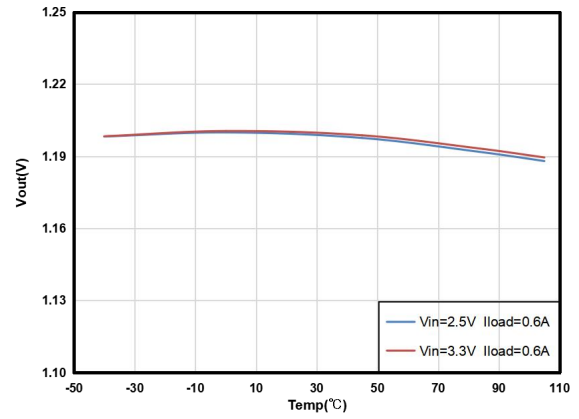


Figure 16. Output voltage vs. Ambient temperature

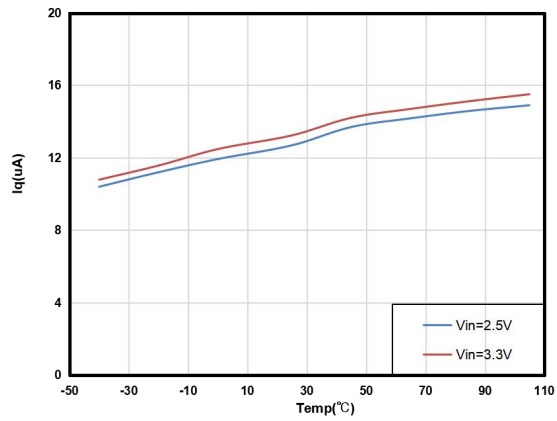


Figure 17. Quiescent current vs. Ambient temperature

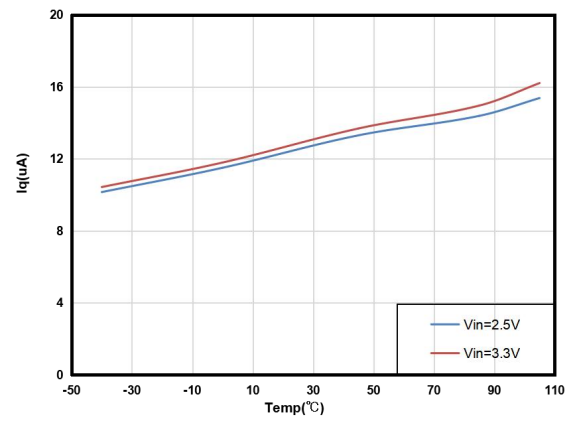


Figure 18. Quiescent current vs. Ambient temperature

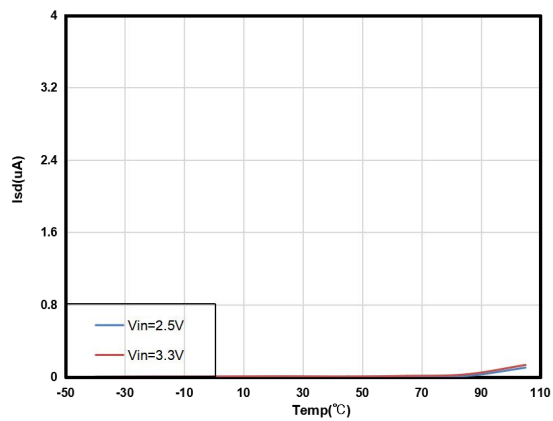


Figure 19. Shut down current vs. Ambient temperature

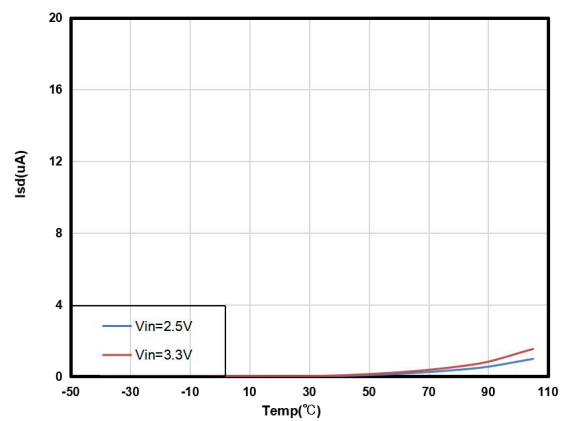


Figure 20. Shut down current vs. Ambient temperature

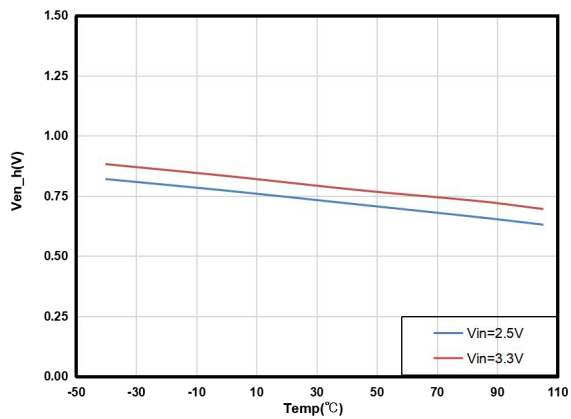


Figure 21. EN voltage vs. Ambient temperature

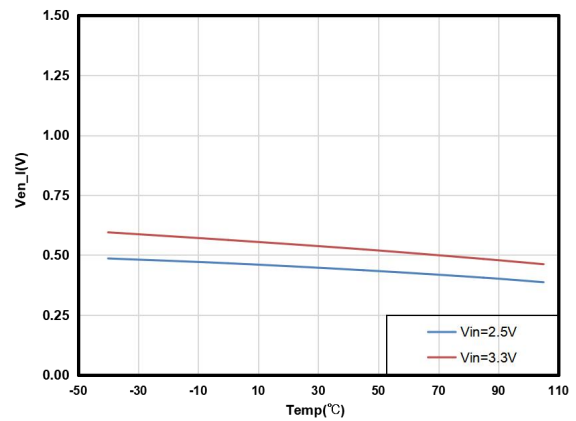


Figure 22. EN voltage vs. Ambient temperature

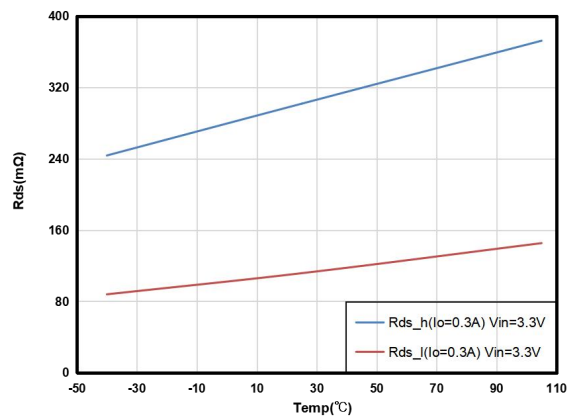
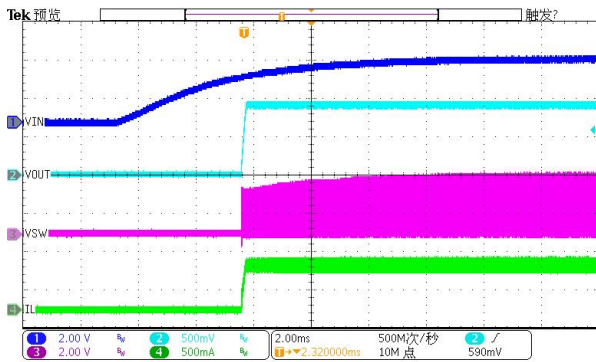


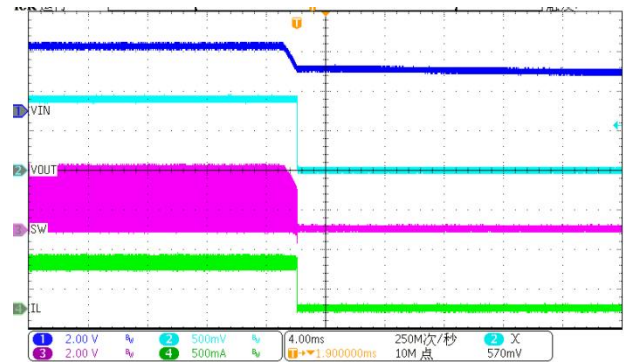
Figure 23. Driver ON resistance vs. Ambient temperature

$V_{IN} = 3.3\text{ V}$, $V_{OUT} = 0.9\text{ V}$, $L = 1\text{ }\mu\text{H}$, $C_{IN} = 10\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$, unless otherwise specified.



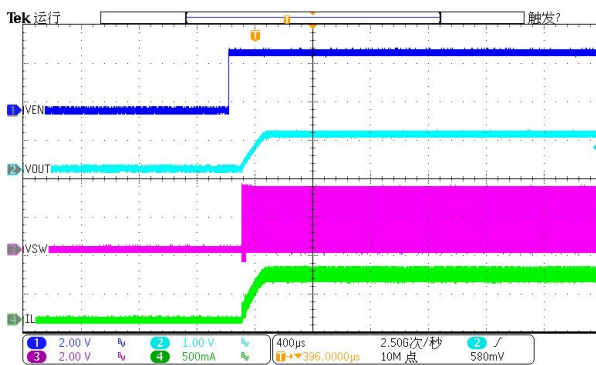
$V_{IN} = 3.3\text{ V}$, $V_{OUT} = 0.9\text{ V}$ with 0.6 A load

Figure 24. V_{IN} start



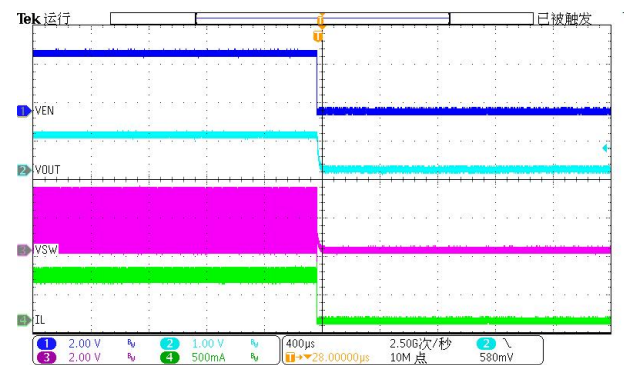
$V_{IN} = 3.3\text{ V}$, $V_{OUT} = 0.9\text{ V}$ with 0.6 A load

Figure 25. V_{IN} drop



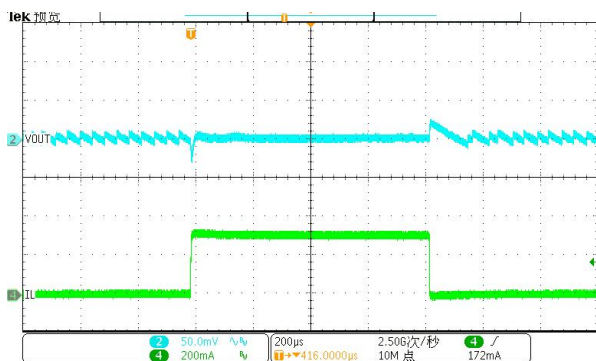
$V_{IN} = 3.3\text{ V}$, $V_{OUT} = 0.9\text{ V}$ with 0.6 A load

Figure 26. V_{EN} start



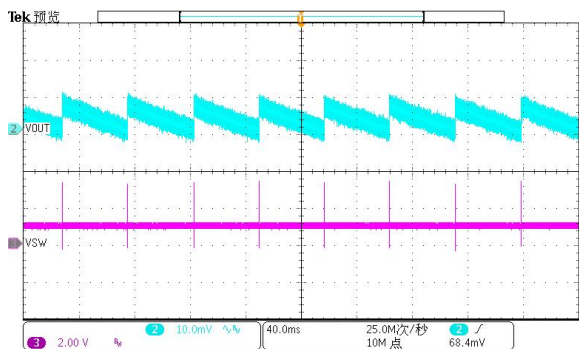
$V_{IN} = 3.3\text{ V}$, $V_{OUT} = 0.9\text{ V}$ with 0.6 A load

Figure 27. V_{EN} drop



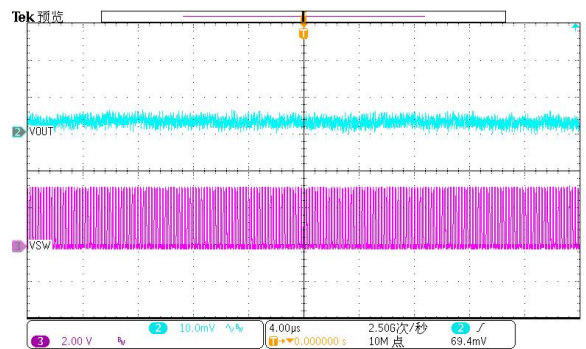
$V_{IN} = 3.3\text{ V}$, $V_{OUT} = 0.9\text{ V}$, $0.001\text{ A} \sim 0.3\text{ A}$

Figure 28. Load transient



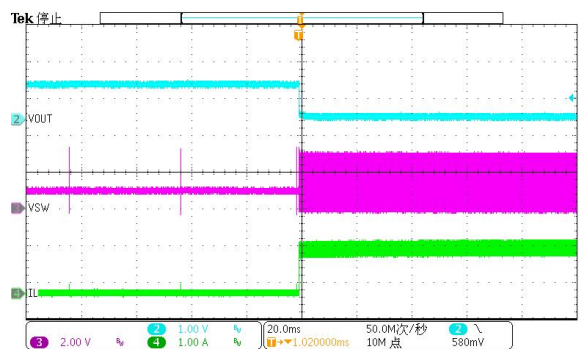
$V_{IN} = 3.3\text{ V}$, $V_{OUT} = 0.9\text{ V}$ with 0 A load

Figure 29. Ripple



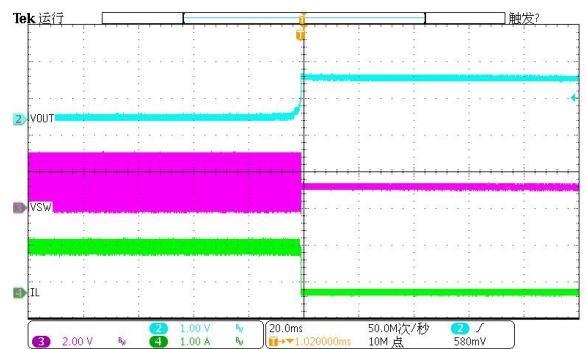
$V_{IN} = 3.3\text{ V}$, $V_{OUT} = 0.9\text{ V}$ with 0.6 A load

Figure 30. Ripple



$V_{IN} = 3.3\text{ V}$, $V_{OUT} = 0.9\text{ V}$, 0 A load $\rightarrow$ short

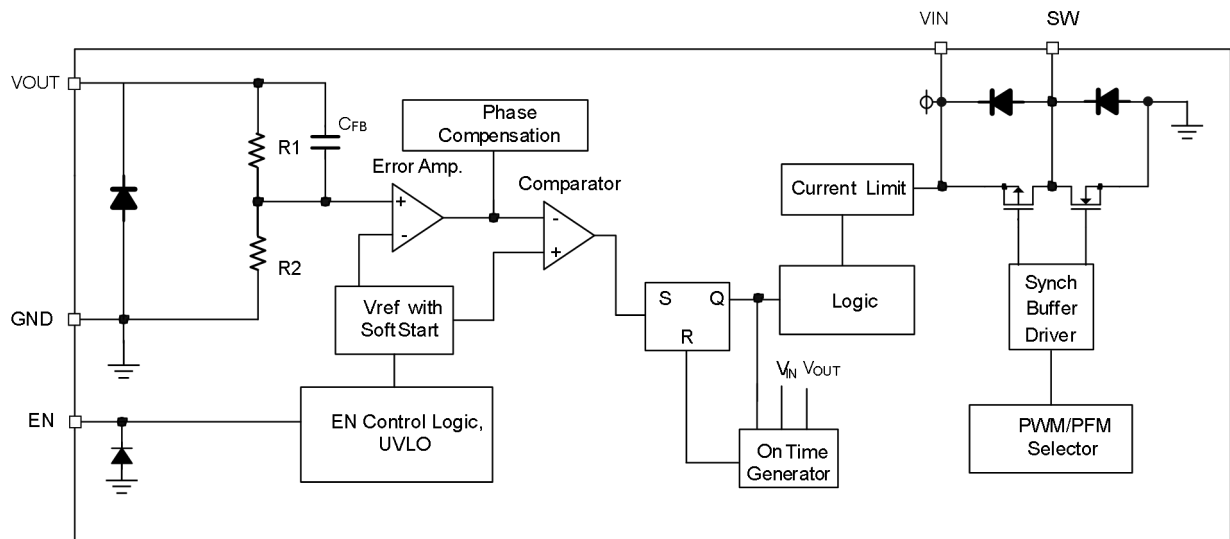
Figure 31. Short circuit protection



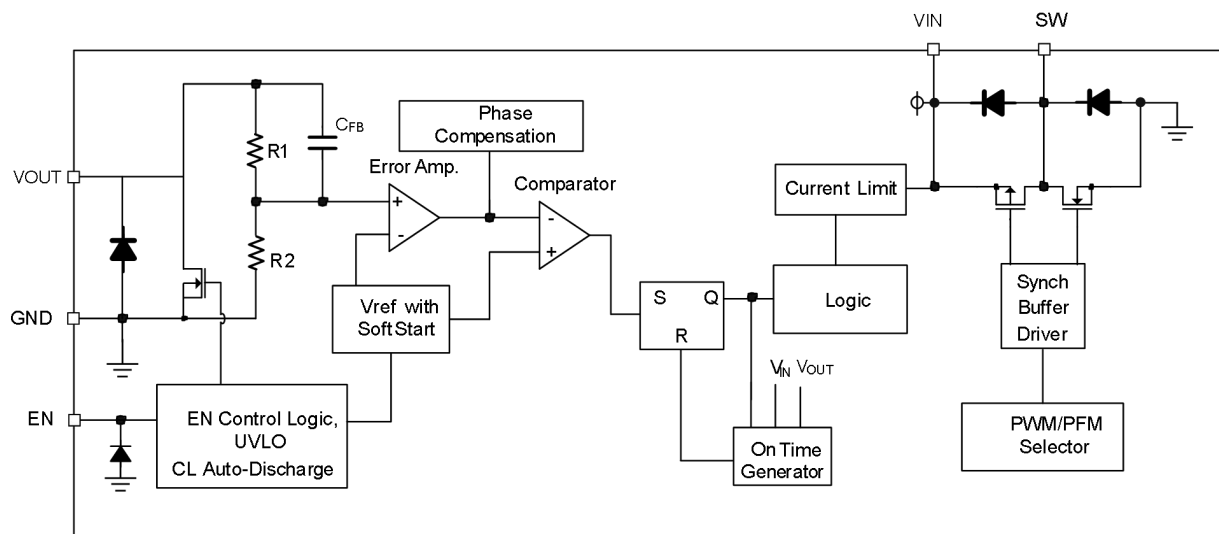
$V_{IN} = 3.3\text{ V}$, $V_{OUT} = 0.9\text{ V}$, short $\rightarrow$ 0 A load

Figure 32. Short circuit recovery

7. Block Diagram



DIO62810/DIO62820 Type A block diagram



DIO62810/DIO62820 Type B block diagram

8. Function Description

8.1. Overview

The DIO62810/DIO62820 are high-efficiency, high-frequency synchronous step-down DC-DC regulator ICs, capable of delivering up to 5 MHz oscillation frequency.

The DIO62810 operates in continuous conduction mode under PWM(Pulse Width Modulation) control, and operates at a stable oscillation frequency regardless of load. Under the PWM/PFM automatic switching control, the DIO62820 operates in discontinuous conduction mode under light load to reduce the oscillation frequency at light load.

The control method is a Constant On-Time Transient High-Speed Circuit Structure, which is characterized by an on-time control method and fast transient response with low ripple voltage. In this control, the ON time (t_{ON}) is generated according to the input voltage and output voltage, and the PMOS driver T_r is turned on. The time setting is as follows.

$$t_{ON} = (V_{OUT} / V_{IN}) \times 250 \text{ ns} \quad (\text{For IC with 4 MHz}) \quad (1)$$

$$t_{ON} = (V_{OUT} / V_{IN}) \times 200 \text{ ns} \quad (\text{For IC with 5 MHz}) \quad (2)$$

The off time (t_{OFF}) is controlled by comparing the output voltage and the reference voltage with the error amplifier and the comparator. Specifically, the reference voltage and a voltage that is obtained by dividing the output voltage with R1 and R2 are compared using the error amplifier. The output of the error amplifier undergoes a phase compensation, and it is sent to the comparator. In the comparator, the output of the error amplifier is compared with the reference voltage, and when it falls below the reference voltage, the SR latch is set and it becomes the ON Cycle again.

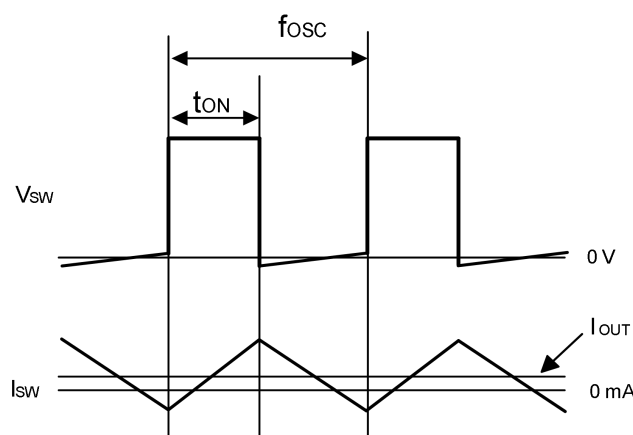


Figure 33. Continuous conduction mode waveform

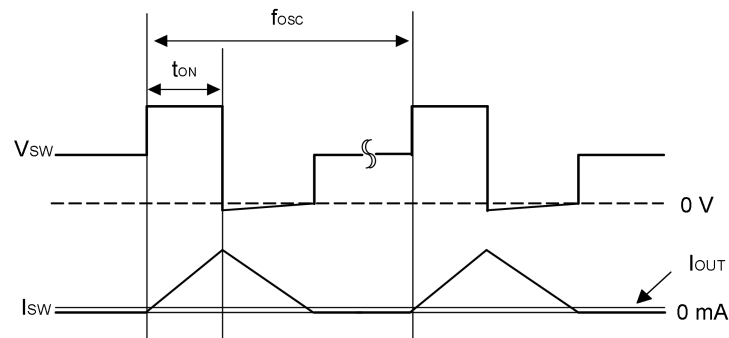


Figure 34. Discontinuous conduction mode waveform

In the phase compensation circuit, the frequency characteristic of the error amplifier is optimized, and ramp waves which are similar to ripple voltages generated at the output are generated to modulate the output signal of the error amplifier. This enables a stable feedback system to be obtained even when a low ESR capacitor such as a ceramic capacitor is used. This also enables a fast transient response and a stable output voltage.

8.2. EN function

Normal operation begins when the EN pin is high. After the output voltage is raised by the soft-start function, and when the EN pin is low, it enters stand-by and the current consumption is suppressed to 0 μ A (typ). Additionally, the PMOS driver and NMOS driver are turned off.

8.3. Soft start

The DIO62810/DIO62820 employs a soft start (SS) mechanism to ensure smooth output ramping during power-up. When the EN goes high, an internal soft-start circuitry controls the output voltage during start-up. The reference voltage which is connected to the error amplifier increases linearly during the soft start period. As a result, the output voltage increases in proportion to the increase of the reference voltage. This avoids excessive inrush current and raises the output voltage smoothly.

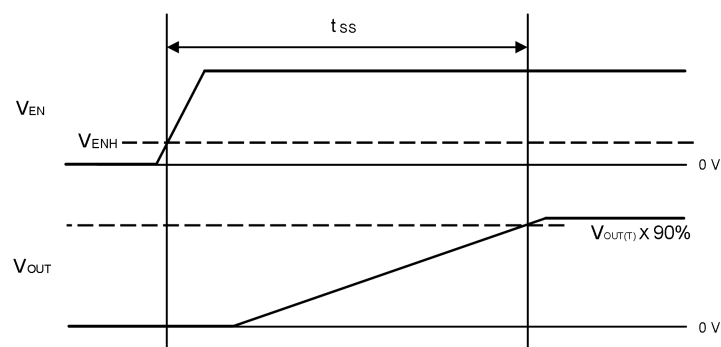


Figure 35. Soft-start

8.4. Undervoltage lockout

When the V_{IN} voltage becomes 2.0 V (typ.) or less, the UVLO function operates to forcibly turn off the PMOS driver to prevent erroneous pulse output due to the operation instability of the internal circuit. When the V_{IN} voltage becomes 2.3 V (typ.) or more, the UVLO function is cancelled. After the UVLO function is cancelled, the output voltage rises with the soft start function, and then the normal operation is performed. Moreover, during the UVLO operation, the internal circuit is still operating, because the UVLO stop is different from the stand-by mode, it just stops the switch operation.

8.5. Current limit

The current limit function monitors and limits the current flowing through the PMOS driver and NMOS driver. The overcurrent operation is as follows. Firstly, when the current flowing through the PMOS driver increases and reaches the current limit value $I_{LIMH} = 1000$ mA (typ.), the current limit state is set and the PMOS driver is forcibly turned off. Secondly, after turning off the PMOS driver through the current limit function, the NMOS driver will turn on. The PMOS driver is prohibited to turn on until the current value flowing through the NMOS driver drops to $I_{LIML} = 800$ mA (typ.). Repeat operations 1 and 2 during the current limit state. When the current limit state is canceled, it automatically returns to normal operation.

8.6. C_L discharge function

Type B can quickly discharge the output capacitor through the internal N-channel MOS transistor connected to the VOUT pin, to prevent malfunction of application due to residual charge remaining in the output capacitor during stand-by. The output voltage during discharging can be calculated by the following equation.

$$V = V_{OUT(T)} \times e^{-t/\tau} \quad (3)$$

$$t = \tau \ln (V_{OUT(T)} / V) \quad (4)$$

where

V : output voltage during discharge

$V_{OUT(T)}$: output voltage (nominal value)

t : discharge time

C_L : effective capacitance of output capacitor

R_{DCHG} : C_L auto-discharge resistance

$\tau : C_L \times R_{DCHG}$

9. Application Information

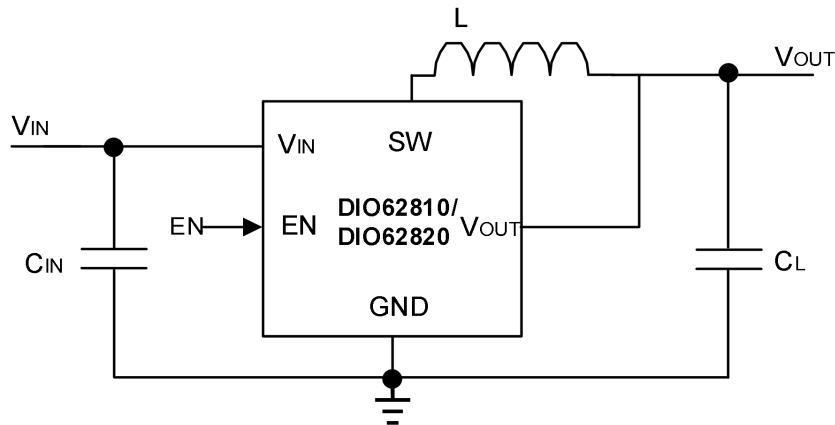


Figure 36. Typical application

Table 1. Typical examples

	Manufacturer	Product Number	Value	Size: L×W×T (Unit: mm)
L	Cyntec	HTTK20161T-1R0MSR	1.0 μ H	2.0 × 1.6 × 1.0
C _{IN} ⁽¹⁾	murata	GRM155R60J106ME44D	10 μ F / 6.3 V	1.0 × 0.5 × 0.5
C _L	murata	GRM155R60J106ME44D	10 μ F / 6.3 V	1.0 × 0.5 × 0.5

Note:

(1) Increase a by-pass capacitor when it's needed.

10. Layout Guidelines

The layout design of the DIO62810/DIO62820 regulator is relatively simple. For the best efficiency and minimum noise issues, place the following components close to the IC: C_{IN}, C_L, L.

1. Maximize the PCB copper area connected to the GND pin to achieve the best thermal and noise performance. If the board space allows, a ground plane is highly desirable.
2. C_{IN} must be close to VIN and GND pins. The loop area formed by C_{IN} and GND must be minimized.
3. The PCB copper area associated with the SW pin must be minimized to avoid the potential noise issue.

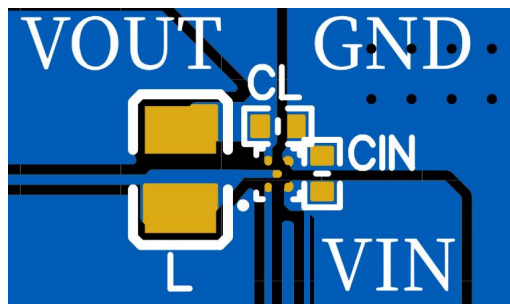


Figure 37. PCB layout guide

11. Board Layout

This section provides the DIO62810/DIO62820 EVM board layout and illustrations from Figure 38 to Figure 40.

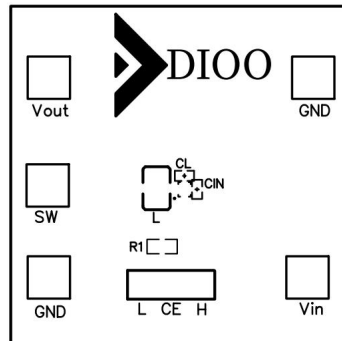


Figure 38. Top assembly

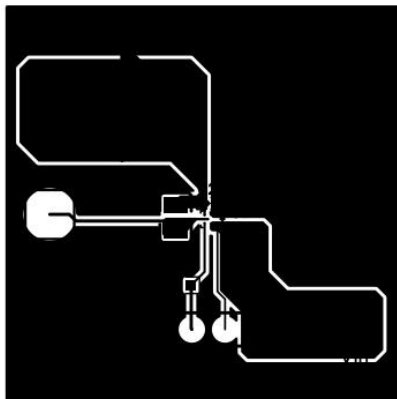


Figure 39. Top layer

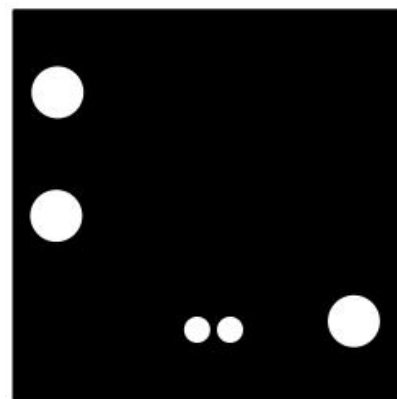
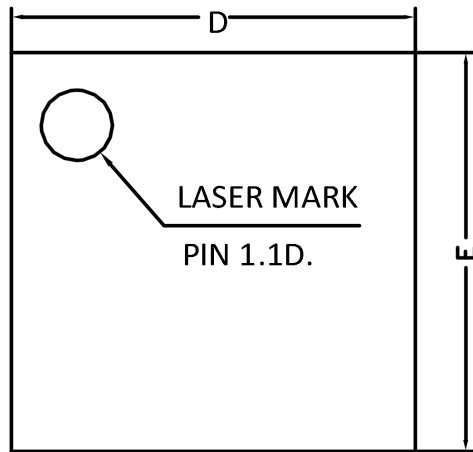


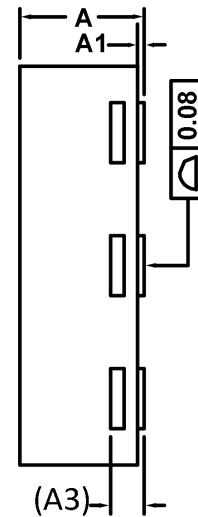
Figure 40. Bottom layer

12. Physical Dimensions

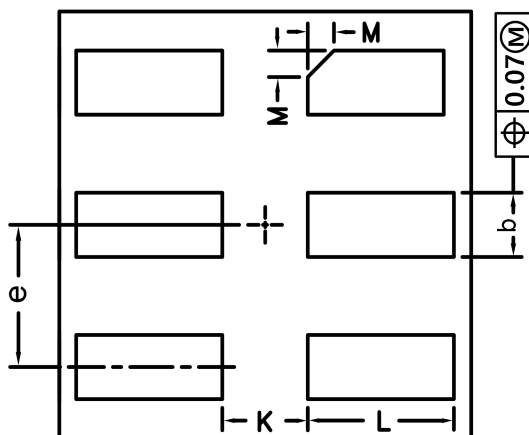
12.1. DFN1.2*1.2-6



TOP VIEW



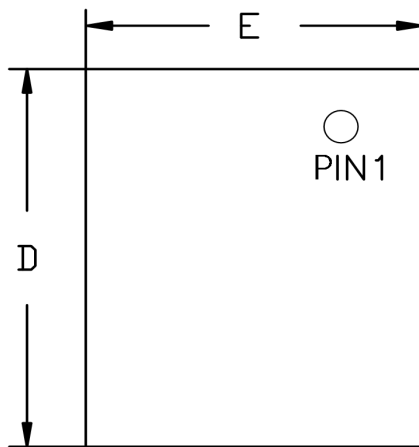
SIDE VIEW



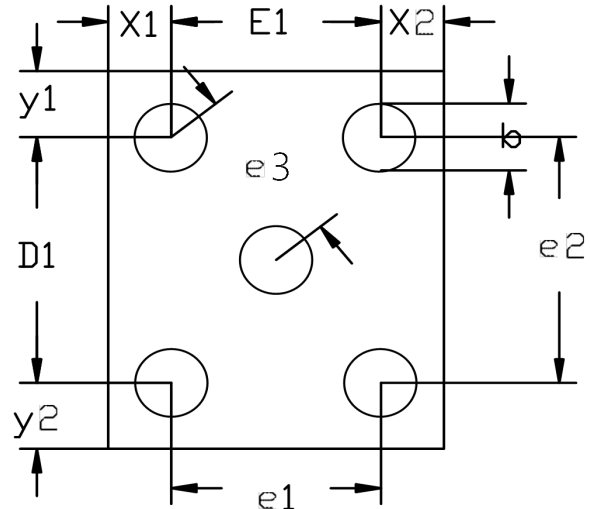
BOTTOM VIEW

Common Dimensions (Units of measure = Millimeter)			
Symbol	Min	Nom	Max
A	0.34	0.37	0.40
A1	0.00	0.02	0.05
A3	0.10 REF		
b	0.13	0.18	0.23
D	1.15	1.20	1.25
E	1.15	1.20	1.25
e	0.35	0.40	0.45
K	0.25 REF		
L	0.425 REF		
M	0.075 REF		

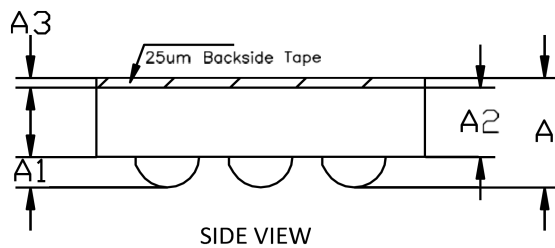
12.2. WLCSP-5



TOP VIEW
(MARK SIDE)



BOTTOM VIEW
(BALL SIDE)



SIDE VIEW

Common Dimensions (Units of measure = Millimeter)			
Symbol	Min	Nom	Max
A	0.260	0.295	0.330
A1	0.060	0.070	0.080
A2	0.175	0.200	0.225
A3	0.025 REF		
D	0.900	0.930	0.960
D1	0.625 BSC		
E	0.740	0.770	0.800
E1	0.500 BSC		
b	0.150	0.170	0.190
e1	0.500 BSC		
e2	0.625 BSC		
e3	0.400 BSC		
x1	0.150 REF		
x2	0.150 REF		
y1	0.1675 REF		
y2	0.1675 REF		

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