

DIO69319

High-Efficiency 3 A, 24 V Input Synchronous Step-Down Converter

Description

The DIO69319 is a high-efficiency, high-frequency synchronous step-down DC-DC regulator ICs capable of delivering up to 3 A output currents. The DIO69319 family operates over a wide input voltage range from 4.5 V to 24 V and integrates the main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The pure COT architecture with pseudo-fixed switching frequency operation provides a fast transient response and eases loop stabilization. Protection features include over-current protection and thermal shutdown.

The DIO69319 always operates in continuous conduction mode, which reduces the output ripple voltage under light load compared to discontinuous conduction mode. The DIO69319 is stable, with an extremely low ESR and high capacitance.

The DIO69319 requires a minimal number of readily-available, standard, external components and is available in a space-saving TSOT23-6 package.

Features

- Low $R_{DS(ON)}$ for internal switches (top/bottom)
80 m Ω /40 m Ω , 3.0 A
- 4.5 V ~ 24 V input voltage range
- High-efficiency synchronous-mode
- Internal soft-start limits the inrush current
- Over-current protection
- Output short circuit protection with hiccup mode
- Thermal shutdown
- Available in TSOT23-6 package

Applications

- Portable navigation devices
- Portable navigation devices
- Set top boxes
- Portable TVs
- LCD TVs

Ordering Information

Part Number	Top Marking	RoHS	T _A	Package	
DIO69319TST6	W319	Green	-40 to 85°C	TSOT23-6	Tape & Reel, 3000

If you encounter any issue in the process of using the device, please contact our customer service at marketing@dioo.com or phone us at (+86)-21-62116882. If you have any improvement suggestions regarding the datasheet, we encourage you to contact our technical writing team at docs@dioo.com. Your feedback is invaluable for us to provide a better user experience.

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1. Pin Assignment and Functions

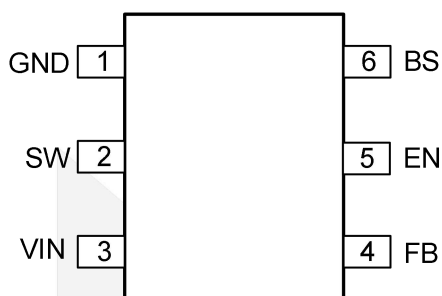


Figure 1. TSOT23-6 (Top view)

Pin Name	Description
GND	Power ground
SW	Inductor pin. Connect this pin to the switching node of inductor.
V _{IN}	Power input
FB	Output feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 19. DIO69319 1.05 V/3 A reference design) to program the output voltage: $V_{OUT} = 0.765 \times (1 + R1 / R2)$.
EN	Enable control. Pull high to turn on. Do not float.
BS	Bootstrap. Connect a capacitor and a resistor between SW and BS pins to form a floating supply across the high-side switch driver. Recommend to use 0.1 μ F BS capacitor.

2. Absolute Maximum Ratings

Exceeding the maximum ratings listed under Absolute Maximum Ratings when designing is likely to damage the device permanently. Do not design to the maximum limits because long-time exposure to them might impact the device's reliability. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Rating	Unit
V _{CC}	Supply voltage (V ₊ – V ₋)	28	V
	EN, SW voltage	V _{IN} + 0.3	V
	FB voltage	6	V
	BS voltage	SW + 6	V
T _{STG}	Storage temperature range	-65 to 150	°C
T _J	Junction temperature range	150	°C
T _L	Lead temperature range	260	°C

3. Recommended Operating Condition

Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Ratings	Unit
V _{CC}	Supply voltage	4.5 to 24	V
T _J	Junction temperature range	-40 to 125	°C
T _A	Ambient temperature range	-40 to 85	°C

4. ESD Ratings

When a statically-charged person or object touches an electrostatic discharge sensitive device, the electrostatic charge might be drained through sensitive circuitry in the device. If the electrostatic discharge possesses sufficient energy, damage might occur to the device due to localized overheating.

Model	Metric	Value	Unit
Human-body model (HBM)	ANSI/ESDA/JEDEC JS-001	±2000	V
Charged device model (CDM)	ANSI/ESDA/JEDEC JS-002	±500	V

5. Thermal Considerations

The thermal resistance determines the heat insulation property of a material. The higher the thermal resistance is, the lower the heat loss. Accumulation of heat energy degrades the performance of semiconductor components.

Symbol	Parameter	Value	Unit
R _{θJA}	Junction-to-ambient thermal resistance	110	°C/W
R _{θJC}	Junction-to-case thermal resistance	42.2	°C/W

6. Electrical Characteristics

The values are obtained under these conditions unless otherwise specified: $V_{IN} = 12\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $L = 1.5\text{ }\mu\text{H}$, $C_{OUT} = 47\text{ }\mu\text{F}$, $T_J = -40^\circ\text{C}$ to 125°C , $I_{OUT} = 1\text{ A}$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage range		4.5		24	V
I_Q	Quiescent current	$I_{OUT} = 0$, $V_{FB} = V_{REF} \times 105\%$		150		μA
I_{SHDN}	Shutdown current	$EN = 0$		10	15	μA
V_{REF}	Feedback reference voltage	$T_J = -40^\circ\text{C}$ to 125°C	0.745	0.765	0.780	V
		$T_J = 0^\circ\text{C}$ to 125°C	0.750	0.765	0.780	
I_{FB}	FB input current	$V_{FB} = 3.3\text{ V}$	-50		50	nA
$R_{DS(ON)}^{(1)}$	Top FET R_{ON}	$T_A = 25^\circ\text{C}$		80		m Ω
$R_{DS(ON)}^{(1)}$	Bottom FET R_{ON}	$T_A = 25^\circ\text{C}$		40		m Ω
$I_{LIM}^{(1)}$	Low side power FET current limit		3.3	4	4.7	A
V_{ENH}	EN rising threshold		1.5			V
V_{ENL}	EN falling threshold				0.4	V
V_{UVLO}	V_{IN} under-voltage unlock threshold, rising			4.15	4.45	V
	Hysteresis V_{IN} voltage			0.4		V
f_{SW}	Switching frequency	$V_{IN} = 12\text{ V}$; $V_{OUT} = 3.3\text{ V}$; Load = 3 A	600	700	800	kHz
	Min ON time			140		ns
	Min OFF time			90	140	ns
	Maximum duty cycle			90%		
$t_{SS}^{(1)}$	Soft start time			1		ms
$t_{SD}^{(1)}$	Thermal shutdown temperature			148		$^\circ\text{C}$
$t_{HYS}^{(1)}$	Thermal shutdown hysteresis			20		$^\circ\text{C}$

Note:

- (1) Guaranteed by design.
- (2) Specifications subject to change without notice.

7. Typical Performance Characteristics

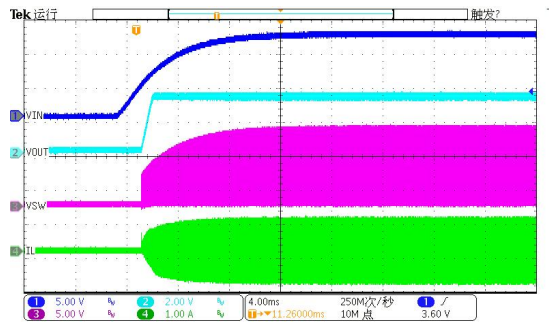

 $V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, No load

Figure 2. Start up from V_{IN}

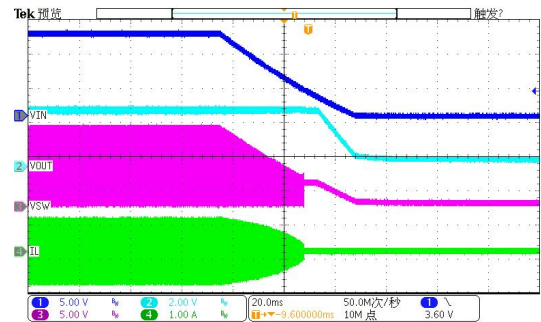

 $V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, No load

Figure 3. Shut down from V_{IN}

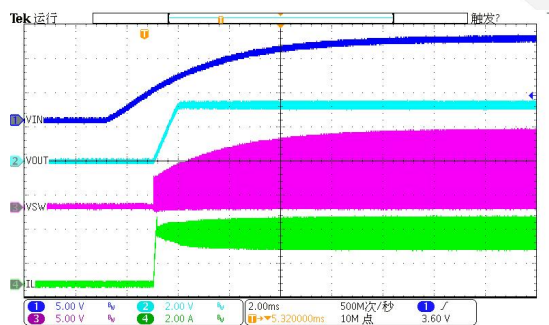

 $V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, Load = 3 A

Figure 4. Start up from V_{IN}

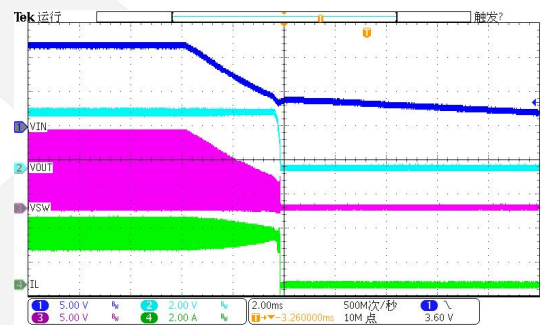

 $V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, Load = 3 A

Figure 5. Shut down from V_{IN}

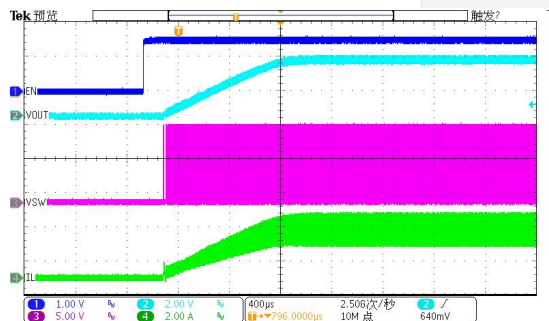

 $V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, Load = 1.1 Ω

Figure 6. Start up from Enable

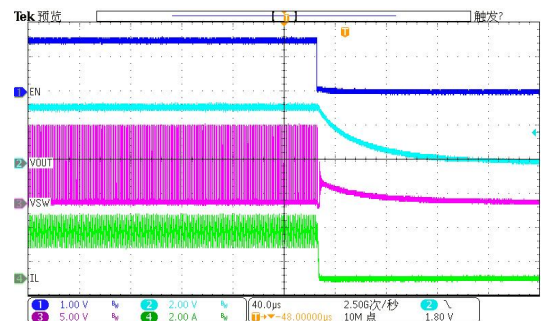

 $V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, Load = 1.1 Ω

Figure 7. Shut down from Enable

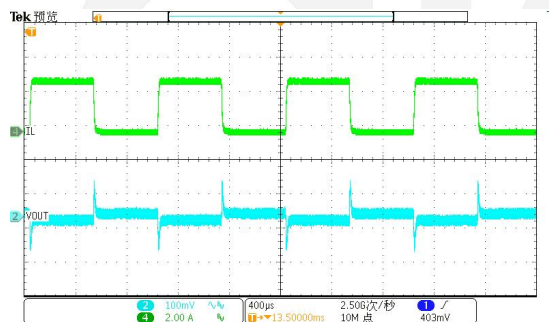

 $V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, Load = 10 mA ~ 3 A

Figure 8. Load transient

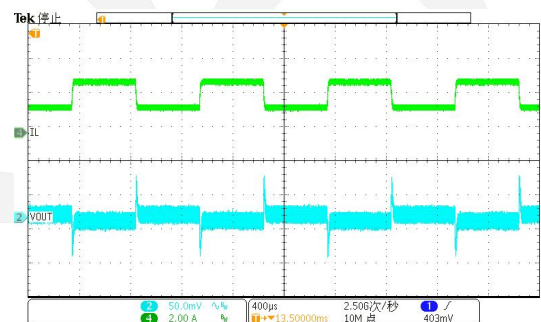

 $V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, Load = 1.5 ~ 3 A

Figure 9. Load transient

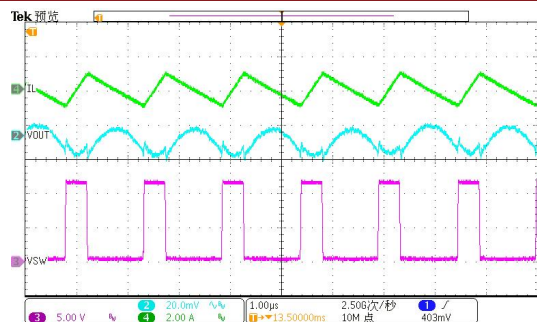

 $V_{IN} = 12\text{ V}, V_{OUT} = 3.3\text{ V}, \text{Load} = 0\text{ A}$

Figure 10. Ripple

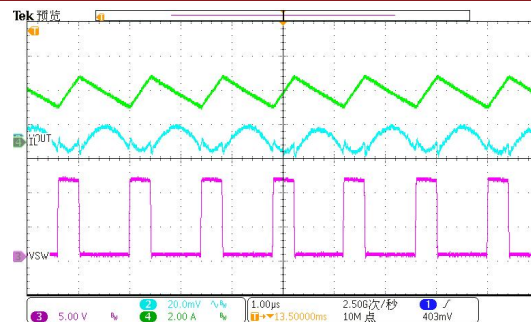

 $V_{IN} = 12\text{ V}, V_{OUT} = 3.3\text{ V}, \text{Load} = 3\text{ A}$

Figure 11. Ripple

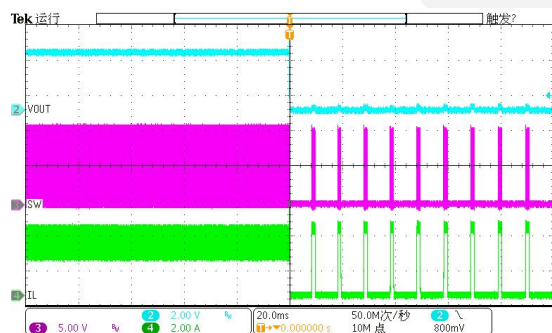

 $V_{IN} = 12\text{ V}, V_{OUT} = 3.3\text{ V}, \text{Load} = 3\text{ A}$

Figure 12. Short circuit protection

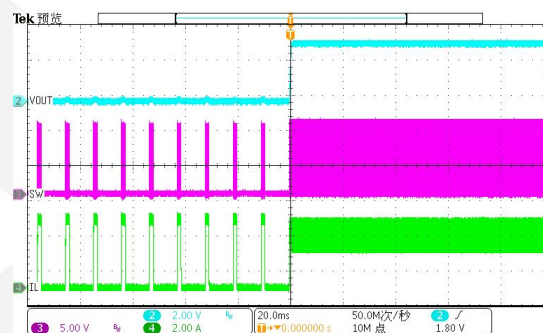

 $V_{IN} = 12\text{ V}, V_{OUT} = 3.3\text{ V}, \text{Load} = 3\text{ A}$

Figure 13. Short circuit recovery

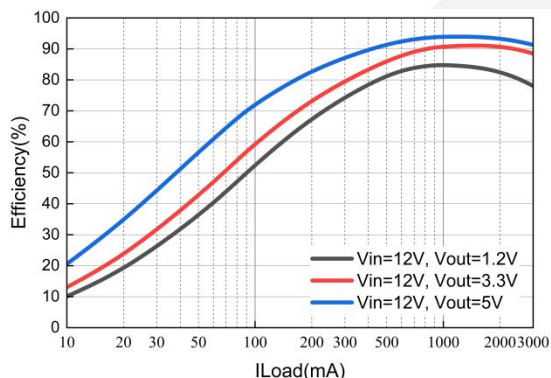


Figure 14. Efficiency vs. Output current

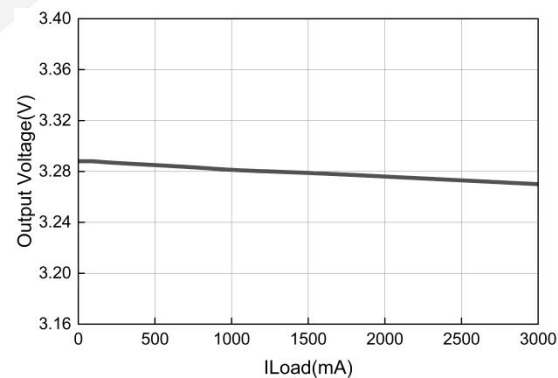


Figure 15. Output voltage vs. Output current

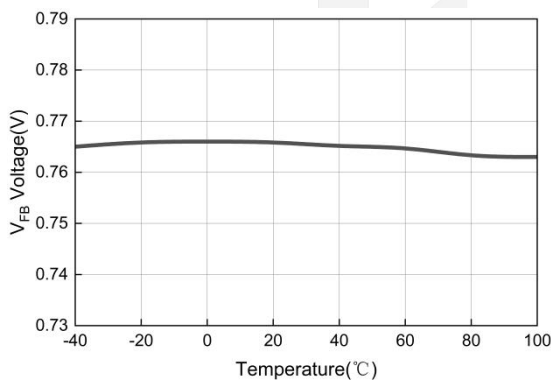


Figure 16. FB voltage vs. Temperature

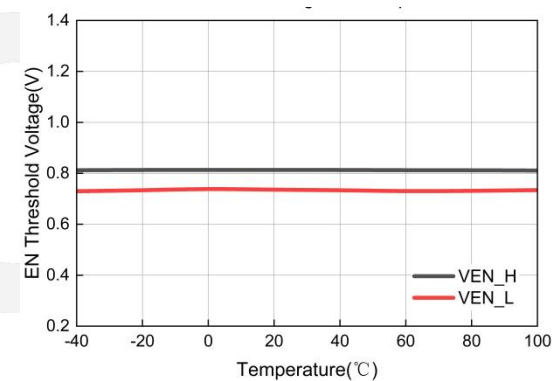


Figure 17. EN threshold voltage vs. Temperature

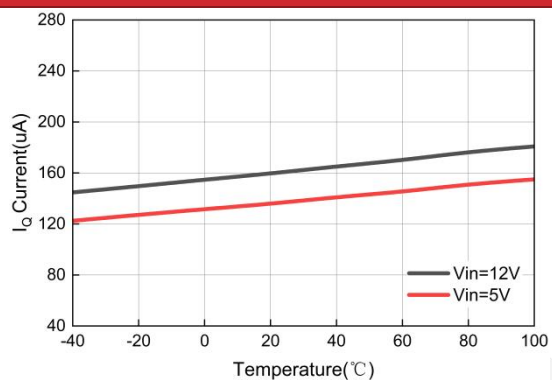
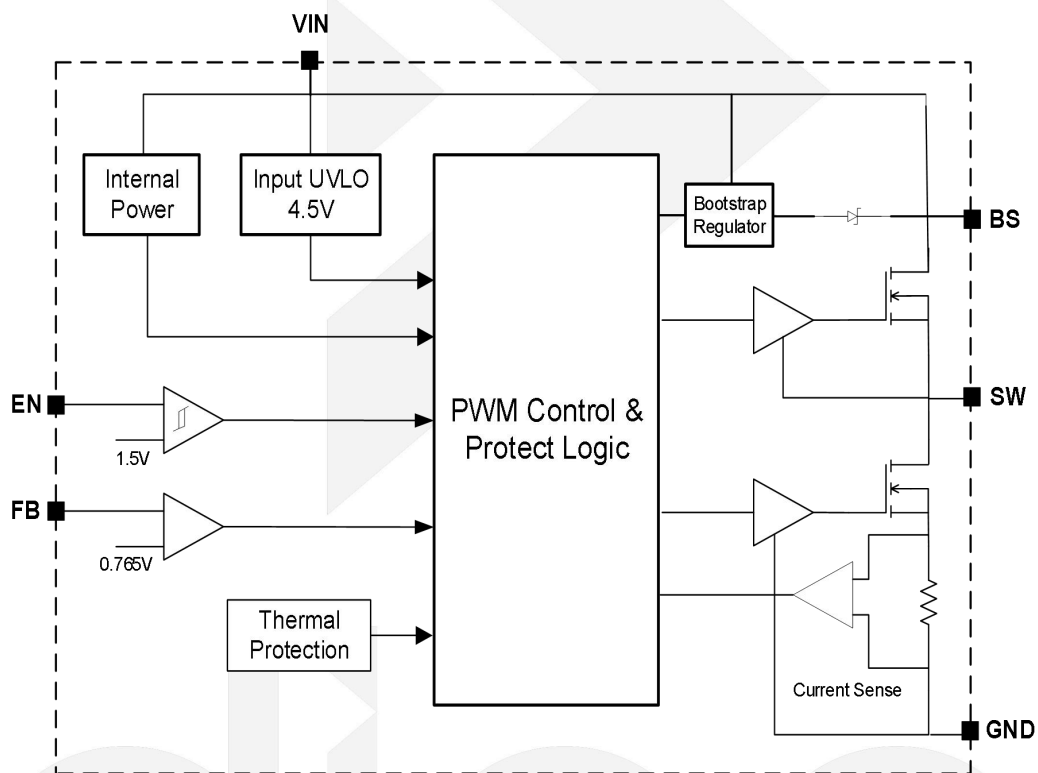


Figure 18. Quiescent current vs. Temperature

8. Block Diagram



9. Application Information

Important notice: Validation and testing are the most reliable ways to confirm system functionality. The application information is not part of the specification and is for reference purposes only.

9.1. Application examples

DIO69319 4.5 V to 24 V input, 1.05 V output converter.

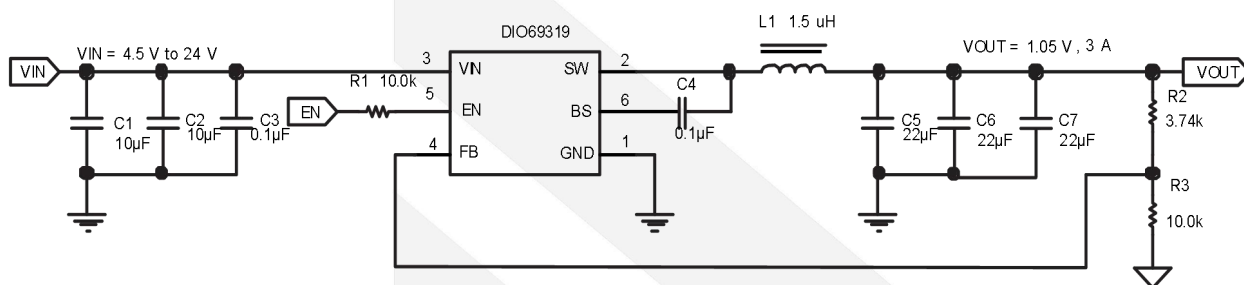


Figure 19. DIO69319 1.05 V/3 A reference design

The DIO69319 is a synchronous buck regulator IC that integrates the pure COT control, and top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra-low $R_{DS(ON)}$ power switches and proprietary pure COT control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size, and thus achieve the minimum solution footprint.

Table 1. Design Parameters

Parameter	Value
Input voltage range	4.5 V to 24 V
Output voltage	1.05 V
Output current	3 A
Output voltage ripple	20 mV _{PP}

Table 2. Recommended Component Values

Output voltage (V)	R2 (kΩ)	R3 (kΩ)	L1 (μH)			C5 + C6 (μF)
			Min	Typ	Max	
1	3.09	10.0	1	1.5	2.2	44 - 66
1.05	3.74	10.0	1	1.5	2.2	44 - 66
1.2	5.76	10.0	1	1.5	2.2	44 - 66
1.5	9.53	10.0	1	1.5	2.2	44 - 66
1.8	13.7	10.0	1	1.5	2.2	44 - 66
2.5	22.6	10.0	1.5	2.2	3.3	44 - 66
3.3	33.2	10.0	1.5	2.2	3.3	44 - 66
5	54.9	10.0	1.5	3.3	4.7	44 - 66

Because of the high integration in the DIO69319 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN} , output capacitor C_{OUT} , output inductor L, and feedback resistors (R1 and R2) need to be selected for the targeted application specifications.

9.2. Feedback resistor dividers R1 and R2

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 10 k and 1 M is highly recommended for both resistors. If V_{OUT} is 3.3 V and $R1 = 40.2$ k is chosen, then R2 can be calculated to be 12 k.

$$R_2 = \frac{0.765V}{V_{OUT} - 0.765V} R_1 \quad (1)$$

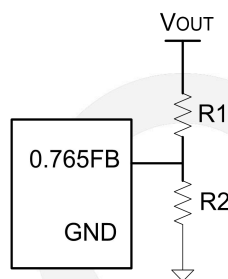


Figure 20. Feedback resistor dividers R1 and R2

9.3. Current protection

The output over-current limit (OCL) is implemented using a cycle-by-cycle valley detect and control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is

temperature compensated. During the on time of the high-side FET switch, the switch current increases at a linear rate determined by V_{IN} , V_{OUT} , the on-time, and the output inductor value.

During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current, I_{OUT} . If the monitored current is above the OCL level, the converter maintains the low-side FET on and delays the creation of a new set pulse, even if the voltage feedback loop requires one, until the current level below the OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the over-current condition exists for consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL threshold is returned to the higher value.

There are some important considerations for this type of over-current protection. The load current is higher than the over-current threshold by one-half of the peak-to-peak inductor ripple current. Also, when the current is limited, the output voltage tends to fall as the demanded load current may be higher than the available current from the converter. This may cause the output voltage to fall. When the V_{FB} falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device will shut down after the UVP delay time (typically 14 μ s) and restart after the hiccup time (typically 8 ms).

When the over-current condition is removed, the output voltage returns to the regulated value.

9.4. UVLO protection

Under voltage lock-out protection (UVLO) monitors the device input voltage. When the voltage is lower than the UVLO threshold voltage, the device is shut off. This protection is non-latching.

9.5. Thermal shutdown

The device monitors its own temperature. If the temperature exceeds the threshold value (typically 155°C), the device is shut off. This is a non-latch protection.

9.6. Input capacitor C_{IN}

This ripple current through the input capacitor is calculated as:

$$I_{CIN_RMS} = I_{OUT} \cdot \sqrt{D(1-D)} \quad (2)$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{CIN_RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for DC/DC design.

To minimize the potential noise problem, place a typical X5R or better-grade ceramic capacitor is really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN} , and IN/GND pins. In this case, a 10 μ F low ESR ceramic capacitor is recommended.

9.7. Output capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady-state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better-grade ceramic capacitor greater than 22 μF capacitance.

9.8. Output inductor L

There are several considerations in choosing this inductor.

- 1) Choose the inductance to provide the desired ripple current. It is suggested to set the ripple current at about 40% of the maximum output current. The inductance is calculated as follows:

$$L = \frac{V_{OUT}(1 - V_{OUT} / V_{IN, MAX})}{F_{SW} \times I_{OUT, MAX} \times 40\%} \quad (3)$$

where F_{SW} is the switching frequency and $I_{OUT, MAX}$ is the maximum load current. The DIO69319 regulator IC is quite tolerant of different ripple current amplitudes. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

- 2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT, MIN} > I_{OUT, MAX} + \frac{V_{OUT}(1 - V_{OUT} / V_{IN, MAX})}{2 \cdot F_{SW} \cdot L} \quad (4)$$

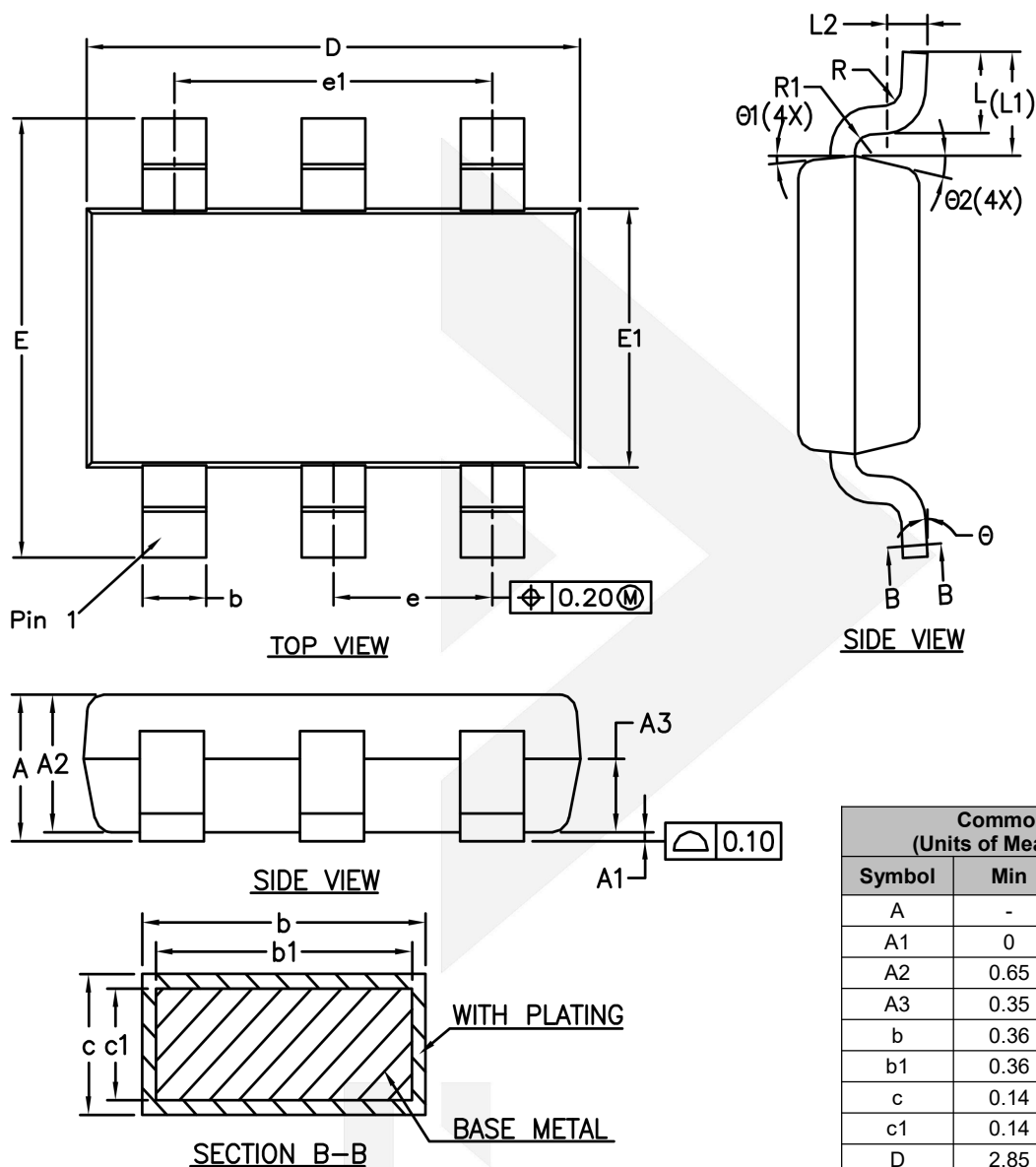
- 3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with $DCR < 50 \text{ m}\Omega$ to achieve good overall efficiency.

10. Layout Guidelines

The layout design of the DIO69319 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN} , L , $R1$, and $R2$.

- (1) It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. If the board space allows, a ground plane is highly desirable.
- (2) C_{IN} must be close to pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.
- (3) The PCB copper area associated with the SW pin must be minimized to avoid the potential noise problem.
- (4) The components $R1$ and $R2$, and the trace connecting to the FB pin must NOT be adjacent to the SW net on the PCB layout to avoid the noise problem.
- (5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull-down 1 $\text{m}\Omega$ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

11. Physical Dimensions: TSOT23-6



Common Dimensions (Units of Measure = Millimeter)			
Symbol	Min	Nom	Max
A	-	-	0.90
A1	0	-	0.15
A2	0.65	0.75	0.85
A3	0.35	0.40	0.45
b	0.36	-	0.50
b1	0.36	0.38	0.45
c	0.14	-	0.20
c1	0.14	0.15	0.16
D	2.85	2.95	3.05
E	2.60	2.80	3.00
E1	1.60	1.65	1.70
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
L	0.30	0.45	0.60
L1	0.575REF		
L2	0.25BSC		
R	-	-	0.25
R1	-	-	0.25
θ	0°	-	8°
$\theta1$	3°	5°	7°
$\theta2$	10°	12°	14°

Disclaimer

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