DIO5558

Programmable POS & NEG Voltage Solution for AMOLED

Description

The DIO5558 is a highly integrated, programmable power management IC for AMOLED and wearable devices. By taking the input supply voltage (2.9 V to 5.5 V) from battery, the DIO5558 generates the AVDD, OVDD, and OVSS outputs following the target settings.

The DIO5558 is operated in symmetry mode. In symmetry mode, the initial output voltages of AVDD, OVDD and OVSS are 3.3 V, 3.3 V and -3.3 V respectively.

The DIO5558 also integrates a serial data interface for the flexibility of the various settings. The DIO5558 supports undervoltage lockout, short-circuit protection, and thermal shutdown protection.

The device is available in package WLCSP-21.

Features

- Supply voltage range: 2.9 V to 5.5 V
- SRL interface protocol
- Programmable OVSS range: -2.0 V to −5.0 V
- AVDD default: 3.3 V
- OVDD default: 3.3 V
- Package: WLCSP-21

Application

- Active matrix OLED power supply

Ordering Information

Part Number	Top Marking	RoHS	T_A	Package	
DIO5558WL21	DE5H	Green	-40°C to 85°C	WLCSP-21	Tape & Reel, 3000

If you encounter any issue in the process of using the device, please contact our customer service at marketing@dioo.com or phone us at (+86)-21-62116882. If you have any improvement suggestions regarding the datasheet, we encourage you to contact our technical writing team at docs@dioo.com. Your feedback is invaluable for us to provide a better user experience.

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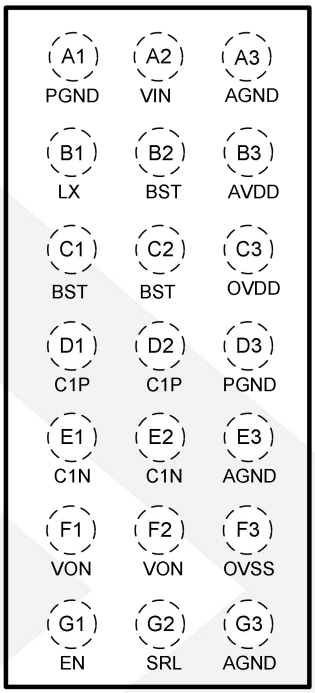
1. Pin Assignment and Functions



WLCSP-21

(Bottom view)

Pin No.	Name	Description
A1/D3	PGND	Power ground
A2	VIN	Power supply input
A3/E3/G3	AGND	Analog ground
B1	LX	Switching node of boost regulator
B3	AVDD	Output voltage for driver
B2/C1/C2	BST	Output of boost regulator
C3	OVDD	Positive output voltage for OLED bias
D1/D2	C1P	Flying capacitor connection
E1/E2	C1N	Flying capacitor connection
F1/F2	VON	Negative charge pump output
F3	OVSS	Negative output voltage for OLED bias
G1	EN	Enable pin
G2	SRL	One-Pin serial interface control

2. Absolute Maximum Ratings

Exceeding the maximum ratings listed under Absolute Maximum Ratings when designing is likely to damage the device permanently. Do not design to the maximum limits because long-time exposure to them might impact the device's reliability. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Rating	Unit
V_{IN}	VIN to AGND	−0.3 to 6.0	V
V_{LX}	LX to PGND	−0.3 to 6.0	V
V_{I1}	Input voltage (EN, SRL)	−0.3 to (V_{IN} +0.3)	V
V_{O1}	Output voltage 1 (BST, AVDD, OVDD, C1P)	−0.3 to 5.5	V
V_{O2}	Output voltage 2 (OVSS, VON, C1N)	−5.5 to 0.3	V
T_J	Operating junction temperature range	−40 to 150	°C
T_A	Operating ambient temperature range	−40 to 85	°C
T_{STG}	Storage temperature range	−65 to 150	°C
$R_{\theta JA}$	Package thermal range	50	°C/W
P_D	Power dissipation at T_A = 25°C, T_J = 125°C	2	W

3. ESD Ratings

When a statically-charged person or object touches an electrostatic discharge sensitive device, the electrostatic charge might be drained through sensitive circuitry in the device. If the electrostatic discharge possesses sufficient energy, damage might occur to the device due to localized overheating.

Model	Condition	Value	Unit
ESD	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V

4. Recommended Operating Condition

Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Rating	Unit
V_{IN}	Input supply voltage	2.9 to 5.5	V
T_A	Operating free-air temperature	-40 to 85	°C

5. Electrical Characteristics

V_{IN} = 2.9 V to 5.5 V, T_A = −40°C to 85°C, unless otherwise specified. Typical values are tested at 25°C ambient temperature, V_{IN} = 3.7 V, V_{AVDD} = 3.3 V, V_{OVDD} = 3.3 V, V_{OVSS} = −3.3 V, C_{fly} = C_{VIN} = C_{AVDD} = C_{OVDD} = C_{BST} = C_{VON} = 4.7 μF, C_{OVSS} = 10 μF.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Operating power						
V_{IN}	V_{IN} input voltage range		2.9	3.7	5.5	V
V_{UVLO}	Under voltage lockout threshold	Rising	2.5	2.6	2.7	V
		Falling	2.3	2.4	2.5	V
I_{IDLE_IN}	Idle mode total input current	V_{IN} = 3.7 V SRL = GND & AVDD, No load		30		μA
Eff1	Efficiency1	V_{IN} = 3.2 V, I_{AVDD} = 3 mA I_{OVDD} = I_{OVSS} = 0 mA		73		%
		V_{IN} = 3.7 V, I_{AVDD} = 3 mA I_{OVDD} = I_{OVSS} = 0 mA		80		
		V_{IN} = 4.2 V, I_{AVDD} = 3 mA I_{OVDD} = I_{OVSS} = 0 mA		72		
Eff2	Efficiency2	V_{IN} = 3.2 V, I_{AVDD} = 3 mA I_{OVDD} = I_{OVSS} = 10 mA		83		%
		V_{IN} = 3.7 V, I_{AVDD} = 3 mA I_{OVDD} = I_{OVSS} = 10 mA		86		
		V_{IN} = 4.2 V, I_{AVDD} = 3 mA I_{OVDD} = I_{OVSS} = 10 mA		77		
Eff3	Efficiency3	V_{IN} = 3.2 V, I_{AVDD} = 3 mA I_{OVDD} = I_{OVSS} = 30 mA		85		%
		V_{IN} = 3.7 V, I_{AVDD} = 3 mA I_{OVDD} = I_{OVSS} = 30 mA		88		
		V_{IN} = 4.2 V, I_{AVDD} = 3 mA I_{OVDD} = I_{OVSS} = 30 mA		77		
I_{SD}	Shutdown current	EN = SRL = GND			1	μA
V_{IH}	EN high voltage level		1.0			V
V_{IL}	EN low voltage level				0.4	V
R_{EN}	EN pull low resistance			1		MΩ
Synchronous current mode boost regulator						
V_{BOOST}	BOOST output voltage				5.5	V
I_{BOOST_MAX}	BOOST maximum load current	OVDD = 3.3 V, OVSS = -3.3 V	110			mA
		OVDD = 4.0 V, OVSS = -4.0 V	170			mA
f_{OSC_LX}	LX switching frequency			0.5		MHz

I_{LIM_LX}	LX current limit		0.4	0.6	0.85	A
R_{ON_NMOS1}	LX NMOS ON-resistance			0.5		Ω
R_{ON_PMOS1}	LX PMOS ON-resistance			0.5		Ω
AVDD						
V_{AVDD}	Output voltage			3.3		V
	Output voltage tolerance		-1		1	%
I_{AVDD_MAX}	Load current capacity	AVDD = 3.3 V, OVDD = 3.3 V OVSS = –3.3 V	50			mA
	Line regulation	V_{IN} = 2.9 V to 5.5 V, I_{AVDD} = 10 mA		5	10	mV
	Load regulation	V_{IN} = 3.7 V, I_{AVDD} = 0 mA to 10 mA		5	10	mV
	Output transient ripple	V_{IN} = 3.7 V, AVDD = 3.3 V OVDD = 3.3 V, OVSS = –3.3 V I_{AVDD} & I_{OVDD} & I_{OVSS} ≤ 5 mA when OVDD or OVSS voltage change	-10		10	mV
	Output voltage ripple	V_{IN} = 3.7 V AVDD = 3.3 V, I_{AVDD} ≤ 5 mA OVDD = 3.3 V, I_{OVDD} ≤ 30 mA OVSS = –3.3 V, I_{OVSS} ≤ 30 mA	-5		5	mV
		V_{IN} = 3.7 V AVDD = 3.3 V, I_{AVDD} ≤ 5 mA OVDD = 3.3 V, I_{OVDD} ≤ 80 mA OVSS = -4.0 V, I_{OVSS} ≤ 80 mA	-5		5	
	Line transient ripple	1. V_{IN} = 4.65 V (max) to 4.15 V 2. V_{IN} = 3.5 V to 3.0 V AVDD = 3.3 V, I_{AVDD} = 10 mA OVDD = 3.3 V, I_{OVDD} = 30 mA OVSS = –3.3 V, I_{OVSS} = 30 mA T_R = T_F = 50 µs	-10		10	mV
		1. V_{IN} = 4.65 V to 4.15 V 2. V_{IN} = 3.5 V to 3.0 V AVDD = 3.3 V, I_{AVDD} = 3 mA OVDD = 3.3 V, I_{OVDD} = 80 mA OVSS = –3.3 V, I_{OVSS} = 80 mA T_R = T_F = 50 µs	-10		10	
	Load transient ripple	V_{IN} = 3.7 V, AVDD = 3.3 V, OVDD = 3.3 V, OVSS = –3.3 V I_{AVDD} = 0 to 10 mA & 10 to 0 mA I_{OVDD} = 0 to 50 mA & 50 to 0 mA I_{OVSS} = 0 to 50 mA & 50 to 0 mA T_R = T_F = 50 µs	−10		10	mV

		V_{IN} = 3.7 V, AVDD = 3.3 V OVDD = 3.3V, OVSS = –4.0 V I_{AVDD} = 0 to 10 mA & 10 to 0 mA I_{OVDD} = 0 to 60 mA & 60 to 0 mA I_{OVSS} = 0 to 60 mA & 60 to 0 mA T_R = T_F = 50 µs	−10		10	
t_{SS1}	Soft-start time			1		ms
I_{CC_AVDD}	Current Limit			250		mA
t_{SCP_AVDD}	Duration to SCP trigger time			1		ms
OVDD						
V_{OVDD}	OVDD output voltage		2.8	3.3	4.0	V
	OVDD output voltage tolerance		-0.5		0.5	%
I_{OVDD}	Load current capacity	OVDD = 3.3 V, OVSS = –3.3 V	80			mA
		OVDD = 4.0 V, OVSS = –4.0 V	100			
	Line regulation	V_{IN} = 3.0 V to 5.5 V OVDD = 3.3 V, I_{OVDD} = 50 mA		5	10	mV
		V_{IN} = 3.0 V to 5.5 V OVDD = 4.0 V, I_{OVDD} = 80 mA		5	10	
	Load regulation	OVDD = 3.3 V I_{OVDD} = 0 mA to 50 mA		5	10	mV
		OVDD = 4.0 V I_{OVDD} = 0 mA to 80 mA		5	10	
	Output transient ripple	V_{IN} = 3.7 V, AVDD = 3.3 V OVDD = 3.3 V, OVSS = −3.3 V I_{AVDD} & I_{OVDD} & I_{OVSS} ≤ 5 mA When OVSS Voltage Change	-10		10	mV
	Output voltage ripple	V_{IN} = 3.7 V AVDD = 3.3 V, I_{AVDD} ≤ 5 mA OVDD = 3.3 V, I_{OVDD} ≤ 80 mA OVSS = −4.0 V, I_{OVSS} ≤ 80 mA	-5		5	mV
	Line transient ripple	1. V_{IN} = 4.65 V to 4.15 V 2. V_{IN} = 3.5 V to 3.0 V AVDD = 3.3 V, I_{AVDD} = 10 mA OVDD = 3.3 V, I_{OVDD} = 30 mA OVSS = –3.3 V, I_{OVSS} = 30 mA T_R = T_F = 50 µs	-10		10	mV
		1. V_{IN} = 4.65 V to 4.15 V 2. V_{IN} = 3.5 V to 3.0 V AVDD = 3.3 V, I_{AVDD} = 3 mA OVDD = 3.3 V, I_{OVDD} = 80 mA OVSS = –3.3 V, I_{OVSS} = 80 mA	-10		10	

		T_R = T_F = 50 μs				
	Load transient ripple	V_{IN} = 3.7 V, AVDD = 3.3 V OVDD = 3.3 V, OVSS = –3.3 V I_{AVDD} = 0 to 10 mA & 10 to 0 mA I_{OVDD} = 0 to 50 mA & 50 to 0 mA I_{OVSS} = 0 to 50 mA & 50 to 0 mA T_R = T_F = 50 μs	-10		10	mV
		V_{IN} = 3.7 V, AVDD = 3.3 V OVDD = 3.3 V, OVSS = –4.0 V I_{AVDD} = 0 to 10 mA & 10 to 0 mA I_{OVDD} = 0 to 60 mA & 60 to 0 mA I_{OVSS} = 0 to 60 mA & 60 to 0 mA T_R = T_F = 50 μs	-10		10	
t_{SS2}	Soft-start time			1.2		ms
I_{CC_OVDD}	Current limit			105		mA
t_{SCP_OVDD}	Duration to SCP trigger time			1		ms
Negative charge pump controller for VON						
V_{VON}	VON output voltage		-5.5			V
I_{VON_MAX}	VON maximum load current	OVDD = 3.3 V, OVSS = –3.3 V	100			mA
		OVDD = 4.0 V, OVSS = –4.0 V	120			
Low dropout regulator for OVSS						
V_{OVSS}	Output voltage		-5.0	-3.3	-2.0	V
	OVSS output voltage tolerance		-1		1	%
I_{OVSS}	Load current capacity	OVDD = 3.3 V, OVSS = -3.3 V	100			mA
		OVDD = 4.0 V, OVSS = –4.0 V	100			
	Output transient ripple	V_{IN} = 3.7 V, AVDD = 3.3 V OVDD = 3.3 V, OVSS = –3.3 V I_{AVDD} & I_{OVDD} & I_{OVSS} ≤ 5 mA When OVDD voltage change	-10		10	mV
	Output voltage ripple	V_{IN} = 3.7 V, AVDD = 3.3 V, I_{AVDD} ≤ 5 mA OVDD = 3.3 V, I_{OVDD} ≤ 30 mA OVSS = –3.3 V, I_{OVSS} ≤ 30 mA	-5		5	mV
		V_{IN} = 3.7 V, AVDD = 3.3 V, I_{AVDD} ≤ 5 mA OVDD = 3.3 V, I_{OVDD} ≤ 80 mA OVSS = –4.0 V, I_{OVSS} ≤ 80 mA	-5		5	
	Line transient ripple	1. V_{IN} = 4.65 V to 4.15 V 2. V_{IN} = 3.5 V to 3.0 V	-10		10	mV

		AVDD = 3.3 V, I_{AVDD} = 10 mA OVDD = 3.3 V, I_{OVDD} = 30 mA OVSS = –3.3 V, I_{OVSS} = 30 mA T_R = T_F = 50 µs				
		1. V_{IN} = 4.65 V to 4.15 V 2. V_{IN} = 3.5 V to 3.0 V AVDD = 3.3 V, I_{AVDD} = 3 mA OVDD = 3.3 V, I_{OVDD} = 80 mA OVSS = –3.3 V, I_{OVSS} = 80 mA T_R = T_F = 50 µs	-10		10	
	Load transient ripple	V_{IN} = 3.7 V, AVDD = 3.3 V OVDD = 3.3 V, OVSS = –3.3 V I_{AVDD} = 0 to 10 mA & 10 to 0 mA I_{OVDD} = 0 to 50 mA & 50 to 0mA I_{OVSS} = 0 to 50 mA & 50 to 0 mA T_R = T_F = 50 µs	-10		10	mV
		V_{IN} = 3.7 V, AVDD = 3.3 V OVDD = 3.3 V, OVSS = –4.0 V I_{AVDD} = 0 to 10 mA & 10 to 0 mA I_{OVDD} = 0 to 60 mA & 60 to 0 mA I_{OVSS} = 0 to 60 mA & 60 to 0 mA T_R = T_F = 50 µs	-10		10	
t_{SS3}	Soft-start time			0.6		ms
I_{CC_OVSS}	Current limit			110		mA
t_{SCP_OVSS}	Duration to SCP trigger time			1		ms

Note: Specifications subject to change without notice.

6. Typical Characteristics

V_{IN} = 3.7 V, default output voltage, C_{VIN} = C_{fly} = C_{AVDD} = C_{OVDD} = C_{BST} = C_{VON} = 4.7 μF, C_{OVSS} = 10 μF. Typical values are tested at 25 °C ambient temperature, unless otherwise specified.

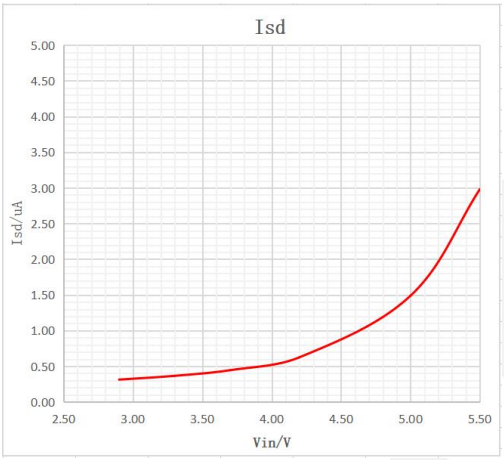


Figure 1. I_{sd} vs. V_{IN}

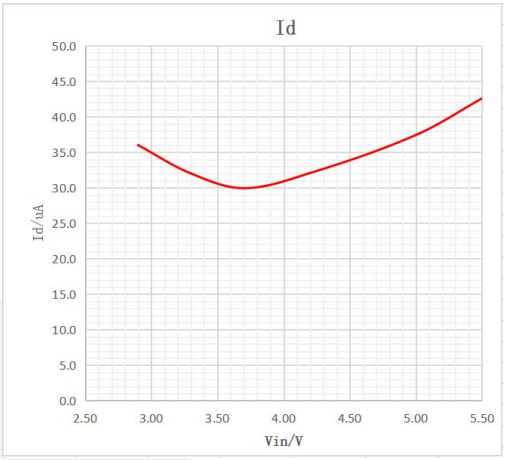


Figure 2. I_d vs. V_{IN}

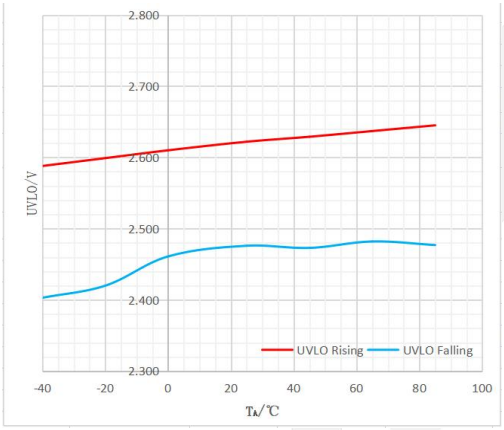


Figure 3. UVLO vs. T_A -- SYS = GND

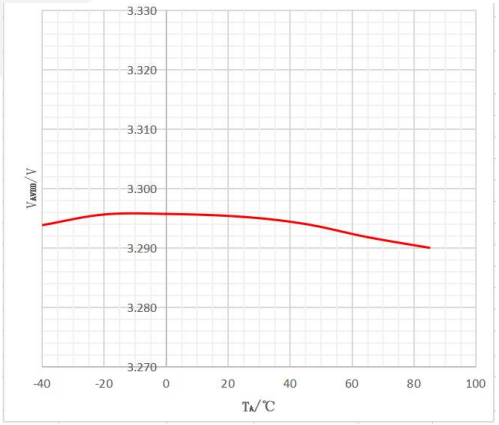


Figure 4. V_{AVDD} vs. T_A

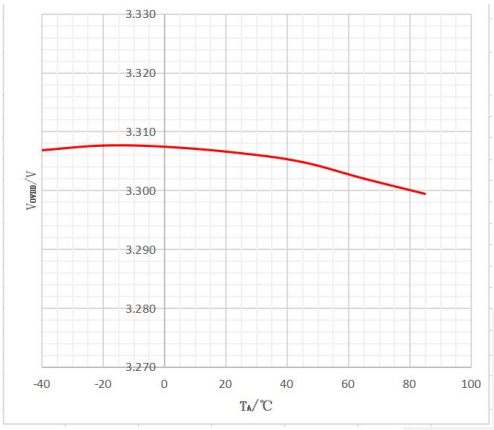


Figure 5. V_{OVDD} vs. T_A

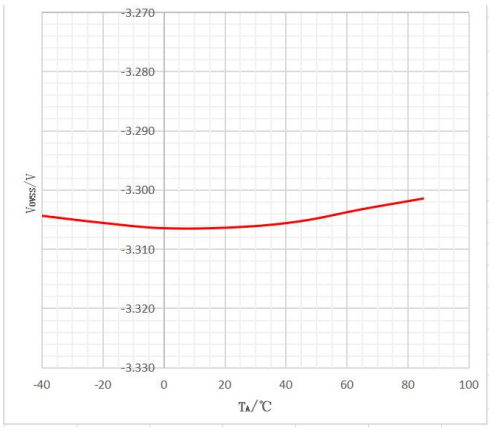


Figure 6. V_{OVSS} vs. T_A

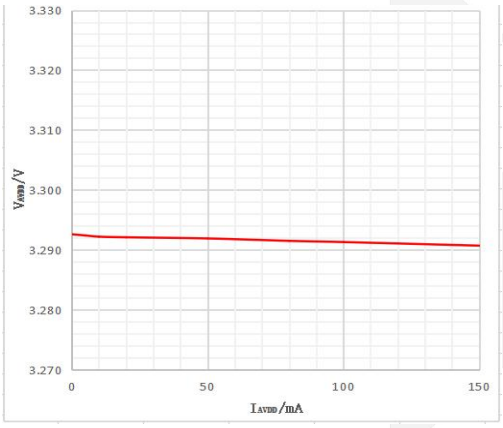


Figure 7. V_{AVDD} load regulation

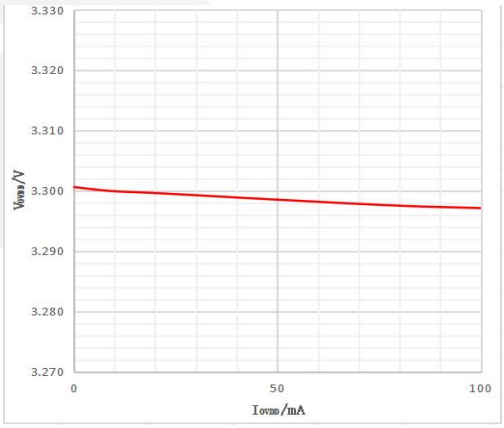


Figure 8. V_{OVDD} load regulation

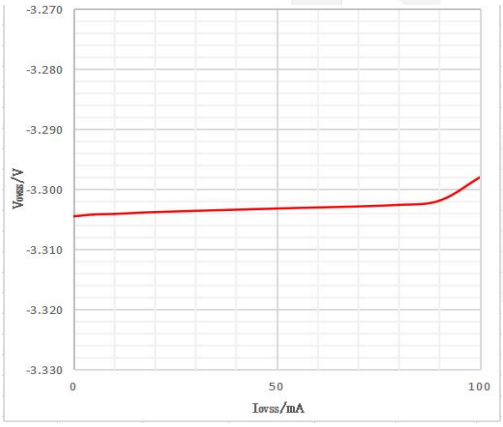


Figure 9. V_{OVSS} load regulation

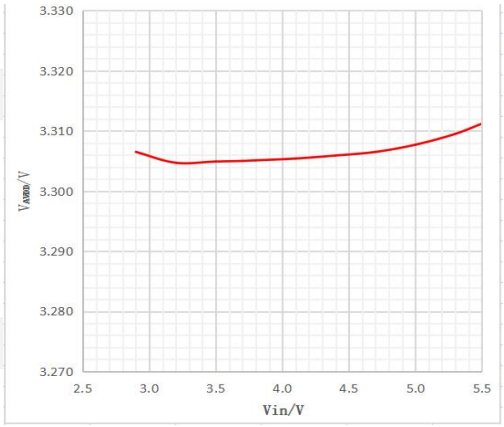


Figure 10. V_{AVDD} line regulation -- no load

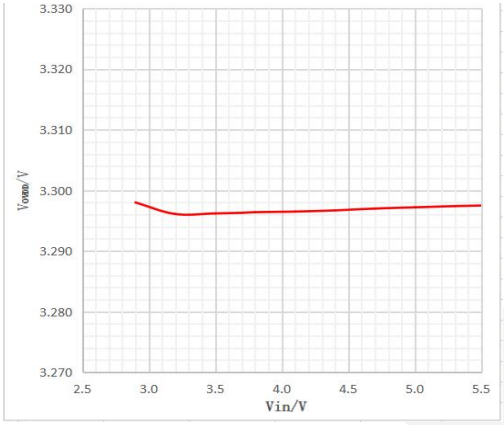


Figure 11. V_{OVDD} line regulation -- no load

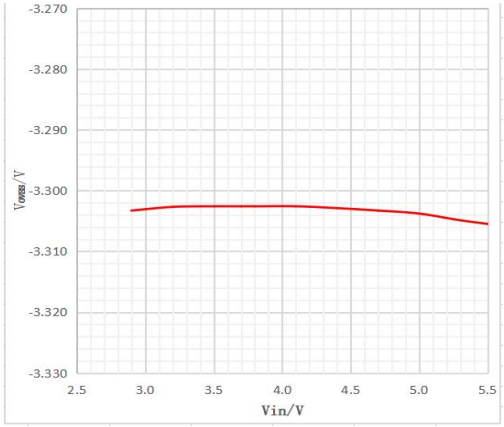


Figure 12. V_{OVSS} line regulation -- no load

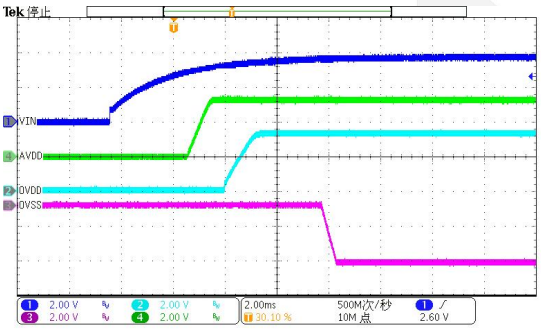


Figure 13. VIN ON, no load

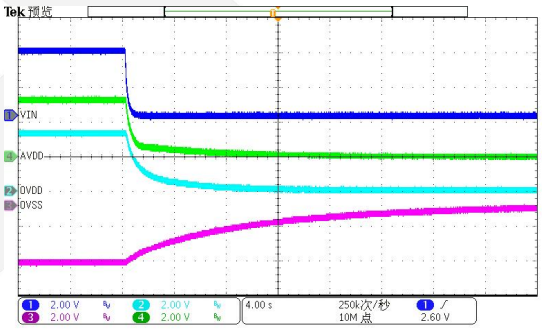


Figure 14. VIN OFF, no load

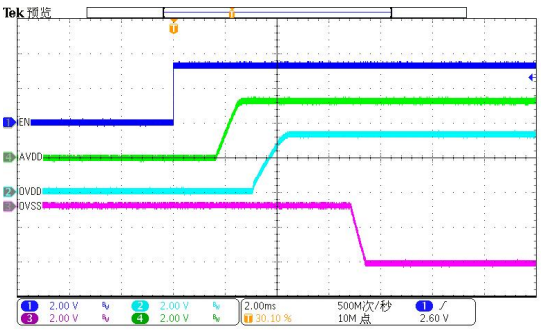


Figure 15. EN ON, no load

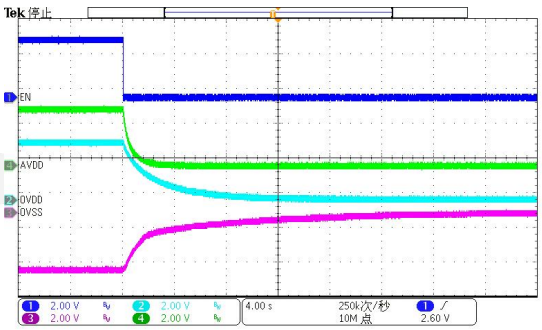


Figure 16. EN OFF, no load

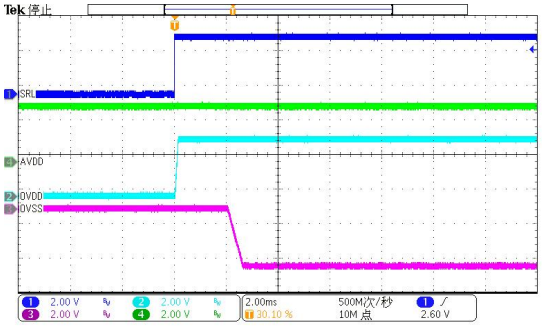


Figure 17. SRL ON, no load

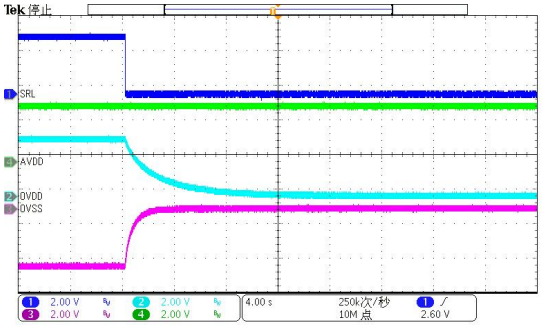
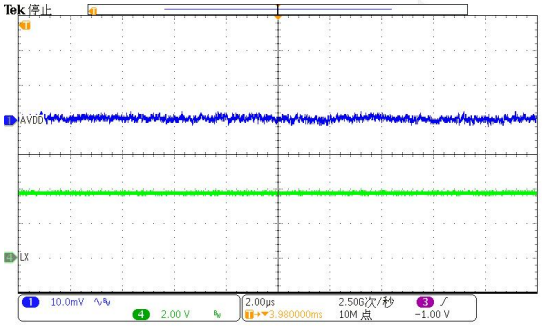
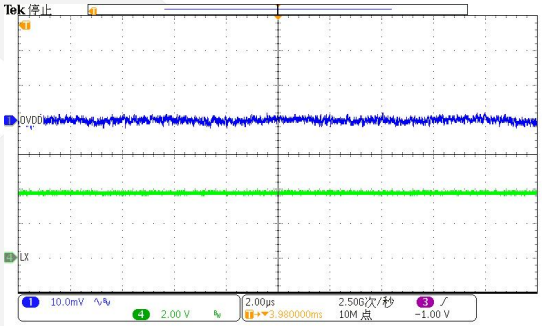


Figure 18. SRL OFF, no load



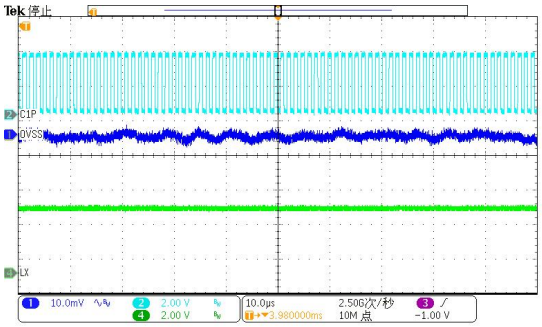
I_{AVDD} = 5 mA, I_{OVDD} = I_{OVSS} = 30 mA

Figure 19. AVDD ripple



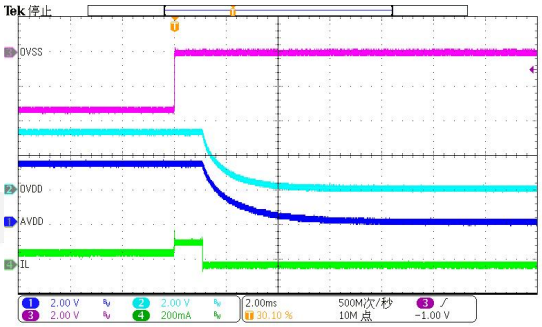
I_{AVDD} = 5 mA, I_{OVDD} = I_{OVSS} = 30 mA

Figure 20. AVDD ripple



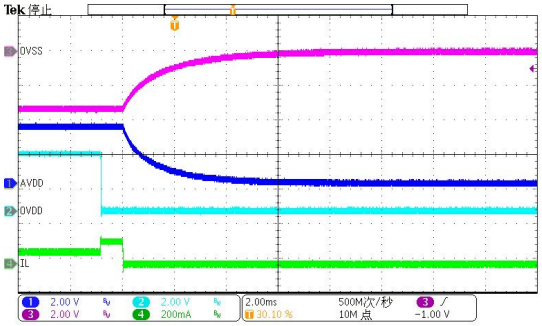
I_{AVDD} = 5 mA, I_{OVDD} = I_{OVSS} = 30 mA

Figure 21. OVSS ripple



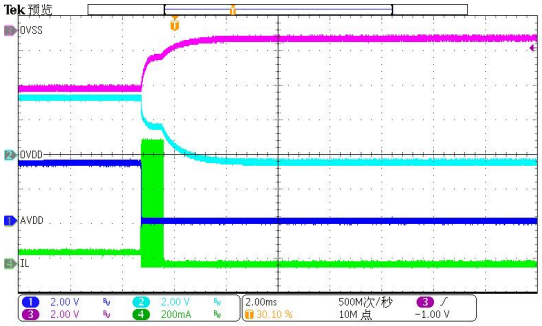
I_{AVDD} = 10 mA, I_{OVDD} = I_{OVSS} = 30 mA

Figure 22. Short circuit -- OVSS to GND



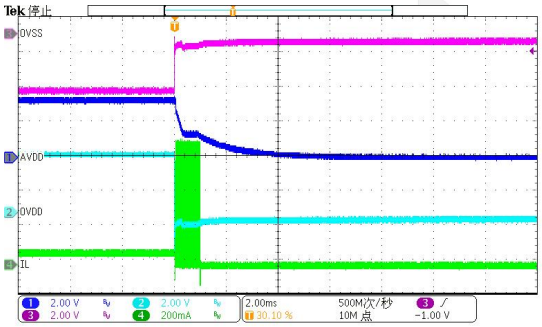
I_{AVDD} = 10 mA, I_{OVDD} = I_{OVSS} = 30 mA

Figure 23. Short circuit -- OVDD to GND



I_{AVDD} = 10 mA, I_{OVDD} = I_{OVSS} = 30 mA

Figure 24. Short circuit -- AVDD to GND



I_{AVDD} = 10 mA, I_{OVDD} = I_{OVSS} = 30 mA

Figure 25. Short circuit -- OVDD to OVSS

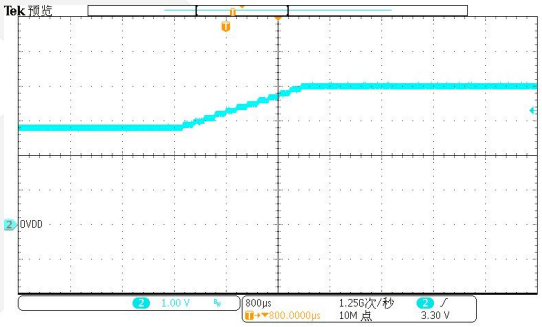


Figure 26. OVDD Programmable

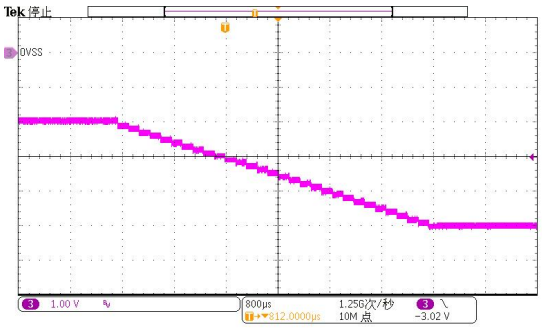


Figure 27. OVSS programmable

7. Function Description

7.1. Input control block

The DIO5558 measures the input voltage from the battery to decide whether to activate the boost regular. The DIO5558 also determines whether it should be in operation or shut down by detecting the status of the EN and SRL pins.

7.2. AVDD

The DIO5558 has a built-in LDO that outputs a 3.3 V AVDD voltage with a minimum output current of 50 mA and a soft-start time of 1 ms.

7.3. OVDD

Through a built-in LDO, the DIO5558 outputs OVDD voltage with a minimum output current of 80 mA. Through a serial data programming approach, the OVDD output voltage can be configured to be between 2.8 V and 4.0 V with a 0.1 V resolution.

7.4. VON

The DIO5558 integrates with a negative charge pump controller, together with two external flying capacitors, to invert either the battery V_{IN} or boost output V_{BOOST} as the input source of LDO for OVSS in order to provide the negative voltage output for OVSS. On this VON pin, a stabilizing capacitor of 10 μF from outside is highly advised.

7.5. OVSS

The DIO5558 produces OVSS voltage using a built-in LDO with a minimum output current of 100 mA. Through a serial data programming approach, the OVSS output voltage is programmable from -2.0 V to -5.0 V with a 0.1 V resolution.

7.6. Undervoltage lockout (UVLO)

When the input UVLO dropping threshold of 2.4 V is detected, the DIO5558 will immediately shut down to avoid the battery from being entirely discharged. As soon as the input voltage rises beyond the UVLO rising threshold of 2.6 V, the DIO5558 will automatically resume operation.

7.7. Undervoltage protection (UVP)

The DIO5558 uses UVP protection in all three LDOs to shield the panel system from any aberrant conditions that can harm it. The DIO5558 will turn off all outputs to GND as soon as the output falls below 80% of AVDD, 80% of OVDD, or 40% of OVSS. Toggling the EN pin will restore DIO5558 functionality after UVP.

7.8. Power sequence

When VIN rises above 2.6 V, the DIO5558 begins to operate, and as soon as VIN falls below 2.4 V, it stops. The DIO5558 will drive AVDD to 3.3 V coupled with soft-start behavior as soon as EN is driven to high level. In the interim, SRL should be kept at a low level. Furthermore, the OVSS and OVDD outputs remain at GND level. After the DIO5558 determines that the SRL input is at a high level, the OVDD will be driven to its default voltage setting. After the OVDD, the OVSS will also be driven to its default voltage level. The soft-start function is present in both outputs. Maintain the SRL at a high level for at least 6 ms before starting the serial data programming procedure to change the OVDD and OVSS to the desired values. All outputs are brought back to GND once EN is pulled to a low level.

7.9. Battery power saving options

7.9.1. Shutdown by HW control, EN & SRL

When the EN and SRL pins are pushed low, the DIO5558 enters shutdown mode and only uses 0.5 μA of the input current. In order to reduce battery usage, the system controller can force the DIO5558 into shutdown mode when the display is allowed to be off.

7.9.2. Idle mode by SRL setting

The DIO5558 can be configured into idle mode to use less battery input current during light load operation on a panel system by disabling some unneeded protection and reducing switch frequency, while maintaining AVDD and OVDD at 3.3 V and OVSS at -3.3 V.

7.10. Serial data interface

A pull-down 1 MΩ internal resistor is built into the serial data input pin of the DIO5558 SRL. The protocol to set the OVDD/OVSS target output voltage as well as the mode choice on the SRL is the low pulse count. Figure 1 depicts the timing of the SRL and the responses of the OVDD/OVSS following the SRL protocol parameters. For your reference, Table 1 includes a list of the timing parameter requirements for SRL. For your reference, Table 2 includes the SRL pulse count mapping table. Please be aware that the approach times for the target for OVDD and OVSS are 0.1 V and 128 μs per step, respectively.

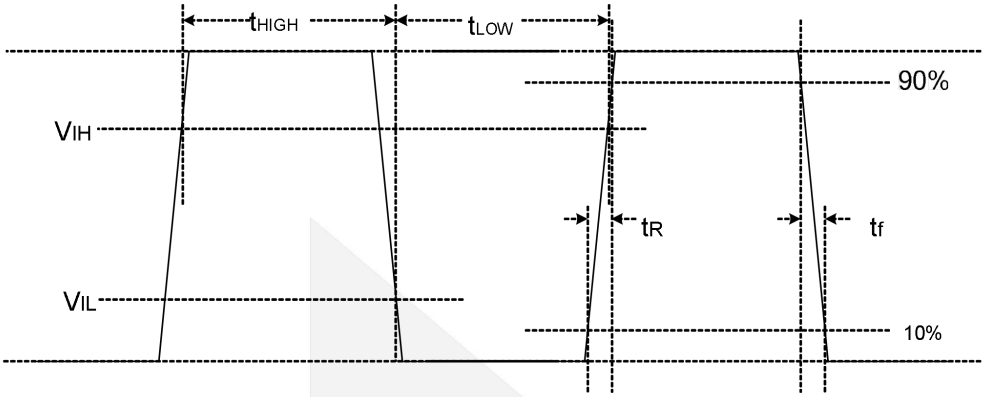


Figure 28. SRL waveform chart

Table 1. SRL timing parameters

Symbol	Description	Min	Typ	Max	Unit
t_R	SRL rise time			200	ns
t_F	SRL fall time			200	ns
V_{IH}	SRL input high voltage	1.0		V_{IN}	V
V_{IL}	SRL input low voltage	0		0.4	V
t_{HIGH}	SRL high level time period	8	20	80	μs
t_{LOW}	SRL low level time period	8	20	80	μs
t_{INT}	SRL initialization time		6		ms
t_{STORE}	End of pulse count	140			μs
t_{OFF}	SRL off	200			μs
t_{NEXT}	Next data waiting time	8		20	ms
t_{STEP}	OVDD/OVSS step time		128		μs

Table 2. SRL pulse

Pulse	Function description				
1	Reserved				
2	Reserved				
3	Reserved				
4	Reserved				
5	Reserved				
6	Reserved				
7	Reserved				
8	Fast discharge function on				
9	OVSS turn off				
10 ~ 22	OVDD setting, 2.8 V to 4.0 V				
48 ~ 78	OVSS setting, –5 V to –2.0 V				
Pulse	**OVDD (V)**	**Pulse**	**OVSS (V)**	**Pulse**	**OVSS (V)**
10	2.8	48	−5.0	64	−3.4
11	2.9	49	−4.9	65	−3.3
12	3.0	50	−4.8	66	−3.2
13	3.1	51	−4.7	67	−3.1
14	3.2	52	−4.6	68	−3.0
15	3.3	53	−4.5	69	−2.9
16	3.4	54	−4.4	70	−2.8
17	3.5	55	−4.3	71	−2.7
18	3.6	56	−4.2	72	−2.6
19	3.7	57	−4.1	73	−2.5
20	3.8	58	−4.0	74	−2.4
21	3.9	59	−3.9	75	−2.3
22	4.0	60	−3.8	76	−2.2
		61	−3.7	77	−2.1
		62	−3.6	78	−2.0
		63	−3.5		

8. Application Information

Important notice: Validation and testing are the most reliable ways to confirm system functionality. The application information is not part of the specification and is for reference purposes only.

8.1. Application examples

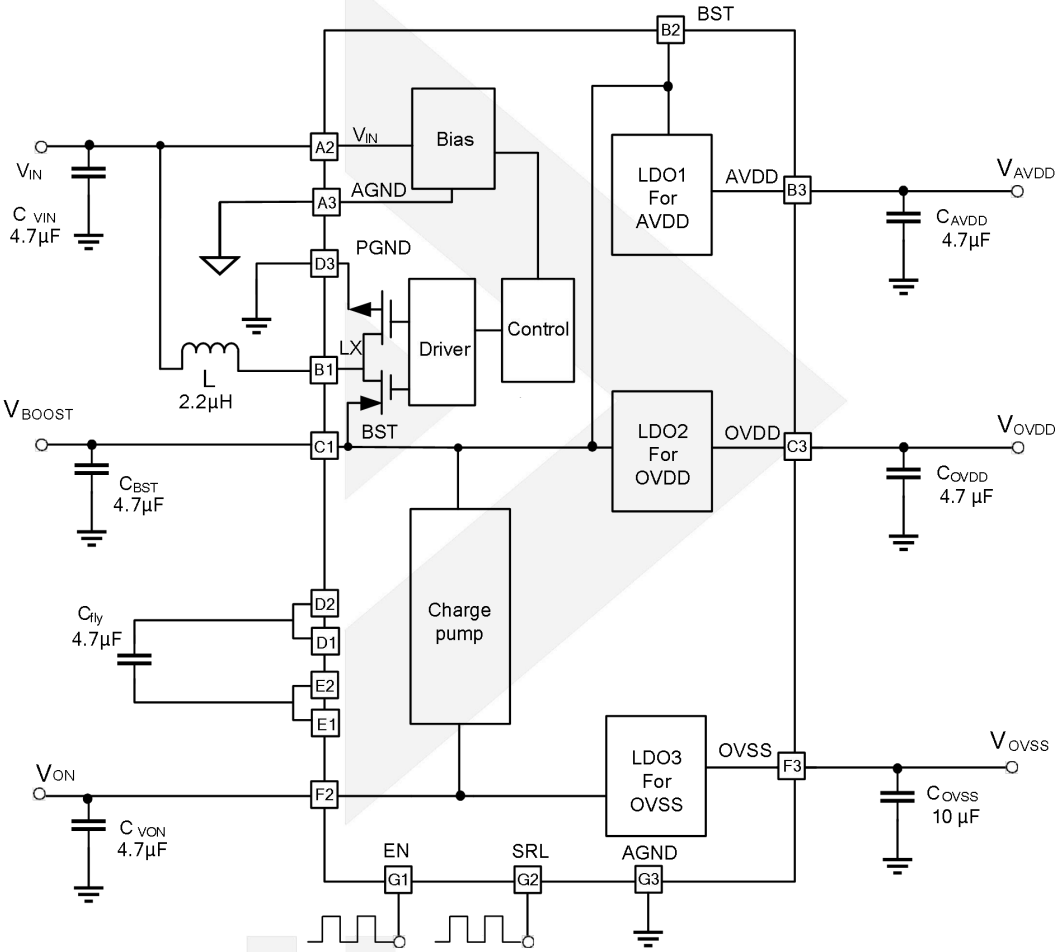
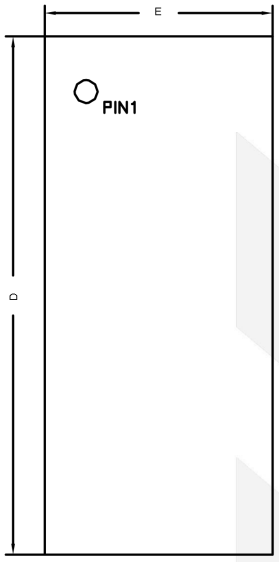
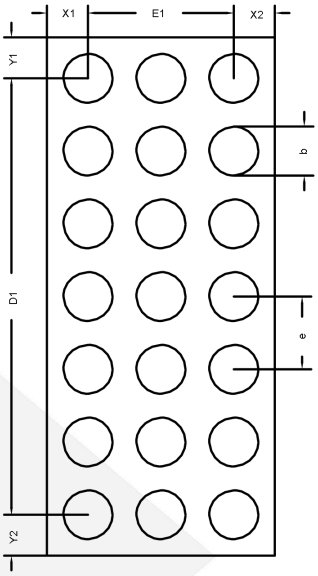


Figure 29. Typical applications W/T LED indication

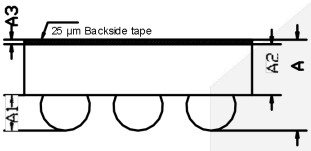
9. Physical Dimensions: WLCSP-21



TOP VIEW
(MARK SIDE)



BOTTOM VIEW
(BALL SIDE)



SIDE VIEW

Common Dimensions (Units of Measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.455	0.500	0.545
A1	0.175	0.195	0.215
A2	0.255	0.280	0.305
A3		0.025 REF	
D	2.820	2.850	2.880
D1		0.800 BSC	
E	1.220	1.250	1.280
E1		0.400 BSC	
b	0.250	0.270	0.290
e		0.400 BSC	
X1		0.225 REF	
X2		0.225 REF	
Y1		0.225 REF	
Y2		0.225 REF	

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