

DIO5718P

High Efficiency, 28 V, 2.0 A Synchronous Step-Down Regulator for Dimmable LED Driver

Features

- Wide input range: 4.5 V ~ 28 V
- Up to 2.0 A output current capability
- Low $R_{DS(ON)}$ for internal switches
High side / low side: 125 m Ω / 75 m Ω
- Fixed 1 MHz switching frequency
- Cycle by cycle 2.8 A valley current limit for low side
- High accuracy for low dimming scale
- Analog dimming with PWM input
- Over temperature protection
- Compact package: TSOT23-6, DFN2*1.5-6

Descriptions

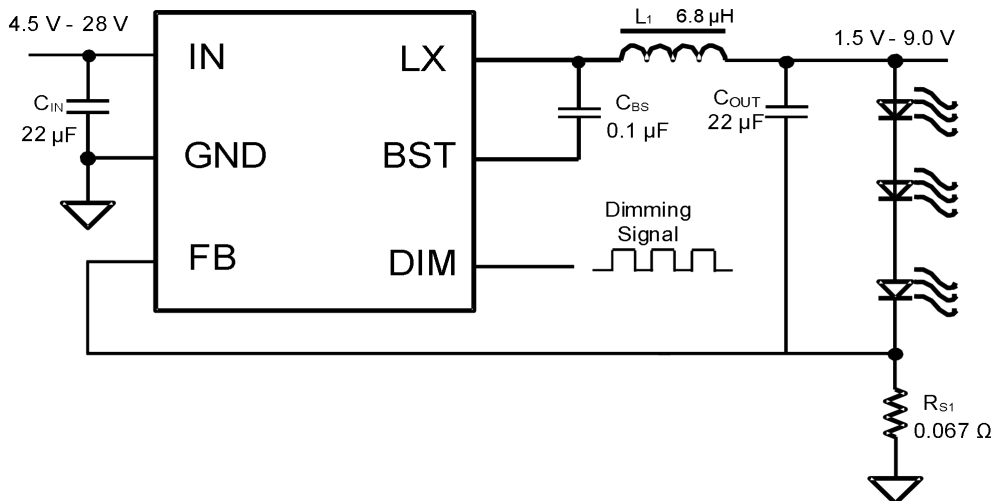
The DIO5718P is a high efficiency synchronous step-down LED regulator that achieves up to 2.0 A output current. It operates at 1 MHz and integrates two very low $R_{DS(ON)}$ power switches to minimize and reduce the external components.

It supports PWM dimming duty 1% ~ 100% to achieve dimmable LED lighting application.

Applications

- DVR or NVR (IP camera) system application
- 24VDC lighting

Typical Applications



Ordering Information

Order Part Number	Top Marking	MSL	RoHS	T _A	Package	
DIO5718PTST6	D8PW	3	Green	-40 to 85°C	TSOT23-6	Tape & Reel, 3000
DIO5718PLT6	8PYW	1	Green	-40 to 85°C	DFN2*1.5-6	Tape & Reel, 3000

Pin Assignment

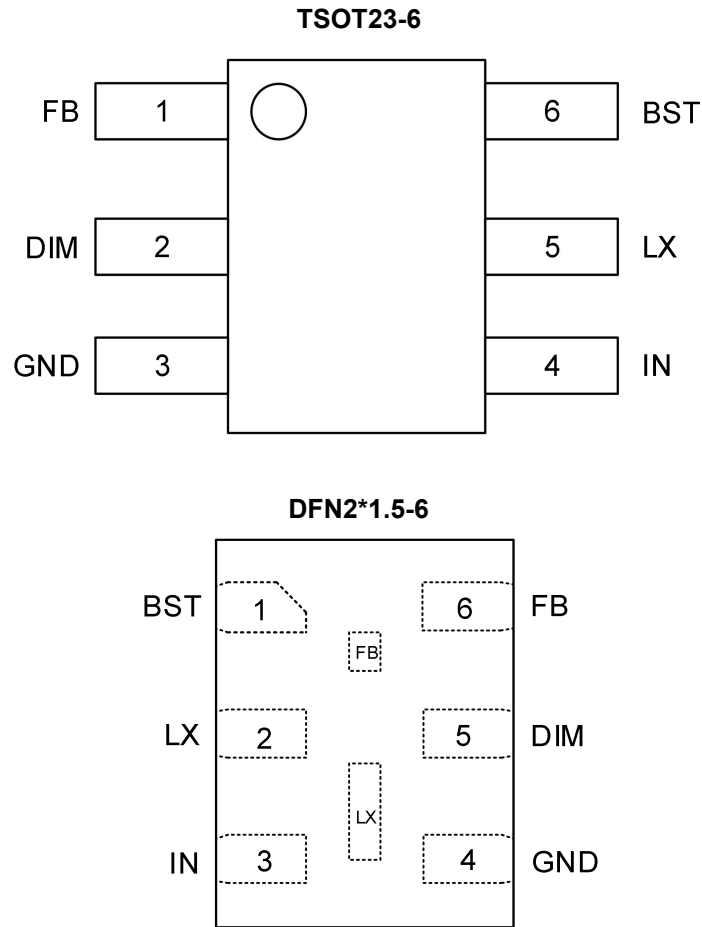


Figure 1. Top view

Pin Descriptions

Name	Description
FB	Output current feedback pin. The output current: $I_{OUT} = 0.1 \text{ V} / R_s$
DIM	Dimming signal input. The PWM dimming duty range: 1% ~ 100% Support the dimming frequency from 10 kHz to 100 kHz
GND	Ground pin
IN	Input supply pin
LX	Switching node pin. Connect this pin to the inductor
BST	Boot-strap pin. Supply for top side gate driver. Decouple this pin to LX with a 0.1 μF ceramic cap



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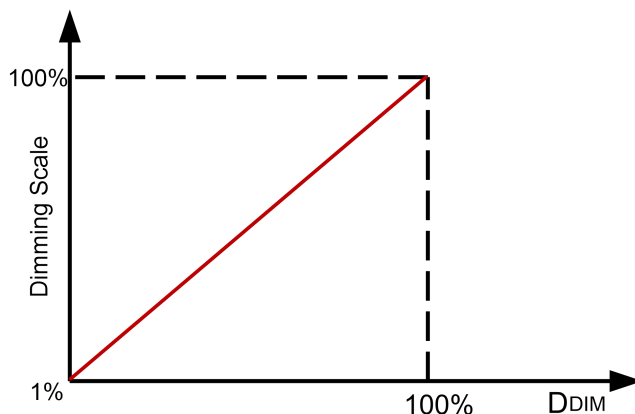


Figure 2. Ideal dimming curve of DIO5718P (dimming frequency 20 kHz)

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Rating	Unit
V_{IN}, V_{DIM}, V_{FB}	IN, DIM, FB		-0.3 to 38	V
V_{LX}	LX		-0.3 to 38	V
$V_{BST} - V_{LX}$	Voltage differential between BST and LX		-0.3 to 5.5	V
P_D	Power dissipation at $T_A = 25^\circ\text{C}$	TSOT23-6	1.5	W
		DFN2*1.5-6	1.39	
θ_{JA}	Package thermal resistance		66	$^\circ\text{C}/\text{W}$
θ_{JC}			15	$^\circ\text{C}/\text{W}$
T_J	Junction temperature range		-40 to 150	$^\circ\text{C}$
T_L	Lead temperature		260	$^\circ\text{C}$
T_{STG}	Storage temperature range		-65 to 150	$^\circ\text{C}$

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications.

Symbol	Parameter	Rating	Unit
V_{CC}	Supply voltage IN	4.5 to 28	V
T_J	Junction temperature range	-40 to 125	$^\circ\text{C}$



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Electrical Characteristics

Typical value: $V_{IN} = 12\text{ V}$, $V_{OUT} = 1.5\text{ V}$, $I_{OUT} = 2.0\text{ A}$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IN pin						
V_{IN}	Input voltage range		4.5		28.0	V
V_{UVLO}	IN UVLO rising threshold		4.0		4.3	V
V_{UVLO_HYS}	UVLO hysteresis			0.4		V
I_Q	Quiescent current	$V_{DIM} = 2\text{ V}$, $V_{FB} = 0.105\text{ V}$		0.3		mA
FB pin						
V_{FB}	Feedback reference voltage	$D_{DIM} = 100\%$	97	100	103	mV
V_{FB_MIN}	Feedback min reference voltage	$D_{DIM} = 1\%$		1		mV
Integrated power switches						
$R_{DS(ON)1}^{(1)}$	High side FET $R_{DS(ON)}$			125		m Ω
$R_{DS(ON)2}^{(1)}$	Low side FET $R_{DS(ON)}$			75		m Ω
$I_{LIM_LOW}^{(1)}$	Low side FET valley current limit			2.8		A
DIM pin						
$D_{DIM}^{(1)}$	PWM dimming duty range		1		100	%
V_{DIM_ON}	Dimming ON threshold		1.5			V
V_{DIM_OFF}	Dimming OFF threshold				0.4	V
BST pin						
$V_{BST_LX}^{(1)}$	Bias voltage for high FET driver	$4.5\text{ V} \leq V_{IN} \leq 28\text{ V}$		5		V
f_s	Operating frequency			1.0		MHz
$t_{ON_MIN}^{(1)}$	Min ON time			100		ns
D_{MAX}	Max duty cycle		88	92		%
Thermal shutdown						
$T_{SD}^{(1)}$	Thermal shutdown temperature			155		$^\circ\text{C}$
$T_{HYS}^{(1)}$	Thermal shutdown hysteresis			20		$^\circ\text{C}$

Note:

- (1) Guaranteed by design.
(2) Specifications subject to change without notice.

Typical Performance Characteristics

Typical value: $V_{IN} = 12\text{ V}$, $I_{OUT} = 1.5\text{ A}$, 3 piece I_R LED, $T_A = 25^\circ\text{C}$, unless otherwise specified.

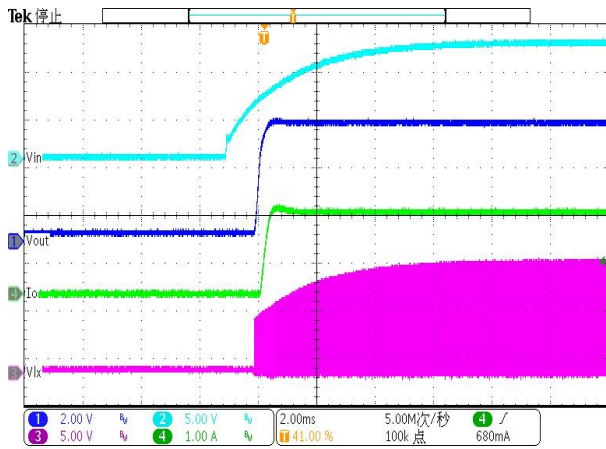


Figure 3. Start up

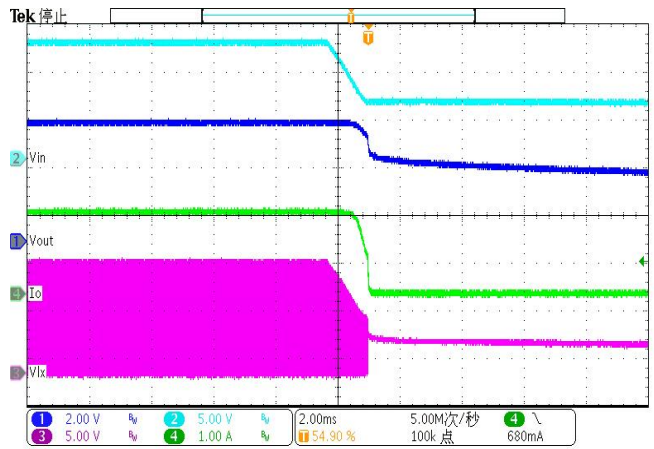


Figure 4. Shut down

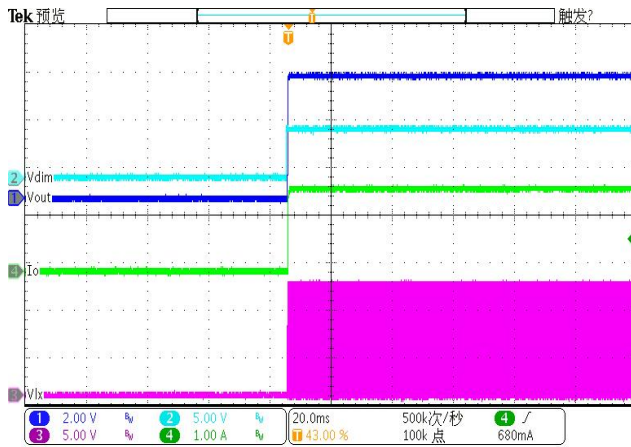


Figure 5. Dim on

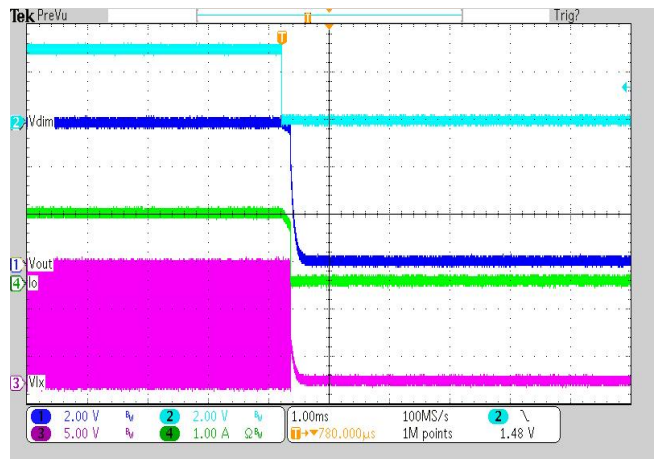


Figure 6. Dim off

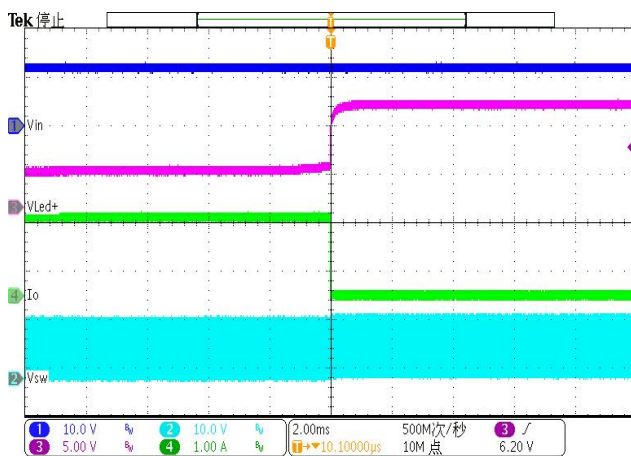


Figure 7. Open LED test

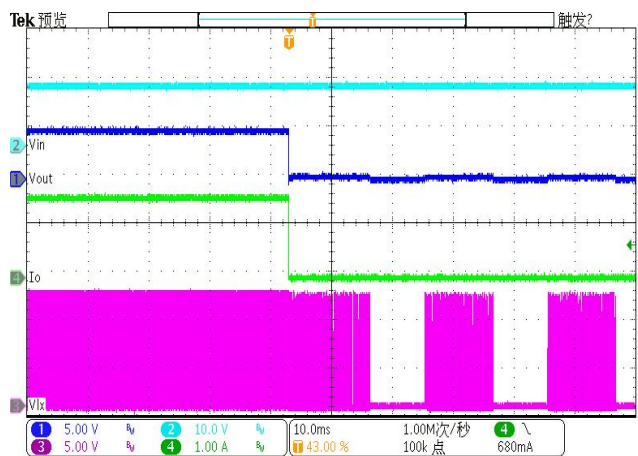


Figure 8. Short LED test

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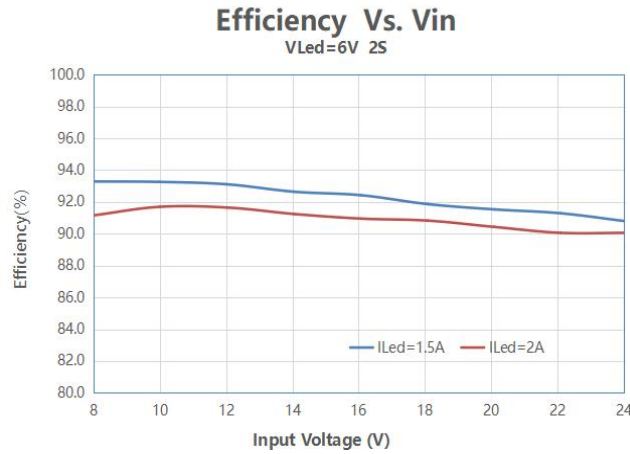
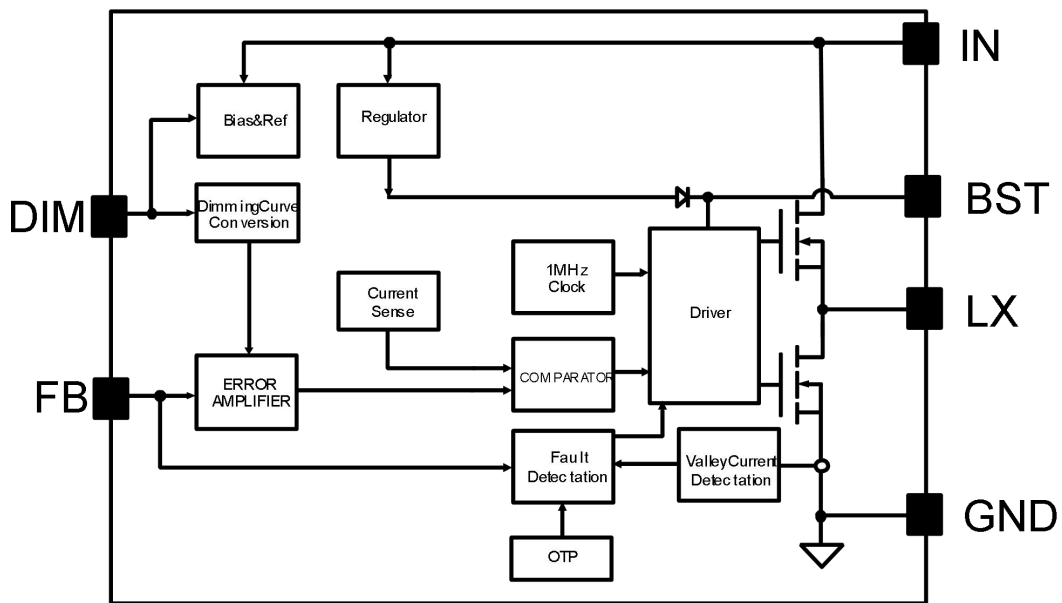


Figure 9. Efficiency vs. V_{IN}

Block diagram





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Operation

The DIO5718P is a 28 V and up to 2 A constant output current capability synchronous buck regulator IC that integrates two very low $R_{DS(ON)}$ power switches to minimize the switching transition loss and conduction loss. The high switching frequency is used to minimize the external inductor and capacitor size to reduce the cost and simplify the design. It supports the PWM dimming duty from 1% ~ 100% for DIM pin to achieve dimmable LED lighting application.

Application Information

Current sensing resistor R_{S1}

Choose the proper R_{S1} to program the output current I_{OUT} .

$$R_{S1} = \frac{0.1V}{I_{OUT}} \quad (1)$$

Input capacitor C_{IN}

The ripple current through input capacitor is calculated as:

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (2)$$

A typical X7R or better grade ceramic capacitor with suitable capacitance should be chosen to handle this ripple current well. To minimize the potential noise problem, place this ceramic capacitor close to the IN and GND pins. Caution should be taken to minimize the loop area formed by C_{IN} and IN / GND pin.

Output capacitor C_{OUT}

The output capacitor is selected to improve the loop stability and handle the output current ripple noise requirements. For the best performance, it is recommended to use a X7R or better grade ceramic capacitor greater than 10 μF capacitance.

Main inductor L_1

There are several considerations in choosing this inductor.

- 1) Select the proper inductance to ensure the loop stability.
- 2) It is suggested to choose the ripple current to be about 40% of the maximum output current as long as the loop stability allows. The inductance is calculated as:

$$L_1 = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN,MAX}}\right)}{f_s \times I_{OUT,MAX} \times 40\%} \quad (3)$$

Where f_s is the switching frequency and $I_{OUT,MAX}$ is the full scale LED current.

- 3) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.



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$$I_{SAT, MIN} > I_{OUT, MAX} + \frac{V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN, MAX}})}{2 \times f_s \times L_1} \quad (4)$$

Boost-strap capacitor C_{BST}

This capacitor provides the gate driver voltage for internal high side MOSEFET. A low ESR more than 100 nF ceramic capacitor connected between BST pin and LX pin is recommended.

Dimming performance

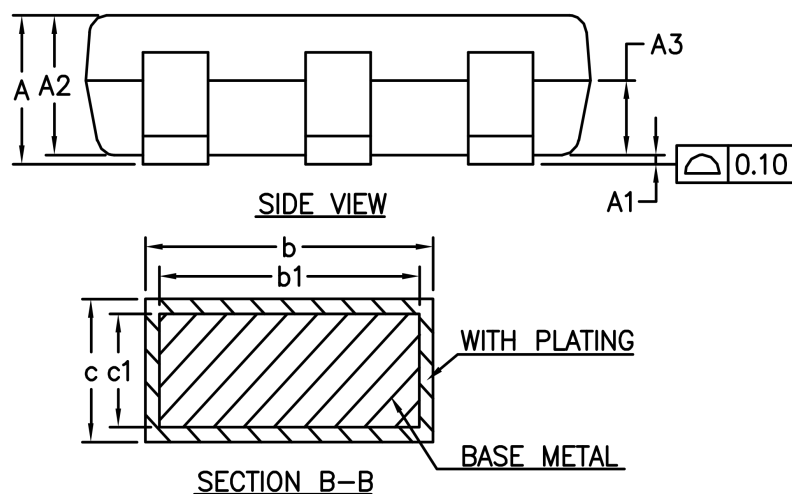
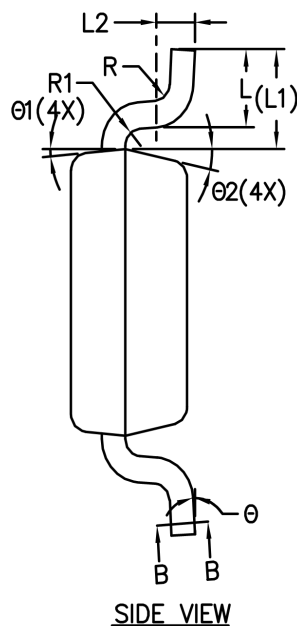
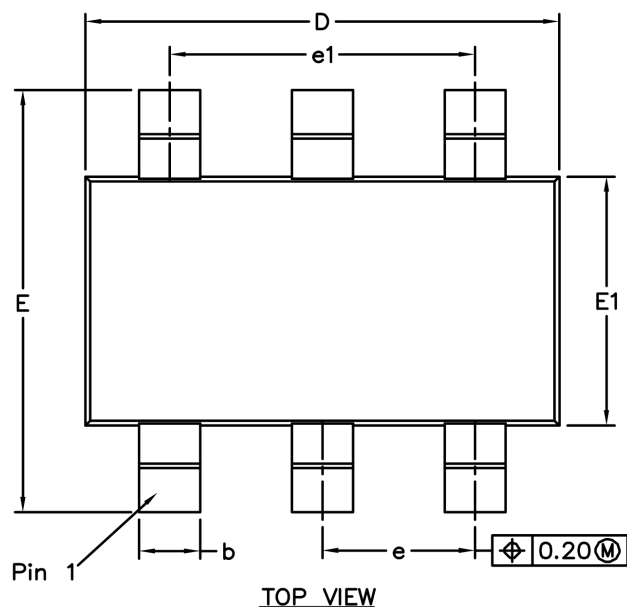
The DIM pin is used to regulate output current by the PWM signal, which supports the frequency from 10 kHz to 100 kHz. The logic high voltage is 1.5 V and the logic low voltage is 0.4 V. The DIM duty from 1% to 100%, the output current will be 1% ~ 100%, the ideal dimming curve shows as figure 2.

Layout

For the best efficiency and minimum noise problems,

- 1) It is desirable to maximize the PCB copper area connected to GND pin to achieve the best thermal and noise performance. If the board space allows, a ground plane is highly desirable.
- 2) C_{IN} must be close to the pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.
- 3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.
- 4) The FB pin must not be adjacent to the LX line on the PCB layout to avoid the noise problem.

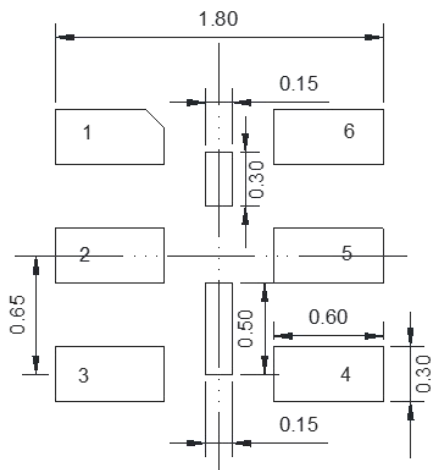
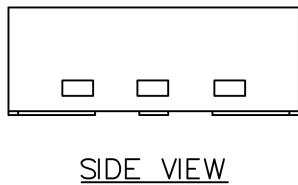
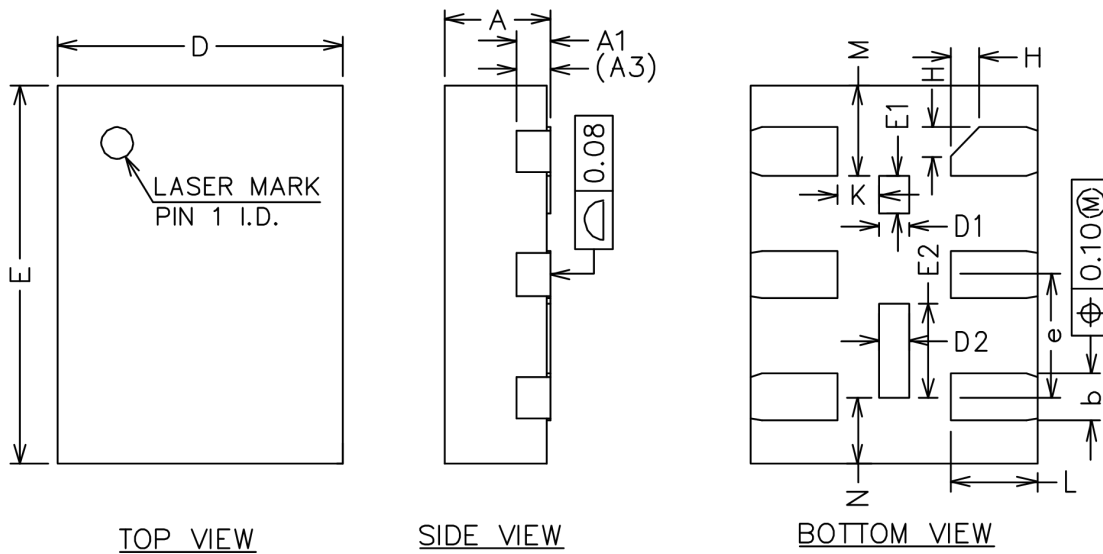
Physical Dimensions: TSOT23-6



Common Dimensions (Units of measure = Millimeter)			
Symbol	Min	Nom	Max
A	-	-	0.90
A1	0	-	0.15
A2	0.65	0.75	0.85
A3	0.35	0.40	0.45
b	0.36	-	0.50
b1	0.36	0.38	0.45
c	0.14	-	0.20
c1	0.14	0.15	0.16
D	2.85	2.95	3.05
E	2.60	2.80	3.00
E1	1.60	1.65	1.70
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
L	0.30	0.45	0.60
L1	0.575 REF		
L2	0.25 BSC		
R	-	-	0.25
R1	-	-	0.25
θ	0°	-	8°
θ1	3°	5°	7°
θ2	10°	12°	14°

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Physical Dimensions: DFN2*1.5-6



Common Dimensions (Units of Measure = Millimeter)			
Symbol	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	0.152 REF		
b	0.20	0.25	0.30
D	1.40	1.50	1.60
E	1.90	2.00	2.10
D1	0.05	0.15	0.25
E1	0.10	0.20	0.30
D2	0.05	0.15	0.25
E2	0.40	0.50	0.60
e	0.55	0.65	0.75
H	0.15 REF		
K	0.10	-	-
L	0.35	0.45	0.55
M	0.33	0.48	0.63
N	0.20	0.35	0.50



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CONTACT US

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