High Efficiency, 28 V, 2.0 A Sychronous Step-Down Regulator for Dimmable LED Driver

Features

- Wide input range: 4.2 V ~ 28 V
- Up to 2.0 A output current capability
- Low $R_{DS(ON)}$ for internal switches
  - High side/Low side: 125 mΩ/75 mΩ
- Fixed 1 MHz switching frequency
- Cycle by cycle 2.8 A valley current limit for low side
- Analog dimming with analog input
- High accuracy for low dimming scale
- Overtemperature protection
- Compact package: TSOT23-6

Applications

- DVR or NVR(IP Camera) system application
- 24VDC Lighting

Package Information

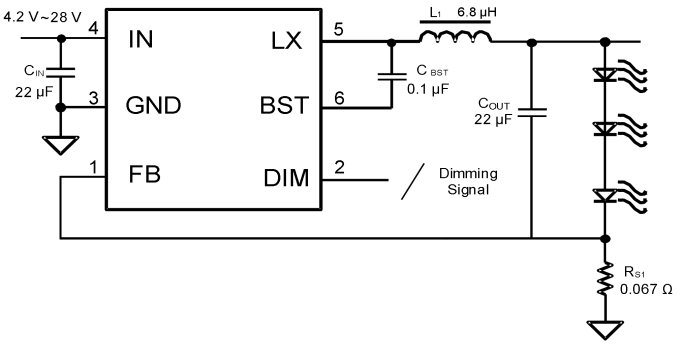
Part Number	Package	Body Size
DIO5718A	TSOT23-6	2.95 mm × 1.65 mm

Description

The DIO5718A is a high efficiency synchronous step-down LED regulator that achieves up to 2.0 A output current. It operates at 1 MHz and integrates two very low $R_{DS(ON)}$ power switches to minimize and reduce the external components.

It supports the ANALOG dimming function. The LED current is programmable through the external resistor.

Simplified Schematic



Ordering Information

Ordering Part No.	Top Marking	MSL	RoHS	T_A	Package	
DIO5718ATST6	18AW	3	Green	-40 to 85°C	TSOT23-6	Tape & Reel, 3000

If you encounter any issue in the process of using the device, please contact our customer service at marketing@dioo.com or phone us at (+86)-21-62116882. If you have any improvement suggestions regarding the datasheet, we encourage you to contact our technical writing team at docs@dioo.com. Your feedback is invaluable for us to provide a better user experience.

Table of Contents

List of Figures

1. Pin Assignment and Functions

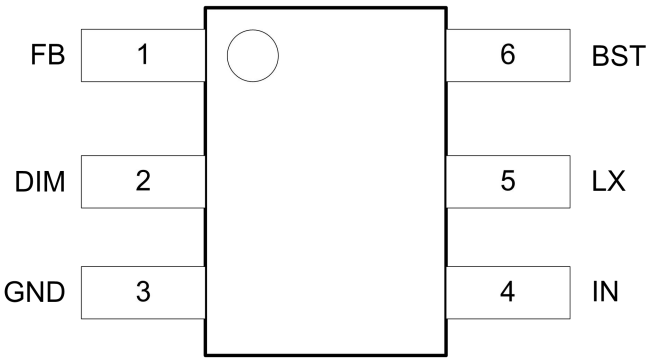


Figure 1. TSOT23-6 (Top view)

Name	Description
FB	Output current feedback pin. The output current: I_{OUT} = 0.1 V/ R_{S1}
DIM	Dimming signal input. When the DIM pin voltage rises from 0.65 V to 1.2 V, the LED current will change from 1% to 100% of the maximum LED current
GND	Ground pin
IN	Input supply pin. Decouple this pin to GND pin with a 1 μF ceramic cap
LX	Switching node pin. Connect this pin to the inductor
BST	Boot-strap pin. Supply for top side gate driver. Decouple this pin to LX with a 0.1 μF ceramic cap

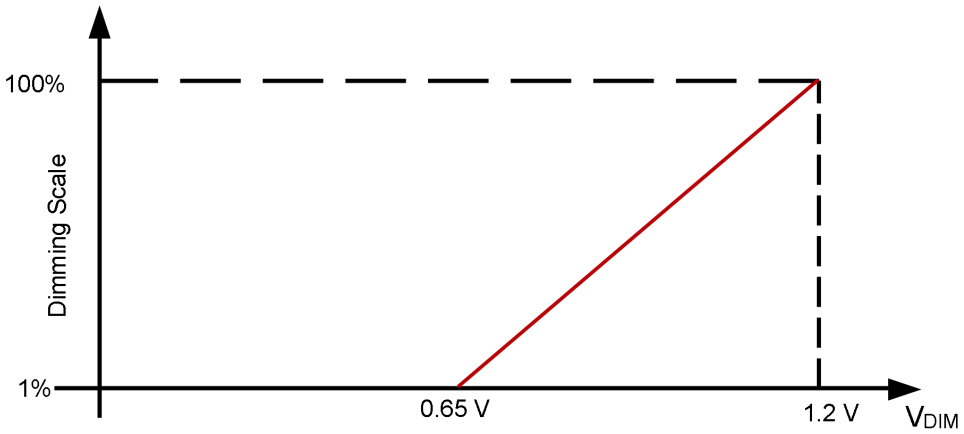


Figure 2. Ideal dimming curve of DIO5718A

2. Absolute Maximum Ratings

Exceeding the maximum ratings listed under Absolute Maximum Ratings when designing is likely to damage the device permanently. Do not design to the maximum limits because long-time exposure to them might impact the device's reliability. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Rating	Unit
$V_{IN, DIM, FB}$	IN, DIM, FB pin voltage.	-0.3 to 30	V
V_{LX}	LX pin voltage	-0.3 to 30	V
V_{BST-LX}	Voltage differential between BST and LX	-0.3 to 5.5	V
P_D	Power dissipation at T_A = 25°C	1.5	W
T_J	Junction temperature range	-40 to 150	°C
T_L	Lead temperature	260	°C
T_{STG}	Storage temperature range	-65 to 150	°C

3. Recommended Operating Conditions

Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Rating	Unit
V_{IN}	Input voltage	4.2 to 28	V
T_J	Junction temperature range	-40 to 125	°C

4. Thermal Considerations

The thermal resistance determines the heat insulation property of a material. The higher the thermal resistance is, the lower the heat loss. Accumulation of heat energy degrades the performance of semiconductor components.

Symbol	Metric	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15	°C/W

5. Electrical Characteristics

Typical value: V_{IN} = 12 V, V_{OUT} = 1.5 V, I_{OUT} = 1 A, T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IN pin						
V_{IN}	Input voltage range		4.2		28	V
V_{UVLO}	IN UVLO rising threshold		3.5		4.2	V
V_{UVLO_HYS}	UVLO hysteresis			0.4		V
I_Q	Quiescent current	V_{FB} = 0.105 V		0.5		mA
FB pin						
V_{FB}	Feedback reference voltage	V_{DIM} = 1.2 V	96	100	104	mV
		V_{DIM} = 0.65 V		3		mV
Integrated power switches						
$R_{DS(ON)1}$(1)	High side FET $R_{DS(ON)}$			125		mΩ
$R_{DS(ON)2}$(1)	Low side FET $R_{DS(ON)}$			75		mΩ
I_{LIM_LOW}(1)	Low side FET valley current limit			2.8		A
DIM pin						
V_{DIM}(1)	Analog dimming range		0.65		1.2	V
BST pin						
V_{BST_LX}(1)	Bias voltage for high FET driver	4.2 V ≤ V_{IN} ≤ 28 V		5		V
f_S	Operating frequency		0.8	1.0	1.2	MHz
t_{ON_MIN}(1)	Min ON time			80	100	ns
D_{MAX}	Max duty cycle		89	92		%
Thermal shutdown						
T_{SD}(1)	Thermal shutdown temperature			150		°C
T_{HYS}(1)	Thermal shutdown hysteresis			15		°C

Note:

(1) Guaranteed by design.

(2) Specifications subject to change without notice.

6. Typical Performance Characteristics

Typical value: V_{IN} = 12 V, I_{OUT} = 1 A, 3 pieces I_R LED, T_A = 25°C, unless otherwise specified.

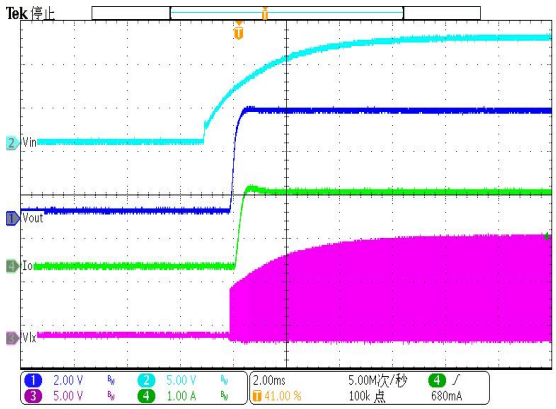


Figure 3. Start up

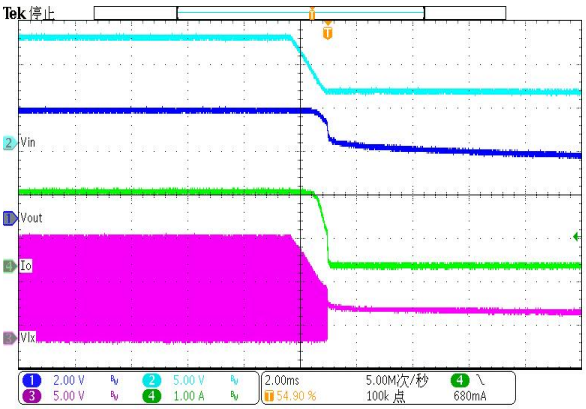


Figure 4. Shut down

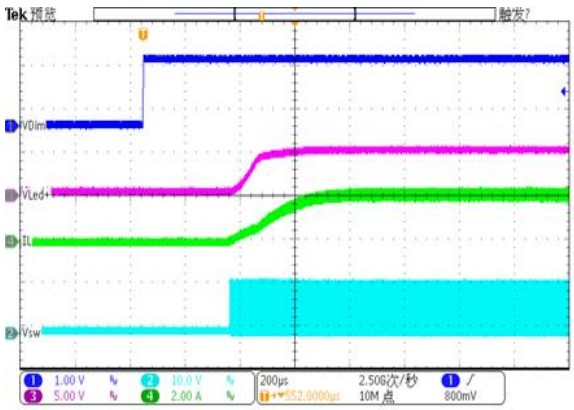


Figure 5. Dim on

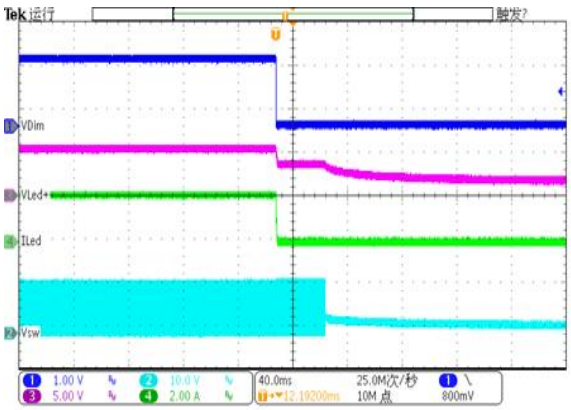


Figure 6. Dim off

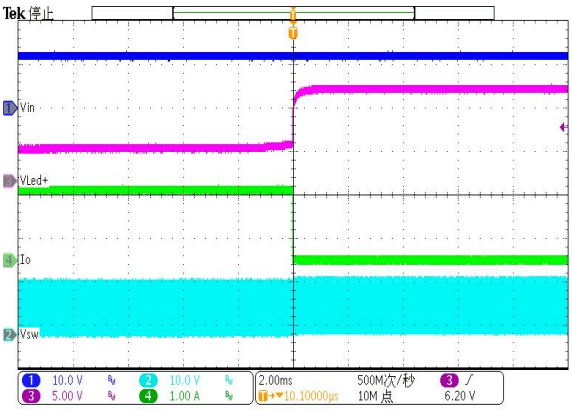


Figure 7. Open LED test

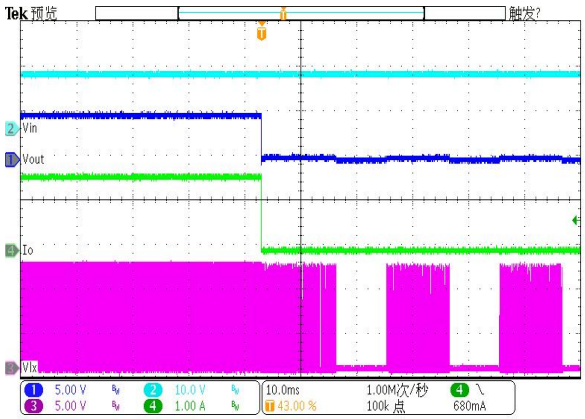
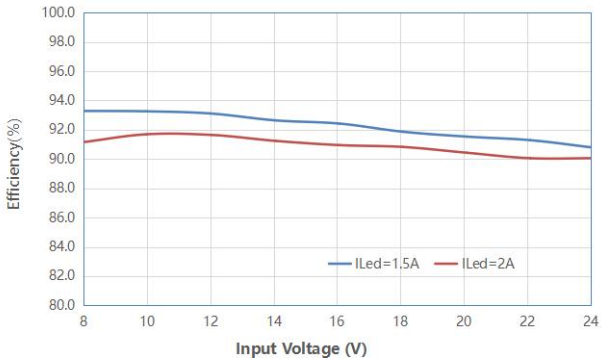


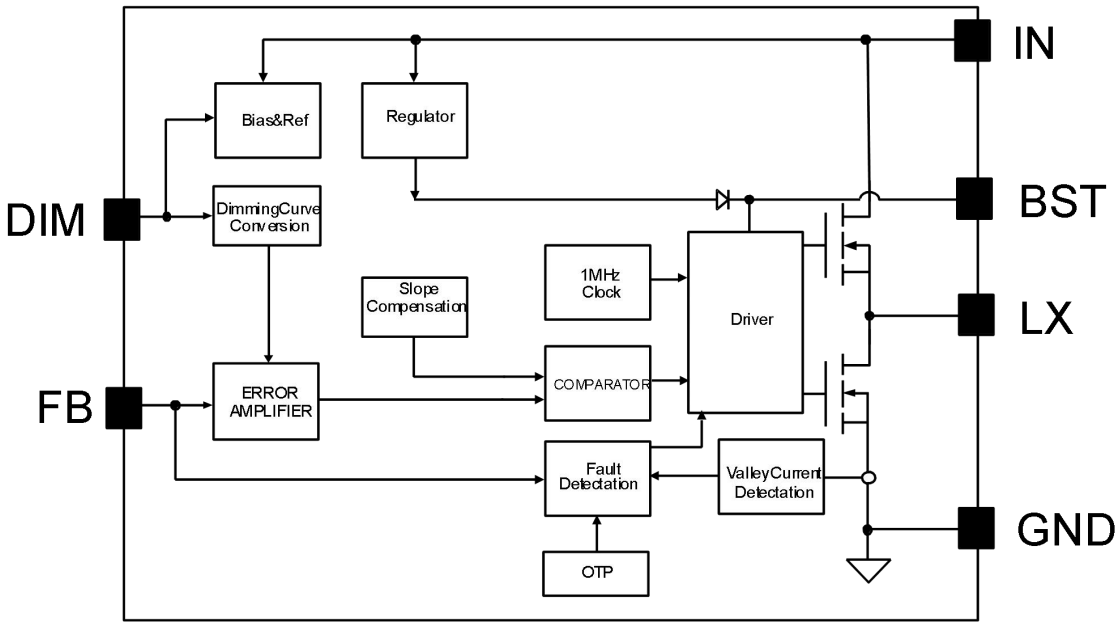
Figure 8. Short LED test



V_{LED} = 6 V, 2 s

Figure 9. Efficiency vs. V_{IN}

7. Block diagram



8. Application Information

Important notice: Validation and testing are the most reliable ways to confirm system functionality. The application information is not part of the specification and is for reference purposes only.

The DIO5718A is a 28 V and up to 2 A constant output current capability synchronous buck regulator IC that integrates two very low $R_{DS(ON)}$ power switches to minimize the switching transition loss and conduction loss. The high switching frequency is used to minimize the external inductor and capacitor size to reduce the cost and simplify the design. It supports the ANALOG dimming with the DIM pin voltage change from 0.65 V to 1.2 V.

8.1. Current sensing resistor R_{S1}

Choose the proper R_{S1} to program the output current I_{OUT}.

$$R_{S1} = \frac{0.1V}{I_{OUT}} \quad (1)$$

8.2. Input capacitor C_{IN}

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (2)$$

A typical X7R or better grade ceramic capacitor with suitable capacitance should be chosen to handle this ripple current well. To minimize the potential noise problem, place this ceramic capacitor really close to the IN and GND pins. Caution should be taken to minimize the loop area formed by C_{IN} and IN/GND pin.

8.3. Output capacitor C_{OUT}

The output capacitor is selected to improve the loop stability and handle the output current ripple noise requirements. For the best performance, it is recommended to use a X7R or better grade ceramic capacitor greater than 10 μF capacitance.

8.4. Main inductor L_1

There are several considerations in choosing this inductor.

1) Select the proper inductance to ensure the loop stability.

2) It is suggested to chose the ripple current to be about 40% of the maximum output current as long as the loop stability allows. The inductance is calculated as:

$$L_1 = \frac{V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN,MAX}})}{f_S \times I_{OUT,MAX} \times 40\%} \quad (3)$$

Where f_S is the switching frequency and $I_{OUT,MAX}$ is the full scale LED current.

3) The saturation current rating of the inductor must be selected to be grater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN,MAX}})}{2 \times f_S \times L_1} \quad (4)$$

8.5. Boot-strap capacitor C_{BST}

This capacitor provides the gate driver voltage for internal high side MOSFET. A low ESR more than 100 nF ceramic capacitor connected between BST pin and LX pin is recommended.

8.6. Dimming performance

The DIM pin is used to regulate output current by the ANALOG signal.

9. Layout

For the best efficiency and minimum noise problems,

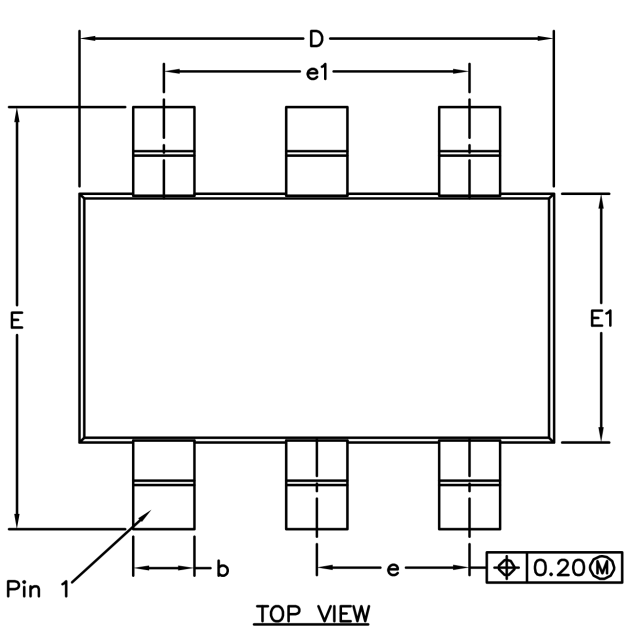
1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

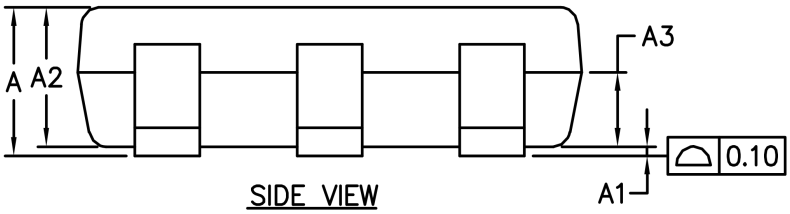
2) C_{IN} must be close to the pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

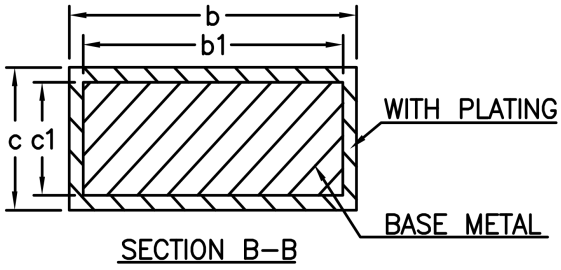
3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) The FB pin must not be adjacent to the LX line on the PCB layout to avoid the noised problem.

10. Physical Dimensions: TSOT23-6







Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	-	-	0.90
A1	0	-	0.15
A2	0.65	0.75	0.85
A3	0.35	0.40	0.45
b	0.36	-	0.50
b1	0.36	0.38	0.45
c	0.14	-	0.20
c1	0.14	0.15	0.16
D	2.85	2.95	3.05
E	2.60	2.80	3.00
E1	1.60	1.65	1.70
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
L	0.30	0.45	0.60
L1	0.575 REF		
L2	0.25 BSC		
R	-	-	0.25
R1	-	-	0.25
θ	0°	-	8°
θ1	3°	5°	7°
θ2	10°	12°	14°

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