5.5 V, 3 A, 1 MHz High-Efficiency, Constant On-Time Synchronous, Step-Down Converter

Features

- Low $R_{DS(ON)}$ for internal switches (top/bottom) 80 mΩ / 50 mΩ, 3.0 A
- 2.4 V to 5.5 V input voltage range
- 7 µA typical quiescent current
- High switching frequency 1 MHz minimizes the external components
- 100% dropout operation
- Output discharge with a R_{DIS} of 50 Ω
- Feedback reference voltage: 0.6 V
- Power-good output
- Reliable short-circuit protection: hiccup mode protection
- Fixed frequency COT architecture achieve ultra fast transient response
- Internal soft start limits the inrush current
- Operating temperature range: -40°C to 85°C

Applications

- LCD TVs
- Set top boxes
- Internet PCs
- Mini-notebook PCs
- Access point routers

Package Information

Part Number	Package	Body Size
DIO60830	DFN-8	2.0 mm × 2.0 mm
	DFN-10	3.0 mm × 3.0 mm
	EP-SOIC8	3.9 mm × 4.9 mm
	SOT563	1.2 mm × 1.6 mm

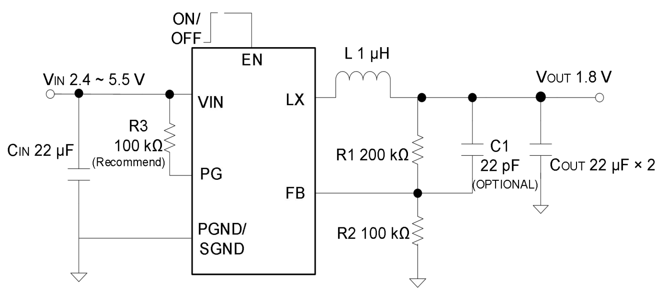
Description

The DIO60830 is a high-efficiency synchronous step-down DC-DC regulator. The DIO60830 can achieve up to 3 A continuous output current from a 2.4 V to 5.5 V input voltage. The output voltage can be regulated to as low as 0.6 V.

The DIO60830 integrates the main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. Low output voltage ripple and small external inductor and capacitor sizes are achieved with 1 MHz switching frequency. Constant-on-time control provides a fast transient response and eases loop stabilization.

The DIO60830 is ideal for a wide range of applications, including LCD TVs, set top boxes and internet PCs.

Simplified Schematic



Ordering Information

Ordering Part No.	Top Marking	MSL	RoHS	T_A	Package	
DIO60830CN8	VH3V	3	Green	-40 to 85°C	DFN2*2-8	Tape & Reel, 3000
DIO60830CD10	DVH3V	3	Green	-40 to 85°C	DFN3*3-10	Tape & Reel, 5000
DIO60830XS8	DVH3V	3	Green	-40 to 85°C	EP-SOIC8	Tape & Reel, 2500
DIO60830SH3	WCV	3	Green	-40 to 85°C	SOT563	Tape & Reel, 5000

If you encounter any issue in the process of using the device, please contact our customer service at marketing@dioo.com or phone us at (+86)-21-62116882. If you have any improvement suggestions regarding the datasheet, we encourage you to contact our technical writing team at docs@dioo.com. Your feedback is invaluable for us to provide a better user experience.

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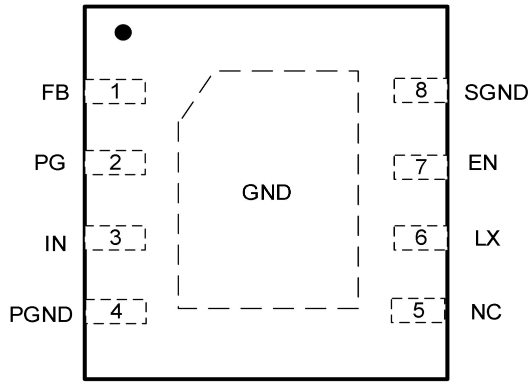
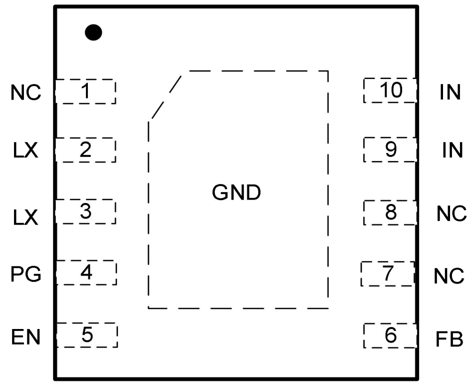
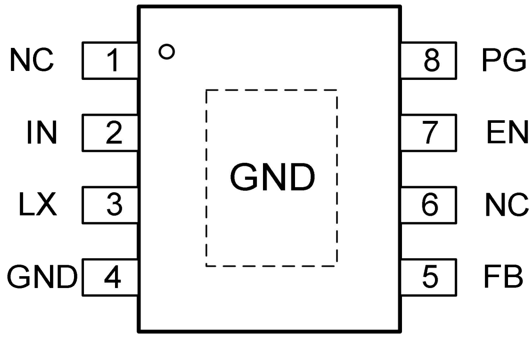
1. Pin Assignment and Functions



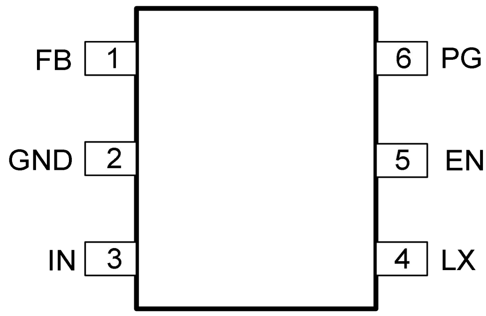
DFN2*2-8 (Top view)



DFN3*3-10 (Top view)



EP-SOIC8 (Top view)



SOT563 (Top view)

Pin Name	Description
FB	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in the pin assignment) to program the output voltage: $V_{OUT} = 0.6 \times (1 + R1/R2)$.
PG	Power good indicator. When the output voltage exceeds 95% of regulation point, it becomes open drain; low otherwise.
IN	Power input.
PGND	Power ground. Must connect this pin to the system ground on the board.
NC	No connection.
LX	Inductor pin. Connect this pin to the switching node of inductor.
EN	Enable control. Pull high to turn on. Do not leave it floating.
SGND	Signal ground. Must connect this pin to the system ground on the board.

2. Absolute Maximum Ratings

Exceeding the maximum ratings listed under Absolute Maximum Ratings when designing is likely to damage the device permanently. Do not design to the maximum limits because long-time exposure to them might impact the device's reliability. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Rating	Unit
V_{CC}	Supply voltage (V+ – V-)	-0.3 to 6.0	V
V_{FB}	Enable, FB voltage	-0.3 to V_{IN} + 0.6	V
P_D	Power dissipation, T_A = 25°C	1	W
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Junction temperature range	150	°C
T_L	Lead temperature range	260	°C
	Dynamic LX voltage in 50 ns duration	VIN + 3 to GND - 4	V

3. Recommended Operating Conditions

Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Rating	Unit
V_{CC}	Supply voltage	2.4 to 5.5	V
T_J	Junction temperature range	-40 to 125	°C
T_A	Ambient temperature range	-40 to 85	°C

4. ESD Ratings

When a statically-charged person or object touches an electrostatic discharge sensitive device, the electrostatic charge might be drained through sensitive circuitry in the device. If the electrostatic discharge possesses sufficient energy, damage might occur to the device due to localized overheating.

Model	Condition	Value	Unit
ESD	HBM, JEDEC:JS-001	±2000	V
	CDM, JEDEC:JS-002	±2000	

5. Thermal Considerations

The thermal resistance determines the heat insulation property of a material. The higher the thermal resistance is, the lower the heat loss. Accumulation of heat energy degrades the performance of semiconductor components.

Symbol	Parameter		Value	Unit
$R_{\theta JA}$	Junction-to-air thermal resistance	DFN2*2-8	120	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	DFN2*2-8	8.2	

6. Electrical Characteristics

V_{IN} = 3.6 V, V_{OUT} = 0.9 V, L = 1 μH, C_{OUT} = 2 × 22 μF, T_A = 25°C, I_{MAX} = 1 A, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage range		2.4		5.5	V
I_Q	Quiescent current	I_{OUT} = 0, V_{FB} = V_{REF} × 105%		7		μA
I_{SHDN}	Shutdown current	EN = 0		0.1	1	μA
V_{REF}	Feedback reference voltage		0.588	0.6	0.612	V
I_{FB}	FB input current	V_{FB} = V_{IN}	-50		50	nA
$R_{DS(ON)}$, P	PFET R_{ON}	V_{IN} = 5 V, I_{OUT} = 100 mA		80		mΩ
$R_{DS(ON)}$, N	NFET R_{ON}	V_{IN} = 5 V, I_{OUT} = 100 mA		50		mΩ
I_{LIM}	PFET current limit		3.5			A
V_{ENH}	EN rising threshold		0.825			V
V_{ENL}	EN falling threshold				0.4	V
V_{UVLO}	Input UVLO threshold				2.4	V
V_{HYS}	UVLO hysteresis			0.15		V
R_{DSC}	Output discharge switch on resistance			50		Ω
f_{OSC}	Oscillator frequency	I_{OUT} = 1 A		1		MHz
	PG rising delay time(1)			50		μs
	PG falling delay time(1)			30		μs
V_{FB,UV_R}	Undervoltage PG rising threshold			0.58		V
V_{FB,UV_F}	Undervoltage PG falling threshold			0.55		V
V_{FB,OV_R}	Overvoltage PG rising threshold			0.63		V
V_{FB,OV_F}	Overvoltage PG falling threshold			0.72		V
	Min on-time			70		ns
	Max duty-cycle		100			%
t_{SS}	Soft-start time			1.2		ms
T_{SD}	Thermal shutdown temperature			150		°C

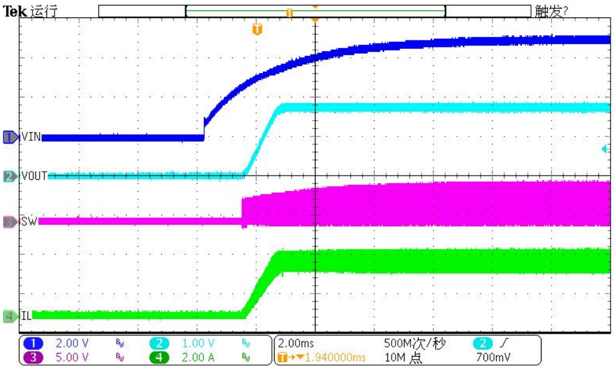
Notes:

(1) Guaranteed by design.

(2) Specifications subject to change without notice.

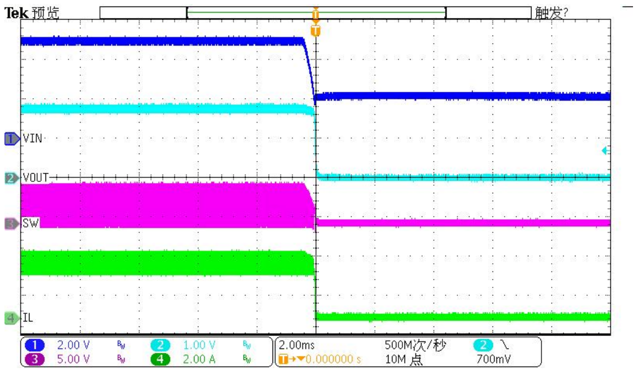
7. Typical Performance Characteristic

V_{IN} = 5 V, V_{OUT} = 1.8 V, L = 1 μH, C_{IN} = 22 μF, C_{OUT} = 22 μF × 2, T_A = 25°C, unless otherwise specified.



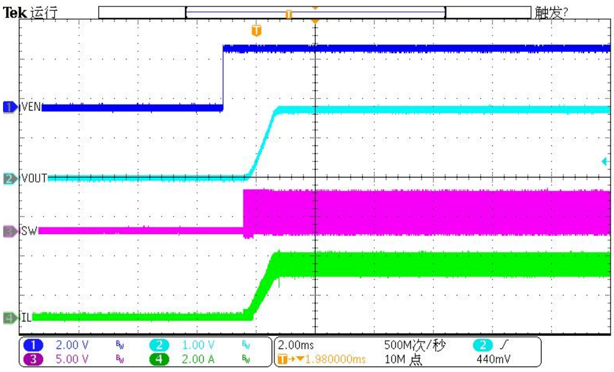
V_{IN} = 5 V, V_{OUT} = 1.8 V with 3 A load

Figure 1. V_{IN} start



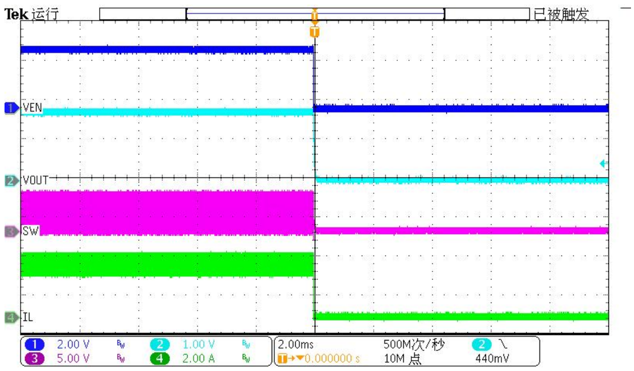
V_{IN} = 5 V, V_{OUT} = 1.8 V with 3 A load

Figure 2. V_{IN} drop



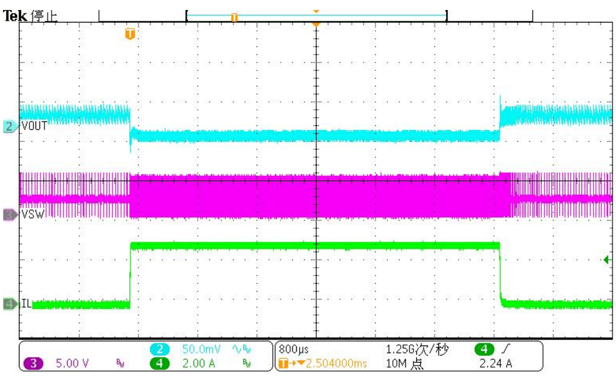
V_{IN} = 5 V, V_{OUT} = 1.8 V with 3 A load

Figure 3. V_{EN} start



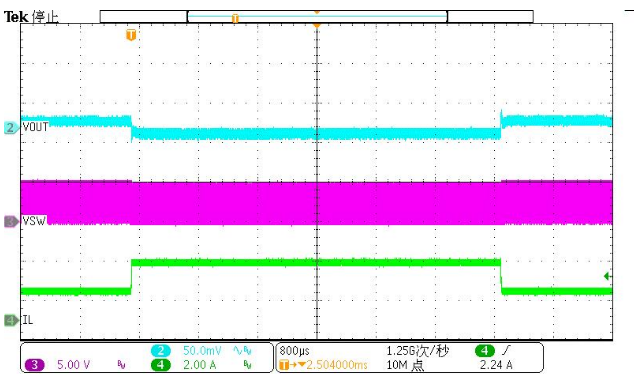
V_{IN} = 5 V, V_{OUT} = 1.8 V with 3 A load

Figure 4. V_{EN} drop



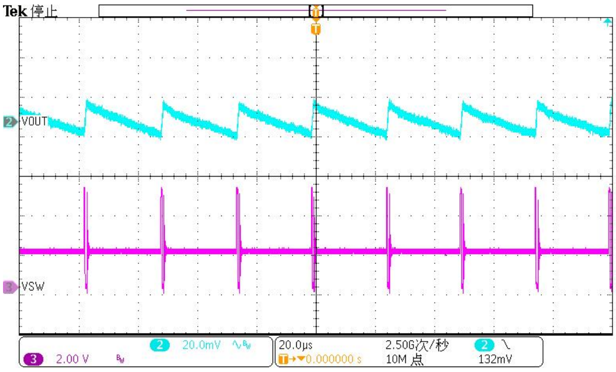
V_{IN} = 5 V, V_{OUT} = 1.8 V, with 0.001 A ~ 3 A load

Figure 5. Load transient



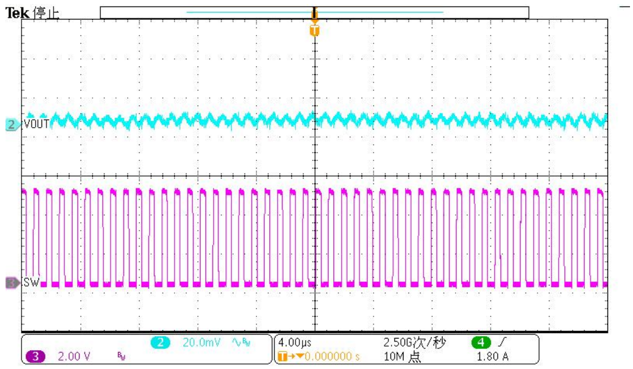
V_{IN} = 5 V, V_{OUT} = 1.8 V, with 1.5 A ~ 3 A load

Figure 6. Load transient



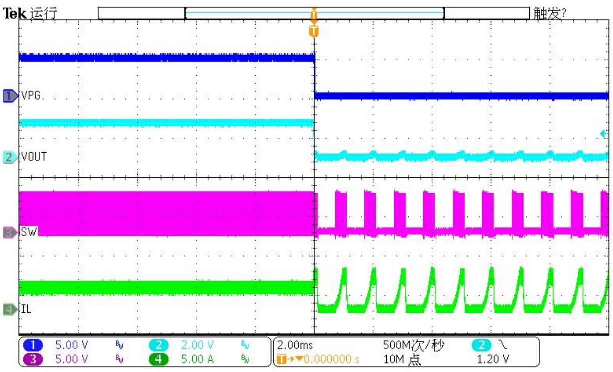
V_{IN} = 5 V, V_{OUT} = 1.8 V with 20 mA load

Figure 7. Ripple



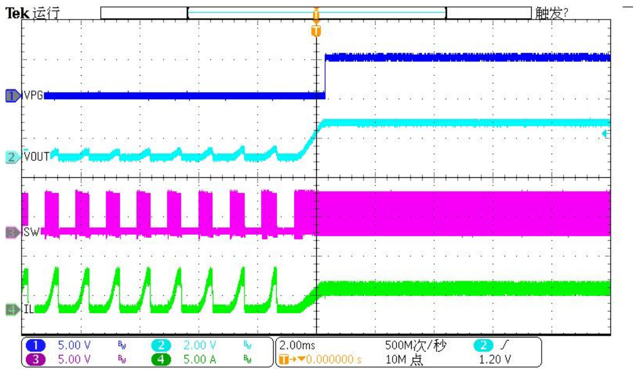
V_{IN} = 5 V, V_{OUT} = 1.8 V with 3 A load

Figure 8. Ripple



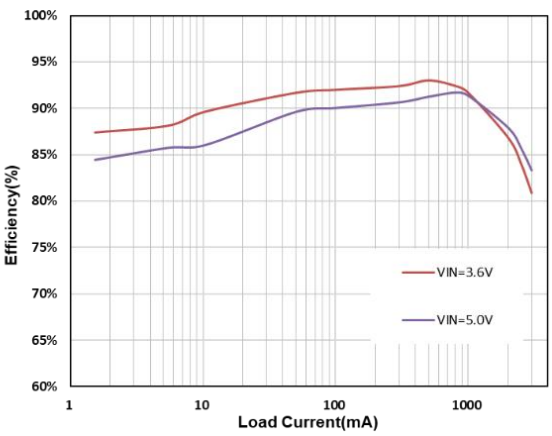
V_{IN} = 5 V, V_{OUT} = 1.8 V, with 3 A load → short

Figure 9. Short circuit protection



V_{IN} = 5 V, V_{OUT} = 1.8 V, with short → 3 A load

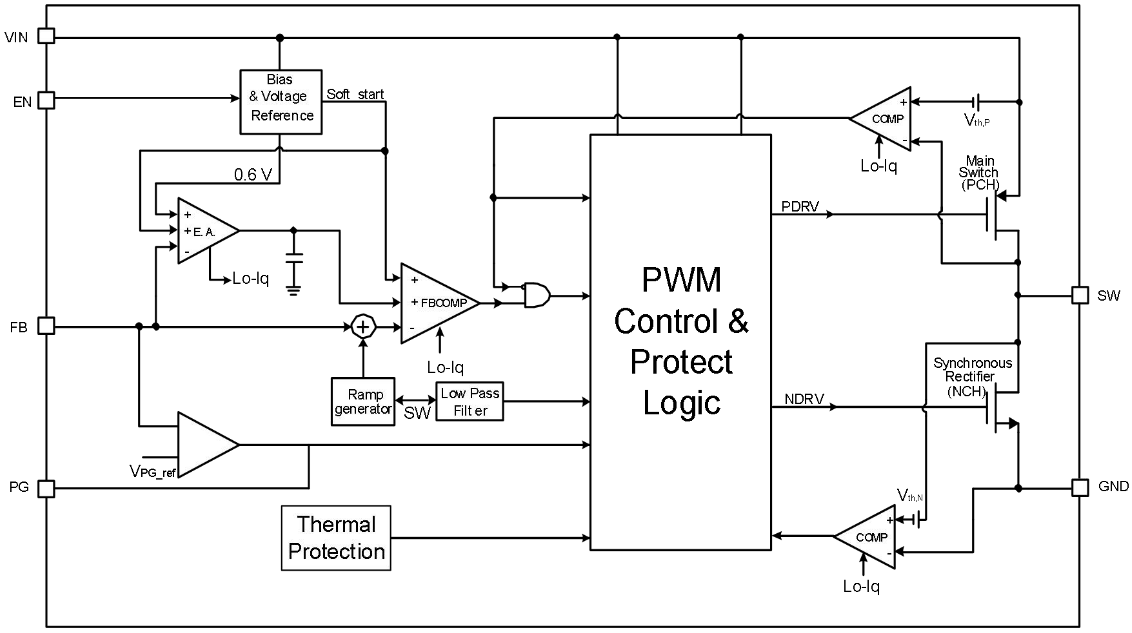
Figure 10. Short circuit protection



V_{OUT} = 1.8 V

Figure 11. Efficiency vs. Load current

8. Block Diagram



9. Application Information

Important notice: Validation and testing are the most reliable ways to confirm system functionality. The application information is not part of the specification and is for reference purposes only.

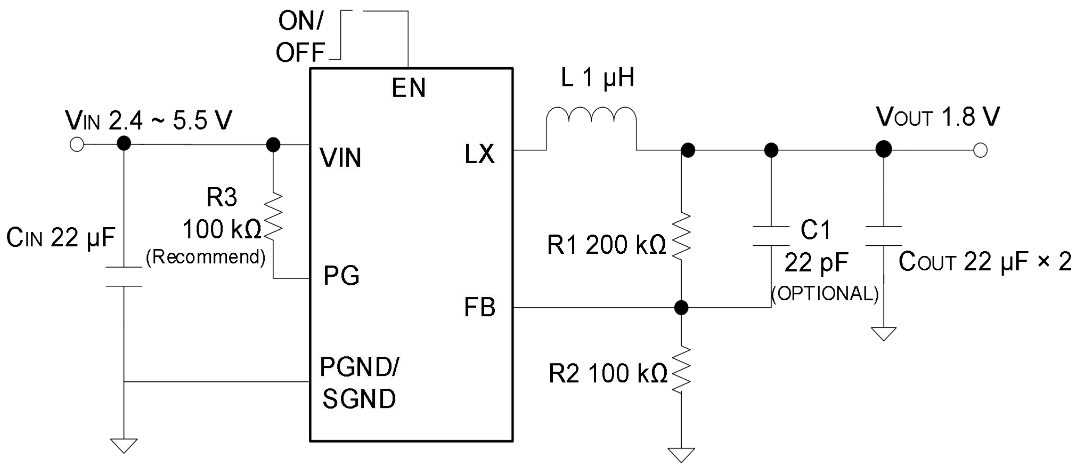


Figure 12. Typical application

The DIO60830 is a synchronous buck regulator IC that integrates the adaptive constant on-time (COT) control, and top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra-low $R_{DS(ON)}$ power switches and proprietary COT control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size, thus achieving the minimum solution footprint.

Because of the high integration in the DIO60830 IC, the application circuit based on this regulator IC is rather simple. Only the input capacitor, C_{IN}, output capacitor, C_{OUT}, output inductor, L, feedback capacitor, C_1, and feedback resistors (R1 and R2) need to be selected for the targeted application specifications.

9.1. Enable

When disabled, the device shutdown supply current is only 0.1 µA. When applying a voltage greater than the EN logic high threshold (typically 0.65 V, rising), the DIO60830 enables all functions and the device initiates the soft-start phase. The DIO60830 has a built-in 1.2 ms soft-start time to prevent output voltage overshoot and inrush current. When the EN voltage falls below its logic low threshold (typically 0.58 V, falling), the device operation is disabled and the 50 Ω active discharge is enabled to discharge the output voltage to ground.

9.2. Power-good (PG) indicator

The PG pin of DIO60830 is actively held low during the soft-start period until the output voltage reaches 95% of its target value. When the output voltage is outside of its regulation by +20% or -10%, PG pulls low until the output returns within 5% of its set value. The PG rising edge transition is delayed by 50 μs.

9.3. Undervoltage lockout

Undervoltage lockout protects the IC from insufficient input voltages. The DIO60830 is active if the input voltage rises above 2.25 V (typ). The DIO60830 is disabled if the input voltage falls below 2.1 V (typ). In this UVLO event, both the high-side and low-side power MOSFETs turn off.

9.4. Thermal shutdown

If the junction temperature of the device reaches the thermal shutdown limit of 150°C, the DIO60830 shuts down both high-side and low-side power MOSFETs. When the junction temperature reduces to the required level (130°C typical), the device initiates a normal power-up cycle with soft-start.

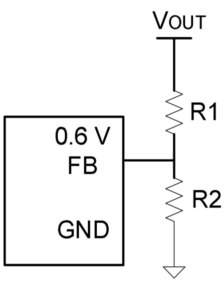
9.5. Switch current limit and short-circuit protection

The protection function prevents the device from drawing excessive current in case of externally-caused overcurrent or short-circuit conditions. If the current limit threshold is reached, the device delivers its maximum output current. Detecting this condition for 32 switching cycles, the device turns off the high-side MOSFET for about 300 μs and then restarts again with a soft-start cycle. As long as the overload condition is present, the device hiccups that way, limiting the output power.

9.6. Feedback resistor dividers R1 and R2

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, choose large resistance values for both R1 and R2. A value of between 100 kΩ and 1 MΩ is highly recommended for both resistors. If R1 is 120 kΩ, then R2 can be calculated from Equation (1).

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} \times R_1 \quad (1)$$



9.7. Input capacitor C_{IN}

With the maximum load current at 3 A, the maximum ripple current through the input capacitor is about 1.5 A. A typical X7R or better grade ceramic capacitor with 6 V rating and greater than 22 μF capacitance can handle this ripple current well. To minimize the potential noise problem, place this ceramic capacitor really close to the IN and GND pins. Carefully minimize the loop area formed by C_{IN}, and IN/GND pins.

9.8. Output capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady-state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, use X5R or a better grade ceramic capacitor with 6 V rating and greater than 10 μF capacitance.

9.9. Output inductor L

There are several considerations in choosing this inductor.

(1) Choose the inductance to provide the desired ripple current. Choose the ripple current to be approximately 40% of the maximum output current. The inductance is calculated from Equation (2).

$$L = \frac{V_{OUT} \times (1 - V_{OUT} / V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%} \tag{2}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current. The DIO60830 regulator IC is quite tolerant of different ripple current amplitudes. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

(2) The saturation current rating of the inductor must be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT} \times (1 - V_{OUT} / V_{IN,MAX})}{2 \times f_{SW} \times L} \tag{3}$$

(3) The DC resistance (DCR) of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Choose an inductor with a DCR lower than 50 mΩ to achieve a good overall efficiency.

9.10. Load transient considerations

The DIO60830 regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 22 pF ceramic capacitor in parallel with R1 may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.

10. Layout Design

The layout design of the DIO60830 regulator is relatively simple. For the best efficiency and minimum noise problems, place four components close to the IC: C_{IN}, L, R1, and R2.

(1) Maximize the PCB copper area connected to the GND pin to achieve the best thermal and noise performance. If the board space allows, a ground plane is highly desirable.

(2) Place C_{IN} close to pins IN and GND. Minimize the loop area formed by C_{IN} and GND.

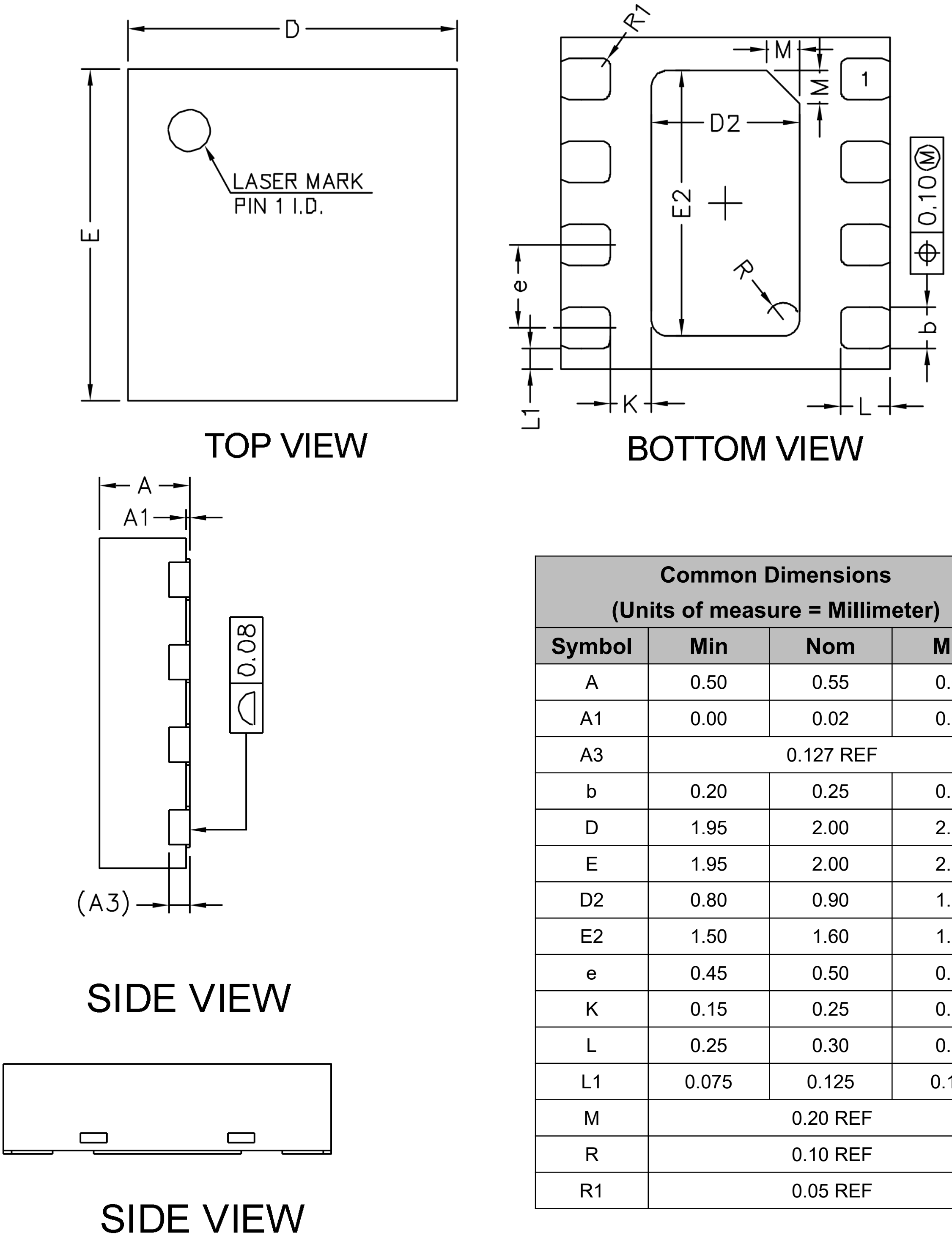
(3) Minimize the PCB copper area associated with LX pin to avoid the potential noise problem.

(4) Avoid placing the components R1 and R2 and the trace connected to the FB pin adjacent to the LX net on the PCB layout to prevent the noise problem.

(5) If the system chip interfaced with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull-down 1 MΩ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

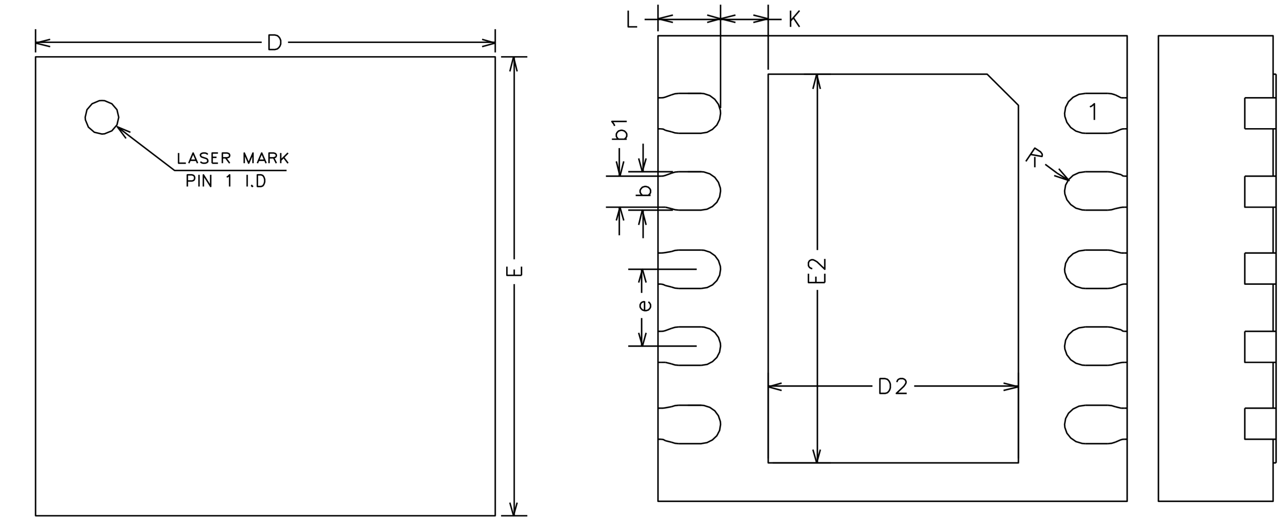
11. Physical Dimensions:

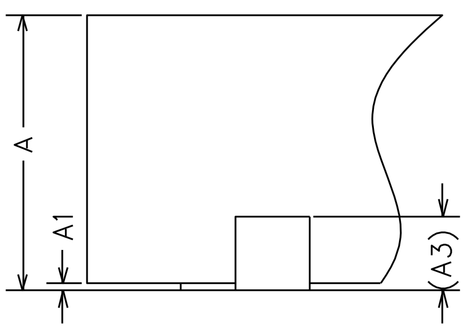
11.1. DFN2*2-8



Common Dimensions (Units of measure = Millimeter)			
Symbol	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	0.127 REF		
b	0.20	0.25	0.30
D	1.95	2.00	2.05
E	1.95	2.00	2.05
D2	0.80	0.90	1.00
E2	1.50	1.60	1.70
e	0.45	0.50	0.55
K	0.15	0.25	0.35
L	0.25	0.30	0.35
L1	0.075	0.125	0.175
M	0.20 REF		
R	0.10 REF		
R1	0.05 REF		

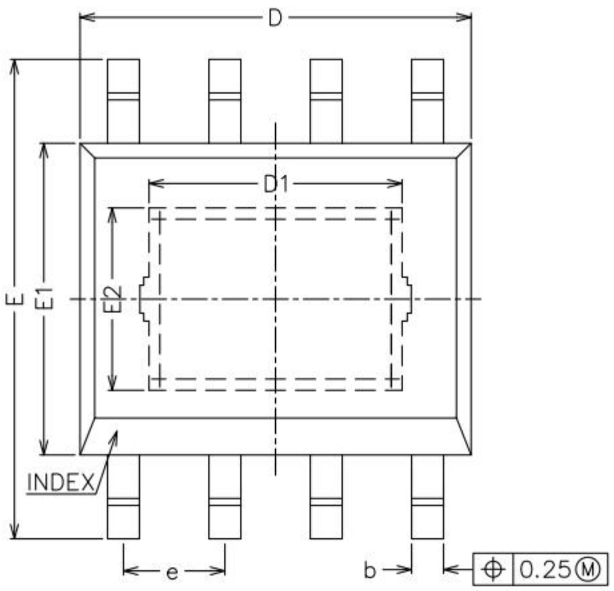
11.2. DFN3*3-10

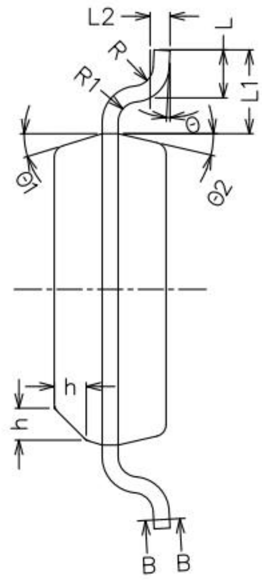


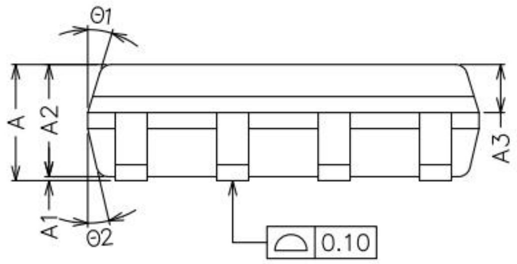


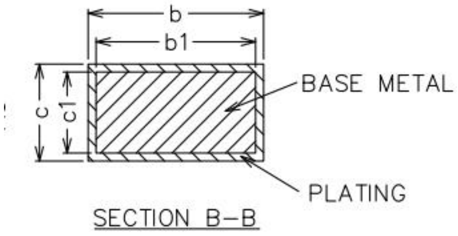
Common Dimensions (Units of measure = Millimeter)			
Symbol	Min	Nom	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.20 REF		
b	0.20	0.25	0.30
b1	0.20 REF		
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.50	1.60	1.70
E2	2.40	2.50	2.60
e	0.40	0.50	0.60
K	0.20	-	-
L	0.30	0.40	0.50
R	0.13	-	-

11.3. EP-SOIC8



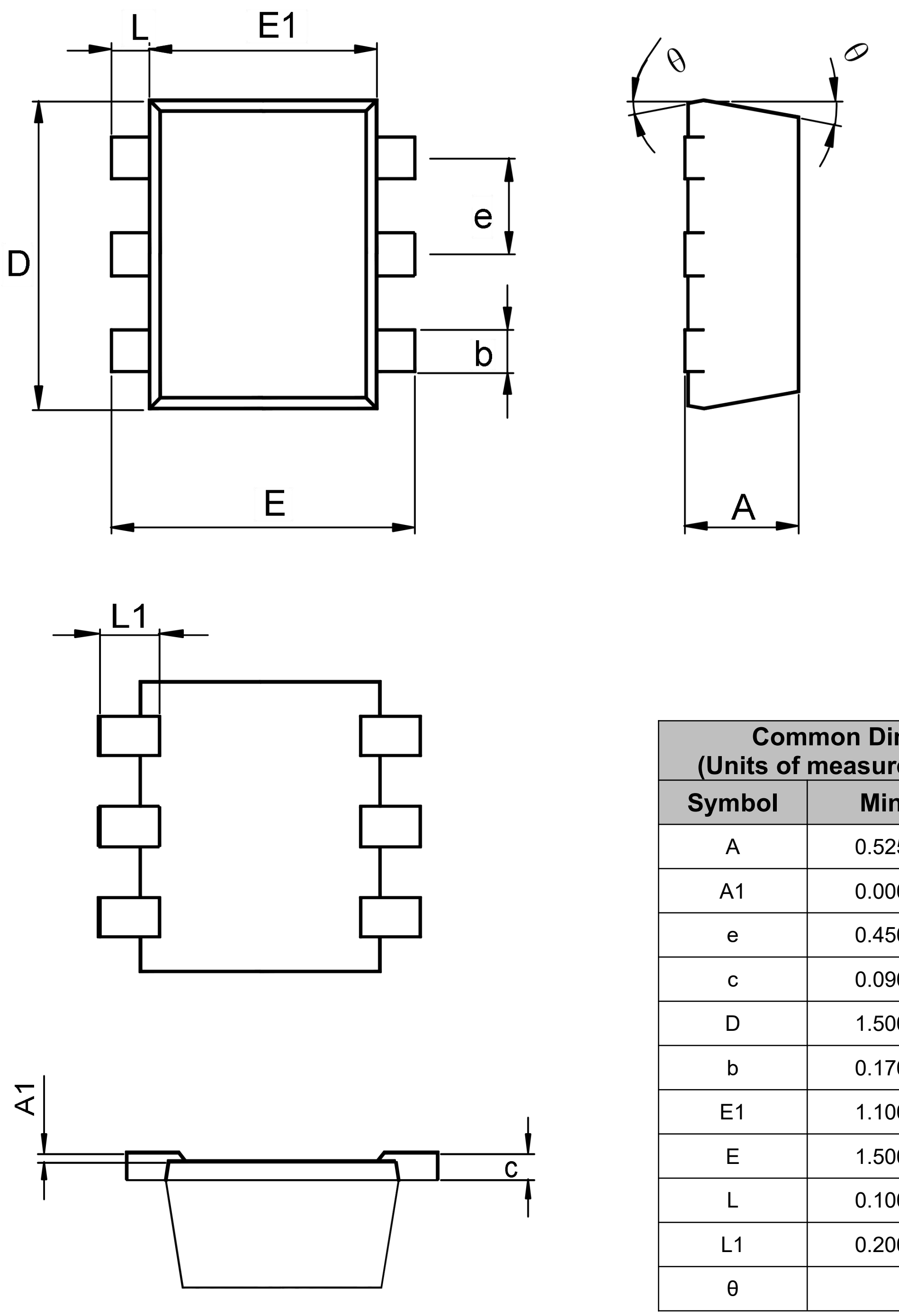






Common Dimensions (Units of measure = Millimeter)			
Symbol	Min	Nom	Max
A	1.35	1.45	1.65
A1	0	-	0.15
A2	1.35	1.40	1.50
A3	0.50	0.60	0.70
b	0.38	-	0.47
b1	0.37	0.40	0.43
c	0.17	-	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
D1	3.02	3.17	3.32
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
E2	2.13	2.28	2.43
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25 BSC		
R	0.07	-	-
R1	0.07	-	-
h	0.30	0.40	0.50
θ	0°	-	8°
θ1	15°	17°	19°
θ2	11°	13°	15°

11.4. SOT563



Common Dimensions (Units of measure = Millimeter)		
Symbol	**Min**	**Max**
A	0.525	0.600
A1	0.000	0.050
e	0.450	0.550
c	0.090	0.180
D	1.500	1.700
b	0.170	0.270
E1	1.100	1.300
E	1.500	1.700
L	0.100	0.300
L1	0.200	0.400
θ	9° REF	

Disclaimer

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