Rev 1.3

DIO6921
High-Efficiency 2 A, 28 V Input Synchronous Step Down Converter

Features

- Low $R_{DS(ON)}$ or internal switches (top/bottom) 120 mΩ/75 mΩ, 2.0 A
- 4.5 ~ 28 V input voltage range
- High-efficiency, synchronous-mode
- Internal soft-start limits the inrush current
- Over current protection
- Thermal shutdown
- Green package:
  TSOT23-6 is pin compatible

Applications

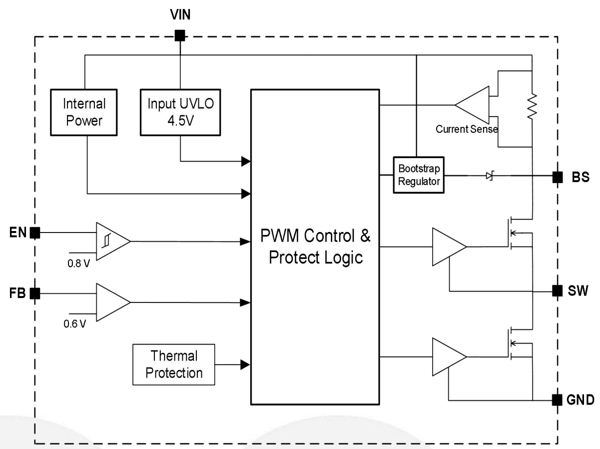
- Portable navigation devices
- Set top boxes
- Portable TVs
- LCD TVs

Descriptions

The DIO6921 is a high-efficiency, high-frequency synchronous step-down DC-DC regulator IC capable of delivering up to 2 A output currents. The DIO6921 operates over a wide input voltage range from 4.5 V to 28 V and integrates the main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The DIO6921 adopts the COT architecture to achieve fast transient responses for high step-down applications and high efficiency at light loads. In addition, it operates at a pseudo-constant frequency of 700 kHz under heavy load conditions to minimize the size of the inductor and capacitor.

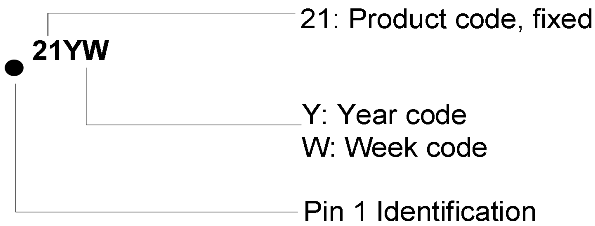
Function Block



Ordering Information

Ordering Part NO.	Top Marking	MSL	RoHS	T_A	Package	
DIO6921TST6	21YW	3	Green	-40 to 85°C	TSOT23-6	Tape & Reel, 3000

Marking Definition



Pin Assignments

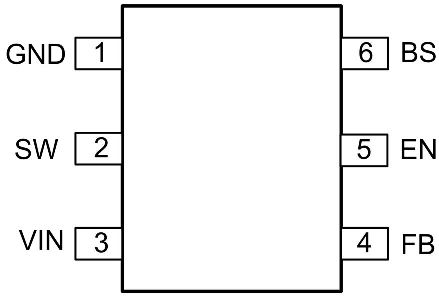


Figure 1. TSOT23-6 (Top view)

Pin Definitions

Pin No.	Pin Name	Description
1	GND	Power ground.
2	SW	Inductor pin. Connect this pin to the switching node of inductor.
3	VIN	Power input.
4	FB	Output feedback pin. Connect this pin to the center point of the output resistor divider to program the output voltage: $V_{OUT} = 0.6 \times (1 + R1/R2)$. Add optional C2 (10 pF~47 pF) to speed up the transient response.
5	EN	Enable control. Pull high to turn on. Do not float.
6	BS	Bootstrap. Connect a capacitor and a resistor between SW and BS pins to form a floating supply across the high-side switch driver. Recommend to use 0.1 µF BS capacitor.

Absolute Maximum Ratings

Stresses beyond those listed under the Absolute Maximum Rating table may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. DIOO does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter		Rating	Unit
V_{IN}	Supply voltage (V+ – V-)		-0.3 to 36	V
V_{EN}	EN voltage		-0.3 to V_{IN} + 0.3	V
V_{FB}	FB voltage		-0.3 to 6	V
V_{BS}	BS voltage		SW + 6	V
V_{SW}	SW voltage	< 20 ns	-5 to 32	V
		> 20 ns	-0.3 to 30	
θ_{JA}	Junction-to-ambient thermal resistance		89	°C/W
θ_{JC}	Junction-to-case thermal resistance		44.5	
T_{STG}	Storage temperature range		-65 to 150	°C
T_J	Junction temperature range		150	°C
T_L	Lead temperature range		260	°C
ESD	Human-body mode (HBM)		±3500	V

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications.

Symbol	Parameter	Rating	Unit
V_{IN}	Supply voltage	4.5 to 28	V
T_J	Junction temperature range	-40 to 125	°C
T_A	Ambient temperature range	-40 to 85	°C

Electrical Characteristics

V_{IN} = 12 V, V_{OUT} = 1.2 V, L = 2.2 μH, C_{OUT} = 22 μF, T_A = 25°C, I_{OUT} = 1 A unless otherwise specified.

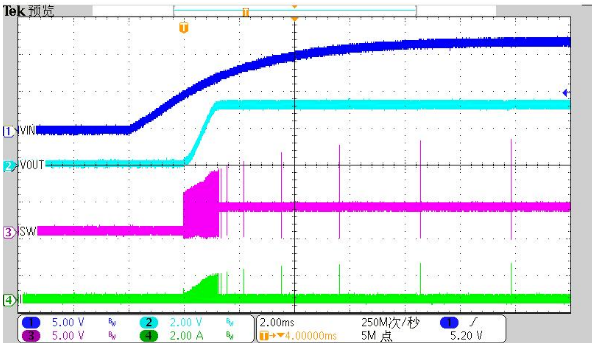
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage range		4.5		28	V
I_Q	Quiescent current	I_{OUT} = 0, V_{FB} = V_{REF} × 105%		140		μA
I_{SHDN}	Shutdown current	EN = 0		5	10	μA
V_{REF}	Feedback reference voltage		0.588	0.6	0.612	V
I_{FB}	FB input current	V_{FB} = V_{IN}	-50		50	nA
$R_{DS(ON)}$(1)	Top FET R_{ON}			120		mΩ
$R_{DS(ON)}$(1)	Bottom FET R_{ON}			75		mΩ
I_{LIM}(1)	Bottom FET valley current limit		2			A
V_{ENH}	EN rising threshold	T_A = 25°C	0.75	0.8	0.85	V
		T_A = -40 ~ 125°C	0.69	0.8	0.91	V
V_{ENL_HYS}	Hysteresis		60	80	100	mV
V_{UVLO}	Input UVLO threshold				4.5	V
V_{UVLO_HYS}	UVLO hysteresis			500		mV
f_{SW}	Switching frequency			700		kHz
T_{ON}	ON time	V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 1 A		145		ns
	Min ON time(1)			50		ns
	Min OFF time(1)			100		ns
t_{SS}(1)	Soft -start time			2		ms
T_{SD}(1)	Thermal shutdown temperature			150		°C
T_{HYS}(1)	Thermal shutdown hysteresis			15		°C

Note:

(1) Guaranteed by design.

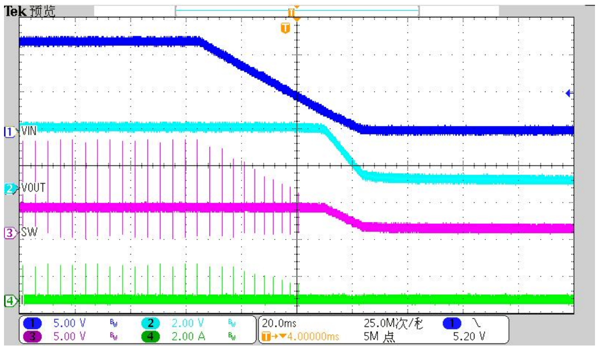
(2) Specifications subject to change without notice.

Typical Operation Performances



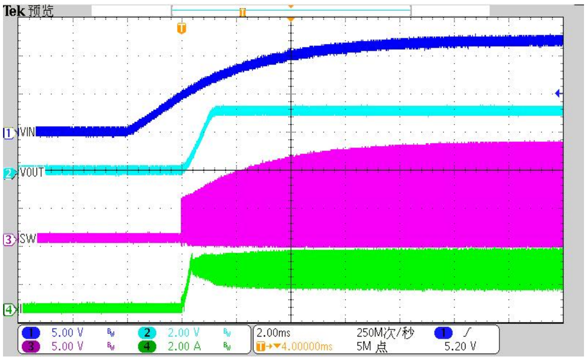
V_{IN} = 12 V, V_{OUT} = 3.3 V, No Load

Start up from V_{IN}



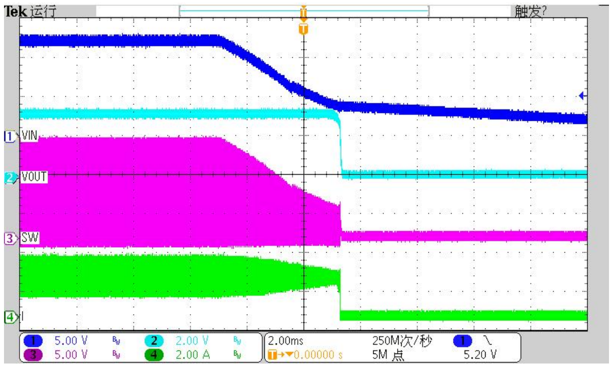
V_{IN} = 12 V, V_{OUT} = 3.3 V, No Load

Shut down from V_{IN}



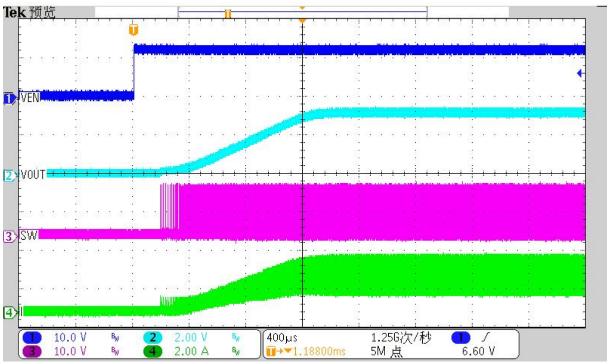
V_{IN} = 12 V, V_{OUT} = 3.3 V, Load = 2 A

Start up from V_{IN}



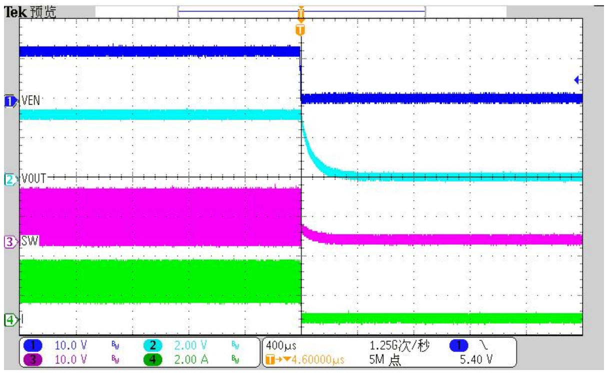
V_{IN} = 12 V, V_{OUT} = 3.3 V, Load = 2 A

Shut down from V_{IN}



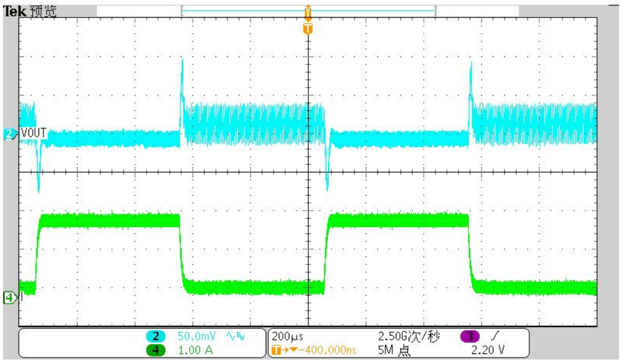
V_{IN} =12 V, V_{OUT} = 3.3 V, Load = 1.65 Ω

Start up from Enable



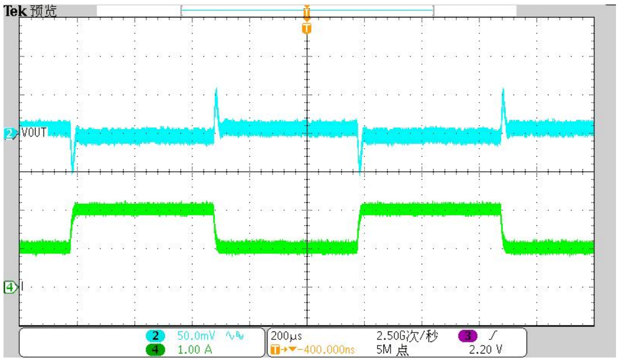
V_{IN} = 12 V, V_{OUT} = 3.3 V, Load = 1.65 Ω

Shut down from Enable



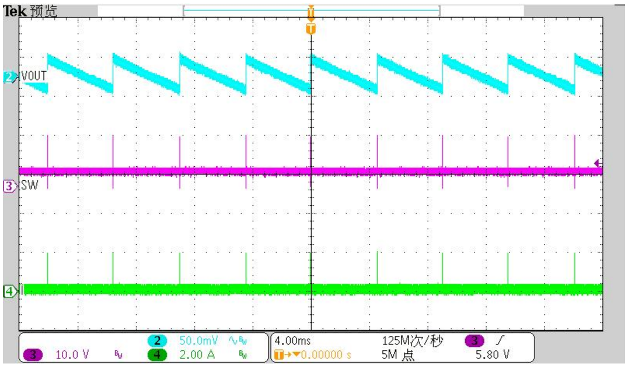
V_{IN} = 12 V, V_{OUT} = 3.3 V, Load = 0.2 ~ 2 A

Load transient



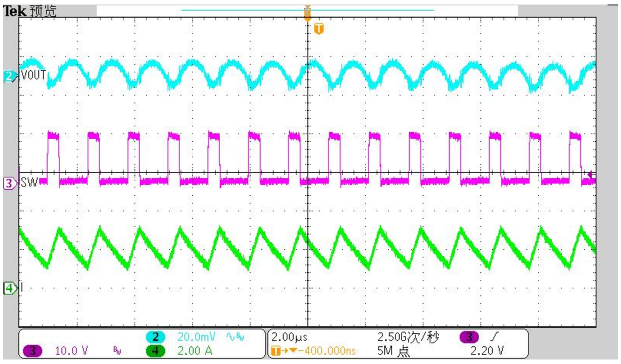
V_{IN} = 12 V, V_{OUT} = 3.3 V, Load = 1 ~ 2 A

Load transient



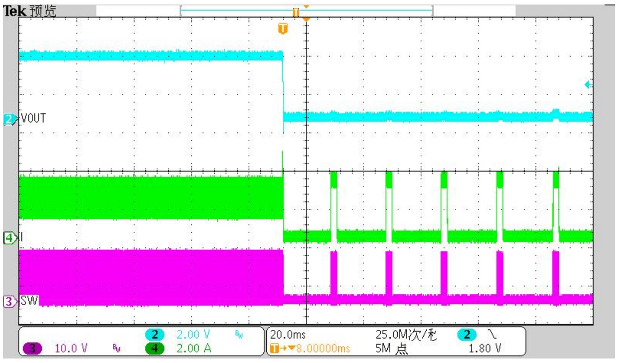
V_{IN} = 12 V, V_{OUT} = 3.3 V, Load = 0 A

Ripple



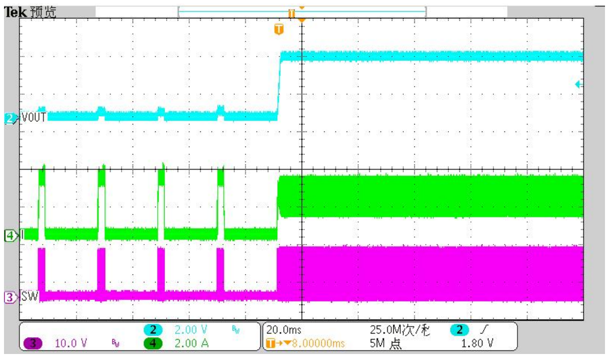
V_{IN} = 12 V, V_{OUT} =3.3 V, Load = 2 A

Ripple



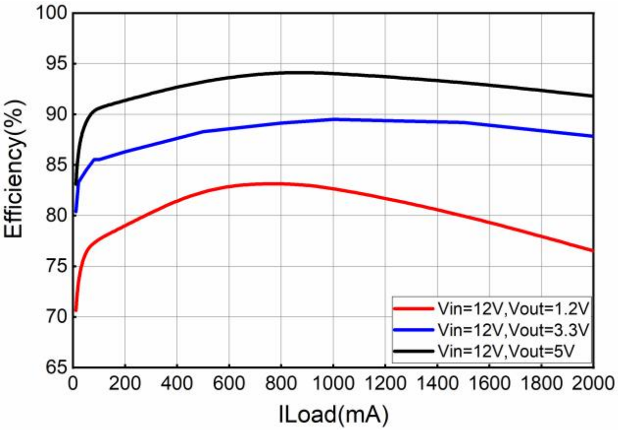
V_{IN} = 12 V, V_{OUT} = 3.3 V, Load = 2 A

Short circuit protection

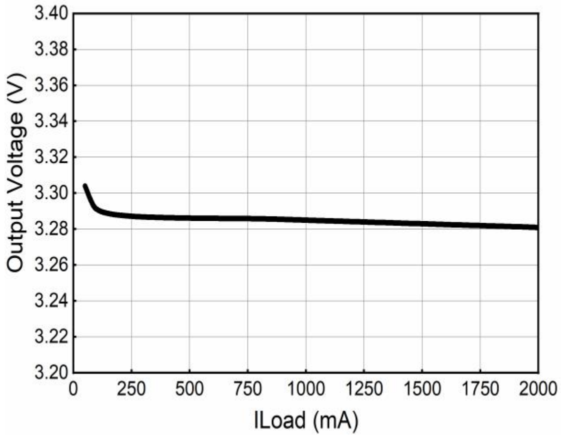


V_{IN} = 12 V, V_{OUT} = 3.3 V, Load = 2 A

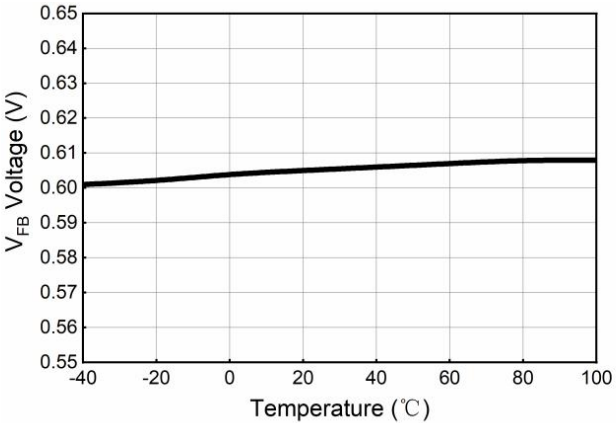
Short circuit recovery



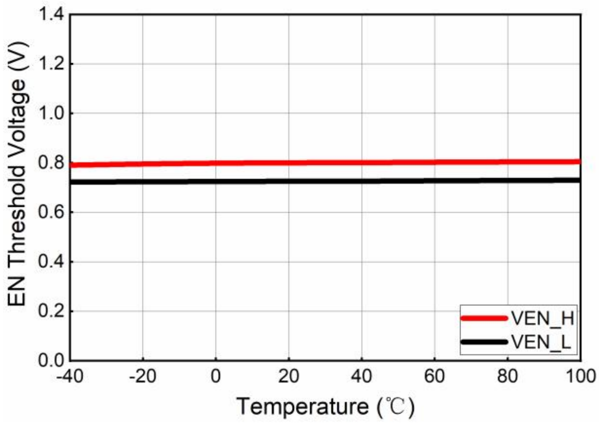
Efficiency vs. Output current



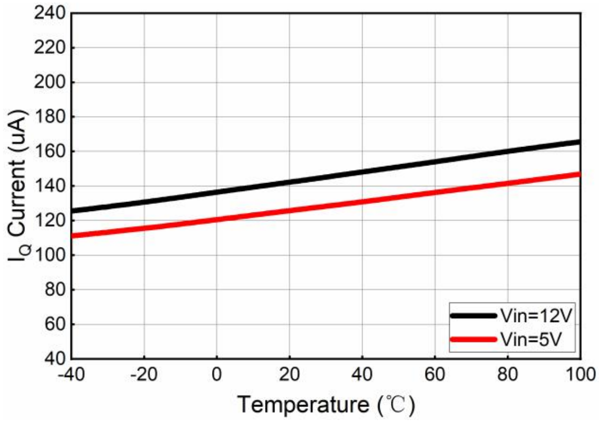
Output voltage vs. Output current



V_{FB} vs. Temperature

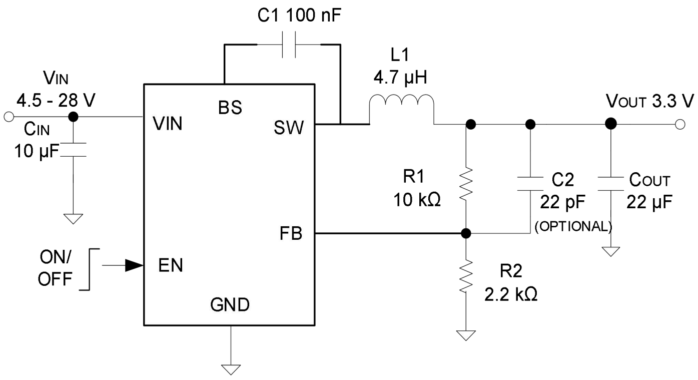


EN threshold vs. Temperature



I_Q vs. Temperature

Typical Application



Operation

The DIO6921 is a synchronous buck regulator IC that integrates the COT control, top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra-low $R_{DS(ON)}$ power switches and proprietary COT control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size, thus achieving the minimum solution footprint.

The DIO6921 provides protection functions such as cycle-by-cycle current limiting and thermal shutdown protection. The DIO6921 will sense the output voltage conditions for fault protection.

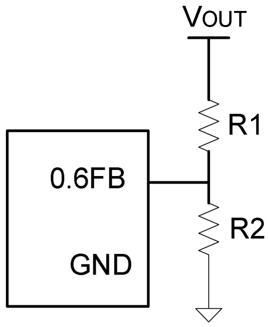
Applications Information

Because of the high integration in the DIO6921 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L1, and feedback resistors (R1 and R2) need to be selected for the targeted application specifications.

Feedback resistor dividers R1 and R2

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, choose large resistance values for both R1 and R2. A value of between 10 kΩ and 1 MΩ is highly recommended for both resistors. If V_{OUT} is 3.3 V, R1=100 kΩ is chosen, then R2 can be calculated to be 22 kΩ.

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} \times R_1 \quad (1)$$



Input capacitor C_{IN}

This ripple current through the input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1-D)} \quad (2)$$

To minimize the potential noise problem, place a typical X5R or better-grade ceramic capacitor close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. In this case, a 10 μF low equivalent series resistance (ESR) ceramic capacitor is recommended.

Output capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady-state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X5R or better grade ceramic capacitor greater than 22 μF capacitance.

Output inductor L1

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%} \quad (3)$$

where fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The DIO6921 regulator IC is quite tolerant of different ripple current amplitudes. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

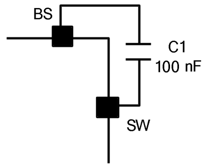
2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \cdot f_{SW} \cdot L} \quad (4)$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR < 50 mΩ to achieve good overall efficiency.

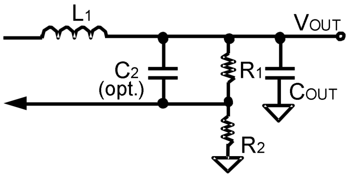
External bootstrap cap

This capacitor provides the gate driver voltage for internal high-side MOSFET. A 100 nF low ESR ceramic capacitor connected between the BS pin and SW pin is recommended.



Load transient considerations

The DIO6921 regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 22 pF ceramic cap in parallel with R1 may further speed up the load transient responses and is thus recommended for applications with large load transient.

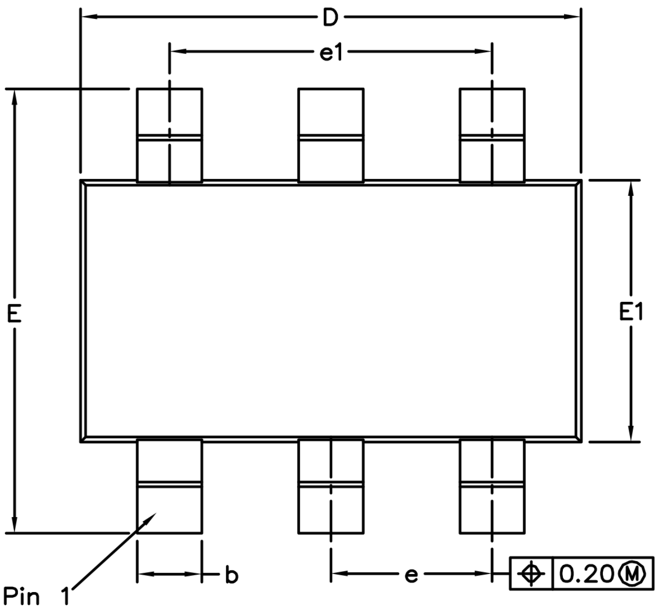


Layout design

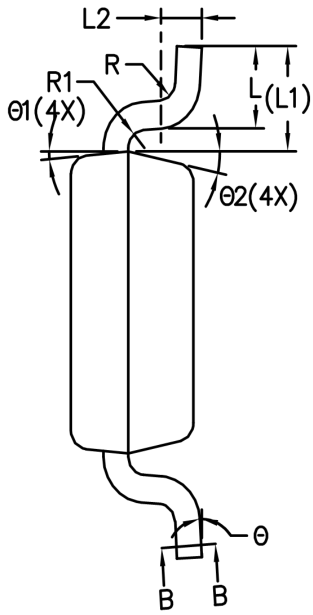
The layout design of the DIO6921 regulator is relatively simple. For the best efficiency and minimum noise problems, place the following components close to the IC: C_{IN}, L1, R1, and R2.

1) It is desirable to maximize the PCB copper area connected to the GND pin to achieve the best thermal and noise performance. If the board space allows, a ground plane is highly desirable.
2) C_{IN} must be close to IN and GND pins. The loop area formed by C_{IN} and GND must be minimized.
3) The PCB copper area associated with the SW pin must be minimized to avoid the potential noise problem.
4) The components R1 and R2, and the trace connecting to the FB pin must NOT be adjacent to the SW net on the PCB layout to avoid the noise problem.
5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull-down 1 MΩ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

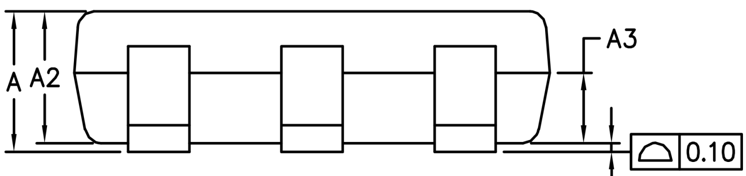
Physical Dimensions: TSOT23-6



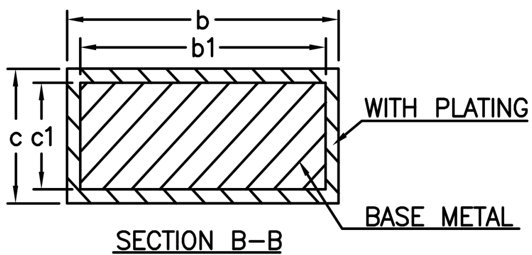
TOP VIEW



SIDE VIEW



SIDE VIEW



SECTION B–B

Common Dimensions (Units of measure = millimeter)			
Symbol	Min	Nom	Max
A	-	-	0.90
A1	0	-	0.15
A2	0.65	0.75	0.85
A3	0.35	0.40	0.45
b	0.36	-	0.50
b1	0.36	0.38	0.45
c	0.14	-	0.20
c1	0.14	0.15	0.16
D	2.85	2.95	3.05
E	2.60	2.80	3.00
E1	1.60	1.65	1.70
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
L	0.30	0.45	0.60
L1	0.575 REF		
L2	0.25 BSC		
R	-	-	0.25
R1	-	-	0.25
Θ	0°	-	8°
Θ1	3°	5°	7°
Θ2	10°	12°	14°

CONTACT US

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