

DI3PCIE350

PCI Express 3.0, 11 Gbps, 2:1 Mux / DeMux Switch

Description

The DI3PCIE350 is a high-performance, two pairs 2:1 data switch for PCIE 3.0, 8 Gbps data. The DI3PCIE350 focuses on the server market. It can minimize the switch channel-to-channel skew and channel-to-channel crosstalk of the super speed signals.

The switch supports bidirectional operation, making it suitable for PCIE 3.0.

Overall, the DI3PCIE350 is a robust and versatile data switch for high-performance PCIE 3.0 applications, offering exceptional data transfer speeds, low power consumption, and reliable protection against ESD.

Features

- Wide V_{DD} input voltage range: 1.5 V to 5.0 V
- Up to 11 Gbps for application PCIE 3.0
- Bidirectional operation
- Bandwidth: 11 GHz (typ)
- -0.9 dB typical insertion loss at 2.5 GHz
- Low active power of 21 μ A (typ) at $V_{DD} = 5$ V
- Low shutdown power of < 0.5 μ A (max)
- Low crosstalk: -38 dB at 2.5 GHz
- Low off isolation: -25 dB at 2.5 GHz
- Operation temperature range: -40°C to 85 °C
- ± 4 kV HBM ESD protection
- Packages: QFN2.5*4.5-20 and QFN2*2-18

Applications

- Servers
- Tablets
- Notebooks

■ Ordering Information

Ordering Part No.	Top Marking	MSL	RoHS	T _A	Package	
DI3PCIE350CN18	D3EV	3	Green	-40 to 85°C	QFN2*2-18	Tape & Reel, 3000
DI3PCIE350BEN20	D3EB	3	Green	-40 to 85°C	QFN2.5*4.5-20	Tape & Reel, 5000

If you encounter any issue in the process of using the device, please contact our customer service at marketing@dioo.com or phone us at (+86)-21-62116882. If you have any improvement suggestions regarding the datasheet, we encourage you to contact our technical writing team at docs@dioo.com. Your feedback is invaluable for us to provide a better user experience.

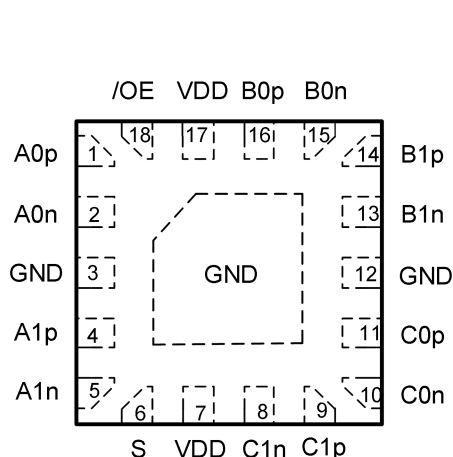
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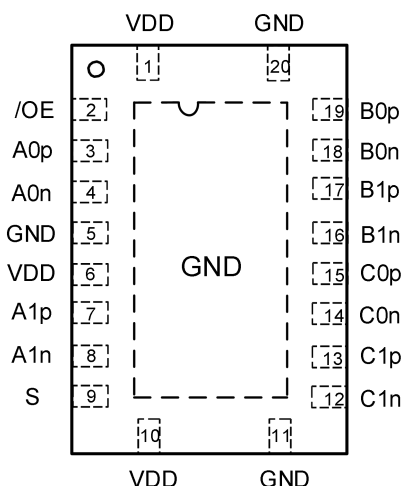
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1. Pin Assignment and Functions



DI3PCIE350CN18

Figure 1. QFN2*2-18 (Top view)



DI3PCIE350BEN20

Figure 2. QFN2.5*4.5-20 (Top view)

Pin Name	I/O	Description
A0n	I/O	Port A, channel 0, high-speed negative signal.
A1p	I/O	Port A, channel 1, high-speed positive signal.
A1n	I/O	Port A, channel 1, high-speed negative signal.
S	I	Switch selection (L: port A to port B; H: port A to port C).
C1n	I/O	Port C, channel 1, high-speed negative signal (connector side).
C1p	I/O	Port C, channel 1, high-speed positive signal (connector side).
C0n	I/O	Port C, channel 0, high-speed negative signal (connector side).
C0p	I/O	Port C, channel 0, high-speed positive signal (connector side).
B1n	I/O	Port B, channel 1, high-speed negative signal (connector side).
B1p	I/O	Port B, channel 1, high-speed positive signal (connector side).
B0n	I/O	Port B, channel 0, high-speed negative signal (connector side).
B0p	I/O	Port B, channel 0, high-speed positive signal (connector side).
A0p	I/O	Port A, channel 0, high-speed positive signal.
/OE	I	Output enable (0 = switches enabled, 1 = switches disabled).
VDD	VDD	Device power.
GND	GND	Ground.

2. Absolute Maximum Ratings

Exceeding the maximum ratings listed under Absolute Maximum Ratings when designing is likely to damage the device permanently. Do not design to the maximum limits because long-time exposure to them might impact the device's reliability. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Ratings	Unit
V_{DD}	Supply voltage	-0.5 to 6.0	V
V_{CNTRL}	DC input voltage (S, /OE) ⁽¹⁾	-0.5 to V_{DD}	V
V_{SW}	DC switch I/O voltage ^(1,2)	-0.3 to 2.1	V
I_{IK}	DC input diode current	-50	mA
I_{SW}	DC switch current	25	mA
T_{STG}	Storage temperature	-65 to 150	°C

Note:

(1) The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

(2) V_{SW} refers to analog data switch paths.

3. Recommended Operating Condition

Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Ratings	Unit
V_{DD}	Supply voltage	1.5 to 5.0	V
V_{CNTRL}	Control input voltage (S, /OE) ⁽¹⁾	0 to 5.0	V
V_{SW}	Switch I/O voltage (all switch paths)	0 to 2.0	V
T_A	Operating temperature range	-40 to 85	°C

Note:

(1) The control inputs must be held HIGH or LOW; Do not leave them floated.

4. ESD Ratings

When a statically-charged person or object touches an electrostatic discharge sensitive device, the electrostatic charge might be drained through sensitive circuitry in the device. If the electrostatic discharge possesses sufficient energy, damage might occur to the device due to localized overheating.

Model	Condition	Value	Unit
Human-body model	JEDEC EIA/JESD22-A114F	±4000	V

5. Thermal Considerations

The thermal resistance determines the heat insulation property of a material. The higher the thermal resistance is, the lower the heat loss. Accumulation of heat energy degrades the performance of semiconductor components.

Symbol	Metric		Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	QFN2*2-18	120	°C/W
		QFN2.5*4.5-20	46.6	°C/W

6. Electrical Characteristics

The values are obtained under these conditions unless otherwise specified: typical values at $V_{DD} = 3.6\text{ V}$, $T_A = 25^\circ\text{C}$.

Symbol	Parameter	Conditions	V_{DD} (V)	Min	Typ	Max	Unit
DC and transient characteristics							
V_{IH}	Control input voltage high	S, /OE	1.5	1.3			V
		S, /OE	3.6	1.4			
		S, /OE	5.0	1.5			
V_{IL}	Control input voltage low	S, /OE	1.5			0.4	V
		S, /OE	3.6			0.4	
		S, /OE	5.0			0.4	
I_{IN}	Control input leakage	$V_{CNTRL} = 0$ to V_{DD}	5.0	-500		500	nA
I_{OZ}	Off-state leakage for open data paths	$V_{SW} = 0$ to 2 V	5.0	-500		500	nA
I_{CL}	On-state leakage for closed data paths ⁽¹⁾	$V_{SW} = 0$ to 2 V	5.0	-500		500	nA
I_{OFF}	Power-off leakage current (all I/O ports)	$V_{SW} = 0$ to 2 V	0	-500		500	nA
R_{ON}	Switch on resistance	$V_{SW} = 0$ to 2 V , $I_{ON} = -8\text{ mA}$	1.5		6	8	Ω
ΔR_{ON}	Difference in R_{ON} between positive-negative	$V_{SW} = 0$ to 2 V , $I_{ON} = -8\text{ mA}$	1.5		0.1		Ω
R_{ONF}	Flatness for R_{ON}	$V_{SW} = 0$ to 2 V , $I_{ON} = -8\text{ mA}$	1.5			0.5	Ω
I_{CC}	Quiescent supply current	$V_{IOE} = 0$, $V_{SEL} = 0$ or V_{DD} , $I_{OUT} = 0$	5.0		21	30	μA
I_{CCZ}	Quiescent supply current (high impedance)	$V_{SEL} = X$, $V_{IOE} = V_{DD}$, $I_{OUT} = 0$	5.0			0.5	μA
I_{CCT}	Increase in quiescent supply current per V_{CNTRL}	V_{SEL} or $V_{IOE} = 1.5\text{ V}$	5.0		7	15	μA

AC electrical characteristics							
t_{ON}	Turn-on time, S to output	$R_L = 50 \Omega$, $V_{SW} = 0.6 V$	1.5 to 5.0		420		ns
t_{OFF}	Turn-off time, S to output	$R_L = 50 \Omega$, $V_{SW} = 2 V$	1.5 to 5.0		100		ns
$t_{ZHM,ZL}$	Enable time, /OE to output	$R_L = 50 \Omega$, $V_{SW} = 0.6 V$	1.5 to 5.0		120		μs
$t_{LZM,HZ}$	Disable time, /OE to output	$R_L = 50 \Omega$, $V_{SW} = 0.6 V$	1.5 to 5.0		110		ns
t_{PD}	Propagation delay ⁽²⁾	$R_L = 50 \Omega$	1.5 to 5.0		60		ps
t_{BBM}	Break-before-make	$R_L = 50 \Omega$, $V_{SW} = 0.6 V$	1.5 to 5.0	120			ns
DOIRR	Differential off isolation	$V_{SW} = 0 dBm$, $R_L = 50 \Omega$, $f = 2.5 GHz$	3.6		-25		dB
		$V_{SW} = 0 dBm$, $R_L = 50 \Omega$, $f = 5.0 GHz$			-22		dB
SDDNEXT	Differential channel crosstalk	$V_{SW} = 0 dBm$, $R_L = 50 \Omega$, $f = 2.5 GHz$	3.6		-38		dB
		$V_{SW} = 0 dBm$, $R_L = 50 \Omega$, $f = 5.0 GHz$			-36		dB
DIL	Differential insertion loss (all data paths)	$V_{IN} = 0 dBm$, $f = 2.5 GHz$, $R_L = 50 \Omega$, $C_L = 0 pF$	3.6		-0.9		dB
		$V_{IN} = 0 dBm$, $f = 5.0 GHz$, $R_L = 50 \Omega$, $C_L = 0 pF$			-1.4		
BW	Differential -3 dB bandwidth	$V_{IN} = 0 dBm$, $R_L = 50 \Omega$, $C_L = 0 pF$ (both data paths)	3.6		11		GHz
$t_{sk(P)}$	Skew of opposite transitions of the same output ⁽²⁾	$R_{PULL_UP} = 50 \Omega$ to V_{DD} , $C_L = 0 pF$	3.6		6		ps
C_{IN}	Control pin input capacitance ⁽²⁾	$V_{DD} = 0 V$, $f = 1 MHz$			2.7		pF
C_{ON}	On capacitance ⁽²⁾	$V_{DD} = 3.3 V$, $f = 2.5 GHz$			0.45		pF
C_{OFF}	Off capacitance ⁽²⁾	$V_{DD} = 3.3 V$, $f = 2.5 GHz$			0.36		pF

Note:

- (1) For test of "DC and transient characteristics", the data switch is closed with the respective switch pin floating.
- (2) Guaranteed by design.
- (3) Specifications subject to change without notice.

7. Typical Characteristics

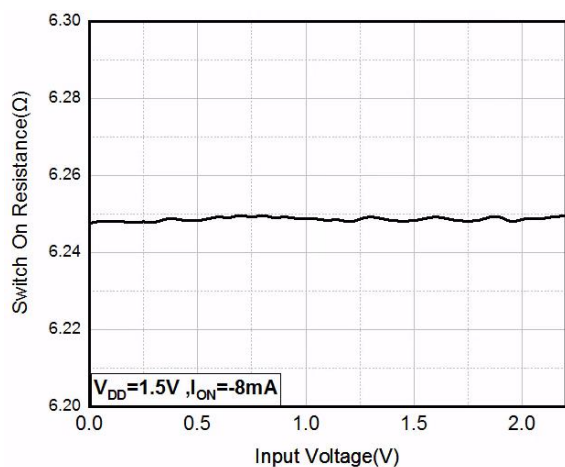


Figure 3. R_{ON} vs. V_{IN}

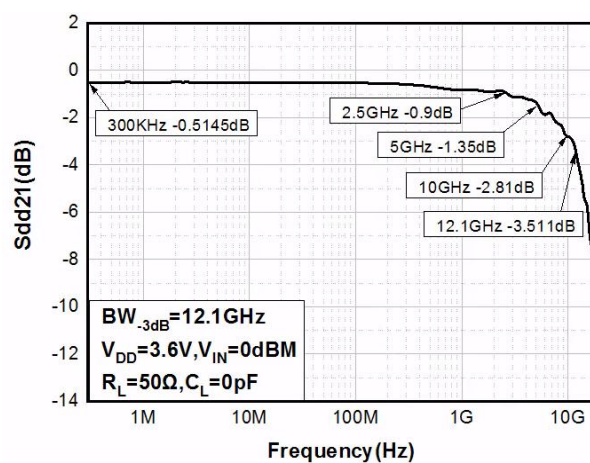


Figure 4. Differential -3 dB bandwidth

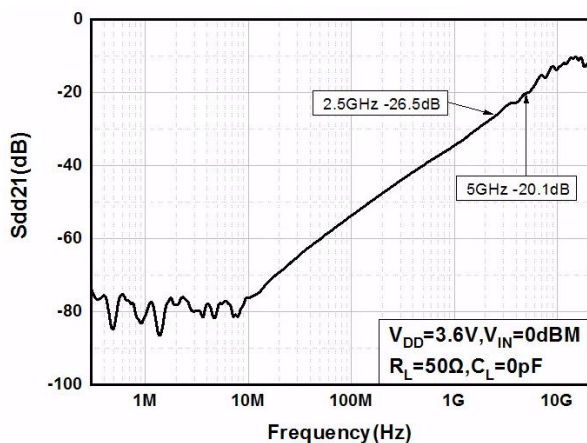


Figure 5. Differential off isolation

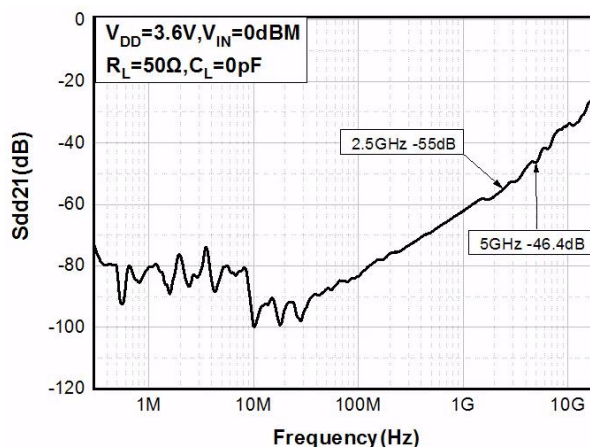
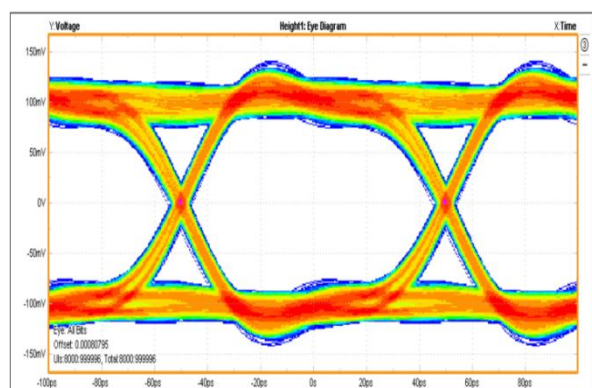
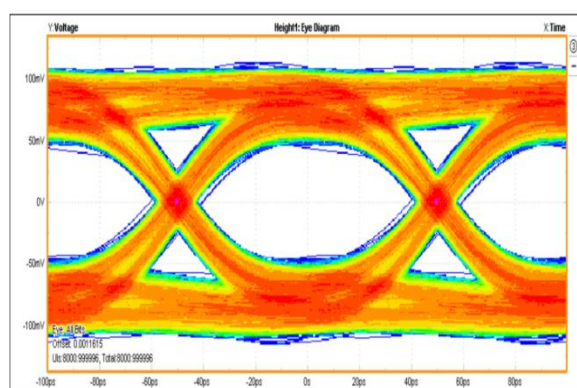


Figure 6. Differential channel crosstalk



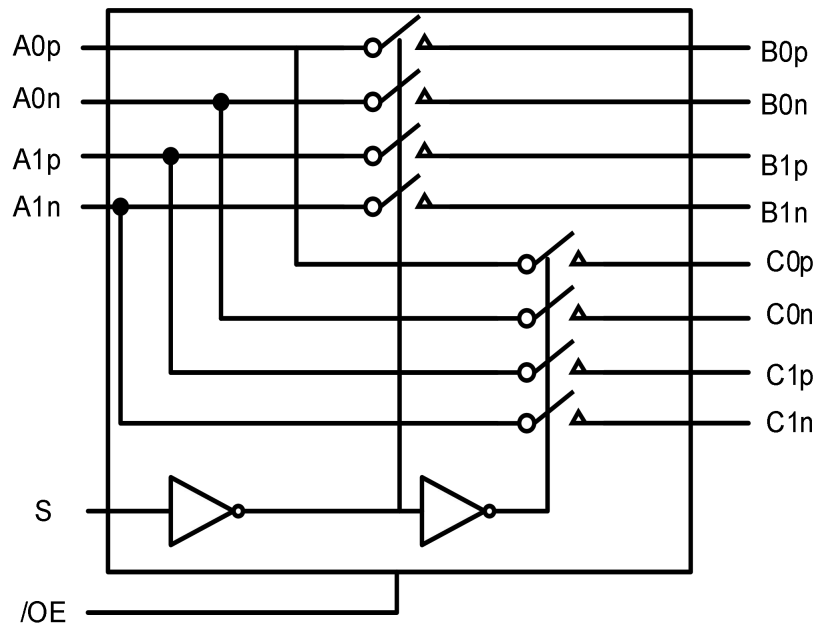
Before Switch



After Switch

Figure 7. Eye opening at 10 Gb/s using PRBS15 pattern

8. Block Diagram



9. Application Information

Important notice: Validation and testing are the most reliable ways to confirm system functionality. The application information is not part of the specification and is for reference purpose only.

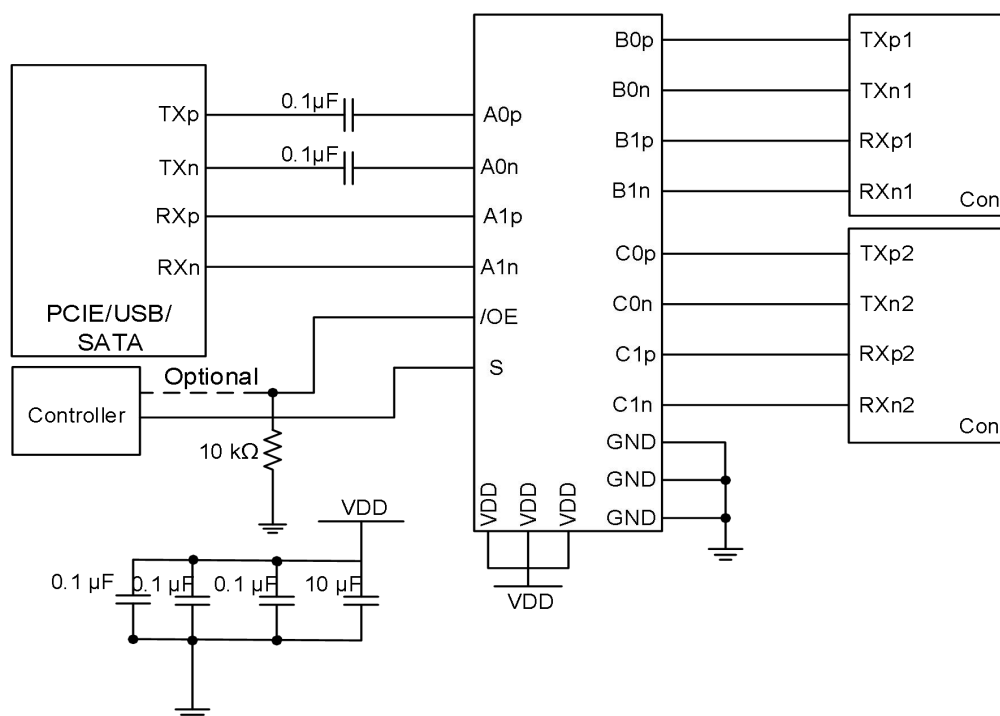


Figure 8. PCIE motherboard

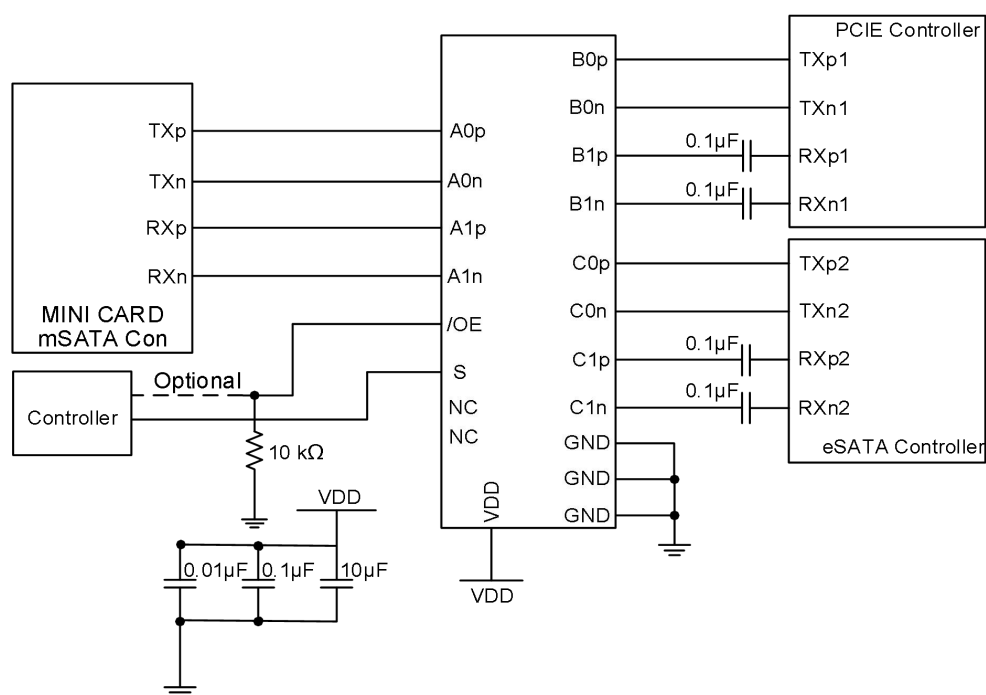
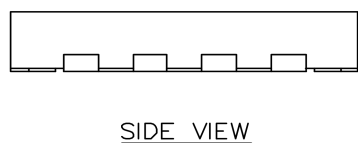
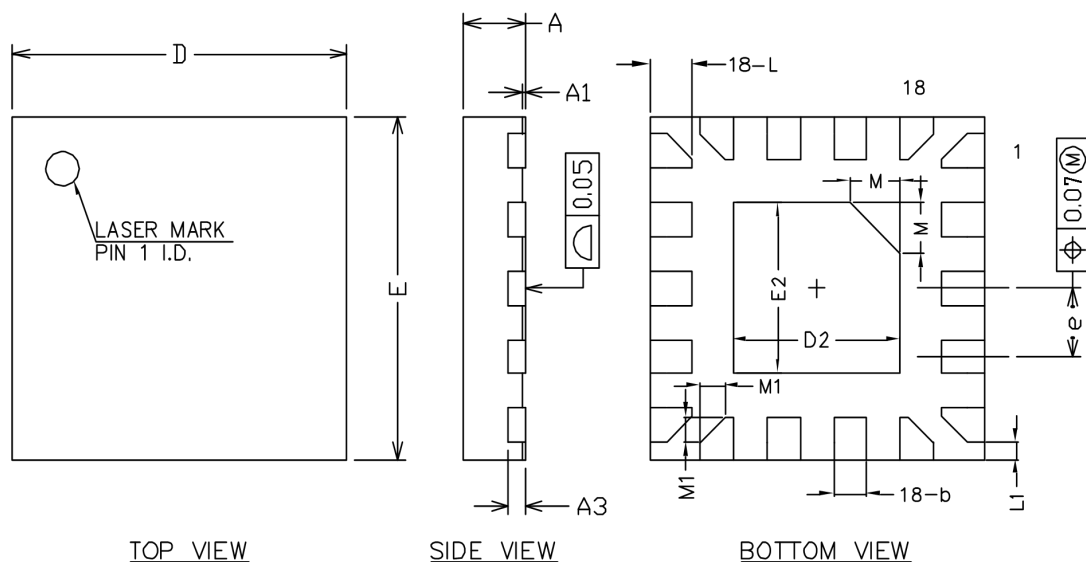


Figure 9. PCIE and eSATA combo

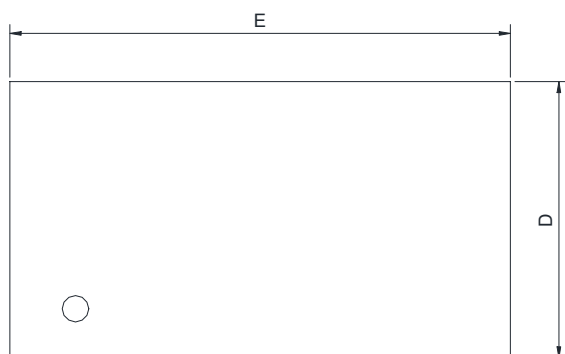
10. Physical Dimensions:

10.1. QFN2*2-18

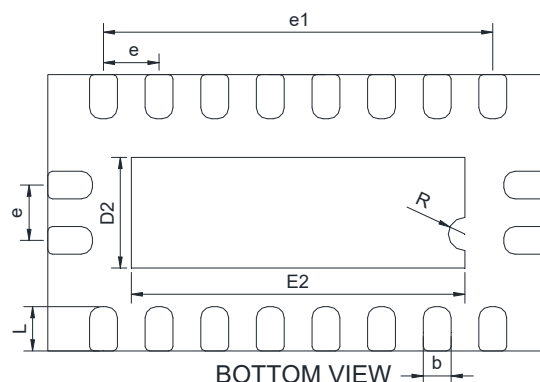


Common Dimensions (Units of measure = Millimeter)			
Symbol	Min	Typ	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	0.100 REF		
b	0.15	0.20	0.25
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.90	1.00	1.10
E2	0.90	1.00	1.10
e	0.30	0.40	0.50
L	0.20	0.25	0.30
L1	0.05	0.10	0.15
M	0.30 REF		
M1	0.15 REF		

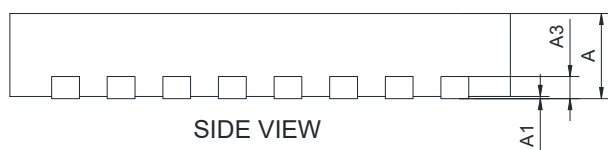
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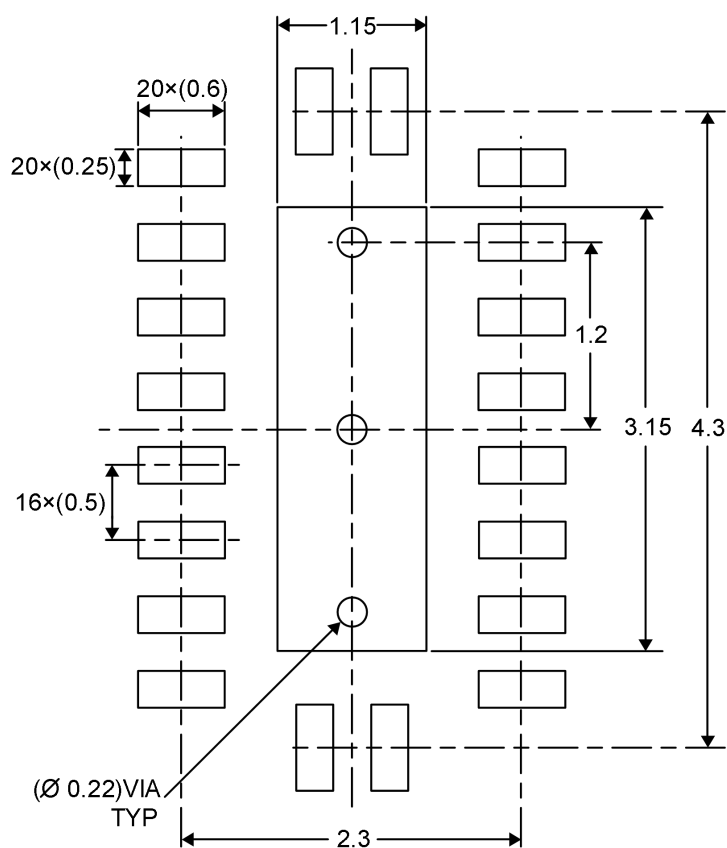
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

Common Dimensions (Units of measure = Millimeter)			
Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.20	0.25	0.30
D	2.40	2.50	2.60
E	4.40	4.50	4.60
D2	0.85	1.00	1.15
E2	2.85	3.00	3.15
e	0.45	0.50	0.55
e1	3.40	3.50	3.60
L	0.30	0.40	0.50
R	0.15 REF		

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