DIO6157

High-Efficiency, 4 A Output Synchronous Step-Down Converter

Features

- Low $R_{DS(ON)}$ for internal switches (25 mΩ)
- 2.5 V to 5.5 V input voltage range
- Adjustable output voltage:
  0.6 V to 5 V
- More than 4 A output current capability
- Low quiescent current: 10 μA
- 2 MHz switching frequency minimizes the external components
- Operation mode: FPWM or auto mode
- High efficiency at light load
- 100% duty cycle for lowest dropout
- Output discharge function
- Protection:
  - Thermal shutdown protection
  - Overcurrent protection
- Package: 1.5 mm x 1.5 mm DFN-6

Applications

- IP network cameras
- Portable electronics
- Solid state drives
- Industrial PCs
- Multifunctional printers

Descriptions

The DIO6157 is a high-efficiency, high-frequency synchronous step-down DC-DC regulator IC capable of delivering more than 4 A output currents.

The DIO6157 has a selection function, which can switch between forced pulse width modulation (FPWM) and auto mode. When the SEL pin is driven HIGH, the DIO6157 enters the forced pulse width modulation mode. It enters the auto mode if the SEL pin is LOW.

If the DIO6157 is selected to work under FPWM mode, the device works with ultra-low output ripple. Under auto mode, the DIO6157 works in PWM mode under medium to heavy load. In such conditions, the DIO6157 functions with a 2 MHz switching frequency to minimize the size of the inductor and output capacitor. If the load drops to meet the light load condition, the DIO6157 automatically enters PSM (Power Save Mode) for high efficiency.

The DIO6157 has a fast transient response feature. The device operates over a wide input ranging from 2.5 V to 5.5 V with very low $R_{DS(ON)}$ to minimize the conduction loss. The DIO6157 is capable of delivering output down to 0.6 V with the feedback voltage of ±6 mV accuracy over -20°C to 85°C junction temperature.

Ordering Information

Part Number	Top Marking	RoHS	T_A	Package	
DIO6157CL6	5GYW	Green	-40 to 85°C	DFN1.5*1.5-6	Tape & Reel, 3000

Pin Assignment

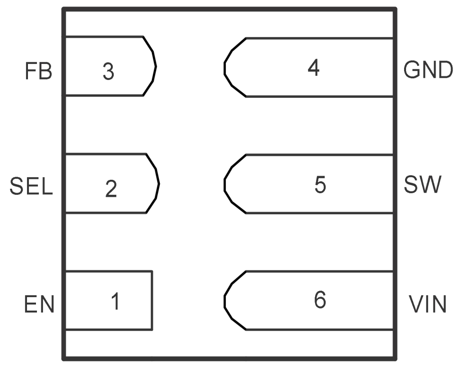


*Figure 1. DFN 1.5*1.5-6 (Bottom view)*

Pin Descriptions

Pin	Name	Description
1	EN	Enable control. Pull high to turn on. Do not leave it floating. Maximum available pull-down resistor: 1 MΩ.
2	SEL	Select pin. It can be selected between FPWM and Auto mode, but can not be floating. Maximum available pull-down resistor: 1 MΩ. SEL = 0 means Auto mode; SEL = 1 means FPWM.
3	FB	Output feedback pin. Connect this pin to the center point of the output resistor divider.
4	GND	Ground pin.
5	SW	Inductor pin. Connect this pin to the switching node of inductor.
6	VIN	Input voltage pin.

Absolute Maximum Ratings

Stresses beyond those listed under the Absolute Maximum Rating table may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Unit
VIN, FB, EN, SEL	Input pin voltage(1)	-0.3	6	V
SW (DC)	Output pin voltage(1)	-0.3	V_{IN} + 0.3	V
SW (DC, in current limit)	Output pin voltage(1)	-1	V_{IN} + 0.3	V
SW (AC, less than 10 ns)(2)	Output pin voltage(1)	-2.5	10	V
T_J	Operating junction	-40	150	°C
T_{STG}	Storage temperature	-65	150	°C
ESD	Human-body model (HBM)		±4000	V
	Charge device model (CDM)		±2000	V

Note:

(1) All voltage values are with respect to the network ground terminal

(2) While switching

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. Does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Input voltage range	2.5		5.5	V
V_{OUT}	Output voltage range	0.6		5.0	V
I_{OUT}	Output current range	0		4.0	A
T_J	Operating junction temperature	-40		125	°C
$R_{\theta JA}$	Junction-to-ambient thermal resistance		107.8		°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		24.2		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		20.5		°C/W

DC Electrical Characteristics

T_J = -40°C to 125°C, and V_{IN} = 2.5 V to 5.5 V. Typical values are at T_J = 25°C and V_{IN} = 5 V, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I_Q	Quiescent current	EN = High, no load, device not switching		10	18	µA
		EN = High, no load, FPWM devices		10		mA
I_{SD}	Shutdown current	EN = Low, T_J = -40°C to 85°C		0.15	0.5	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} rising	2.22	2.35	2.48	V
	Undervoltage lockout hysteresis	V_{IN} falling		150		mV
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
Logic interface EN, SEL						
V_{IH}	High-level threshold voltage	V_{IN} = 2.5 V to 5.5 V	1.0			V
V_{IL}	Low-level threshold voltage	V_{IN} = 2.5 V to 5.5 V			0.4	V
Soft start						
t_{SS}	Soft-start time	Time from EN High to 95% of V_{OUT} nominal		1.8		ms
Output						
V_{FB}(2)	Feedback regulation voltage	2.5 V ≤ V_{IN} ≤ 5.5 V, T_J = -40°C to 125°C	591	600	609	mV
		2.5 V ≤ V_{IN} ≤ 5.5 V, T_J = -20°C to 85°C	594	600	606	mV
$I_{FB,LKG}$	Feedback input leakage current for adjustable output voltage	V_{FB} = 0.6 V		0.01		µA
I_{DIS}	Output discharge current	V_{SW} = 0.4 V, EN = Low		100		mA
	Load regulation	I_{OUT} = 0.5 A to 4 A, V_{OUT} = 1.8 V		0.1		%/A
Power switch						
$R_{DS(on)}$	High-side FET on-resistance			26		mΩ
	Low-side FET on-resistance			25		mΩ
I_{LIM}	High-side FET switch current limit, DC		5.4	6.4		A
	Low-side FET switch current limit, DC(1)				3.5	A
f_{SW}	PWM switching frequency	I_{OUT} = 1 A, V_{OUT} = 1.8 V		2		MHz

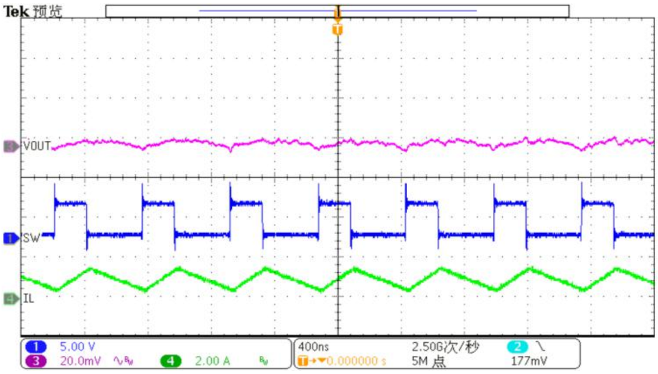
Note:

(1) Specifications subject to change without notice.

(2) Guaranteed by design.

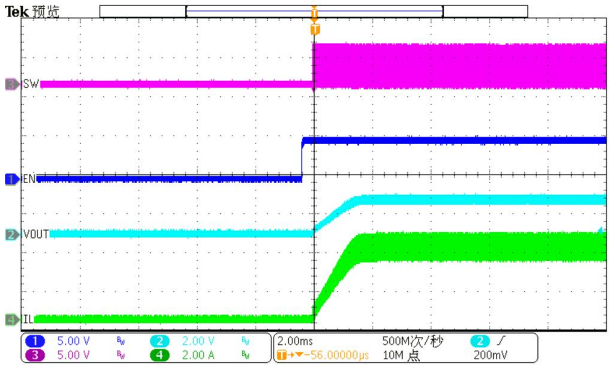
Typical Performance Characteristics

V_{IN} = 5 V, V_{OUT} = 1.8 V, C_{IN} = 2 × 22 µF, C_{OUT} = 3 × 10 µF, C_F = 120 pF, unless otherwise noted.



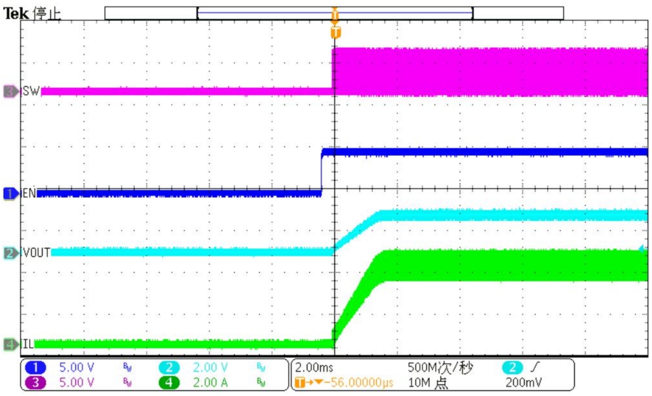
I_{OUT} = 1.0 A

Figure 2. CCM operation



Load = 0.45 Ω

Figure 3. Start-up with load (Auto mode)



Load = 0.45 Ω

Figure 4. Start-up with load (FPWM)

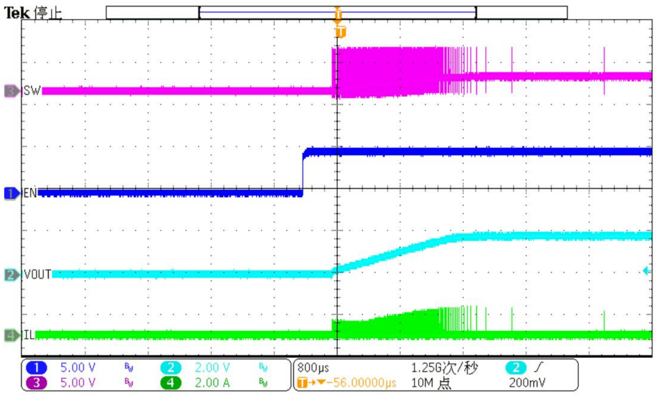


Figure 5. Start-up without load (Auto mode)

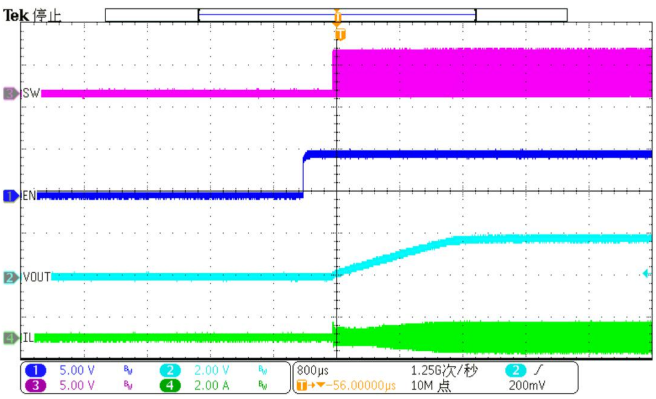
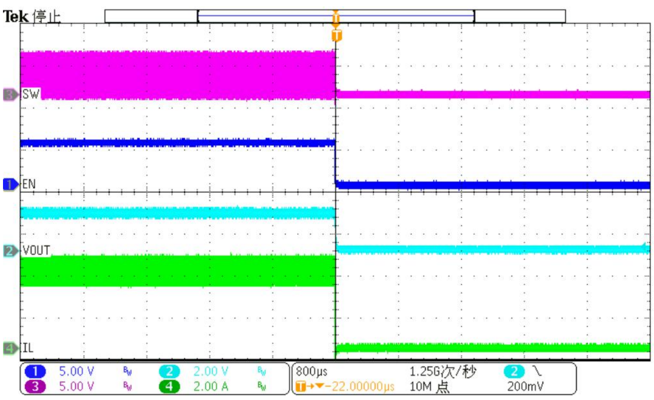
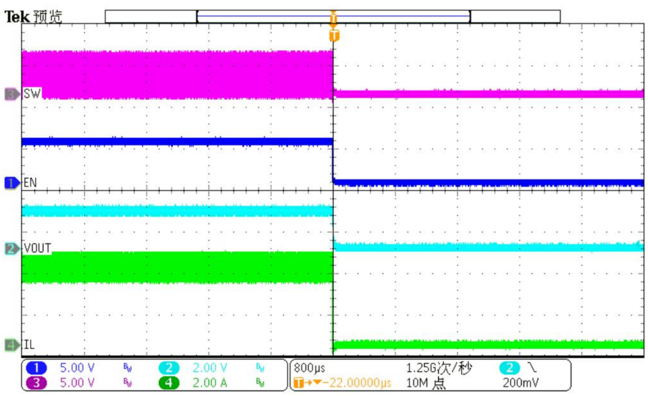


Figure 6. Start-up without load (FPWM)



Load = 0.45 Ω

Figure 7. Disable, active output discharge (Auto mode)



Load = 0.45 Ω

Figure 8. Disable, active output discharge (FPWM)

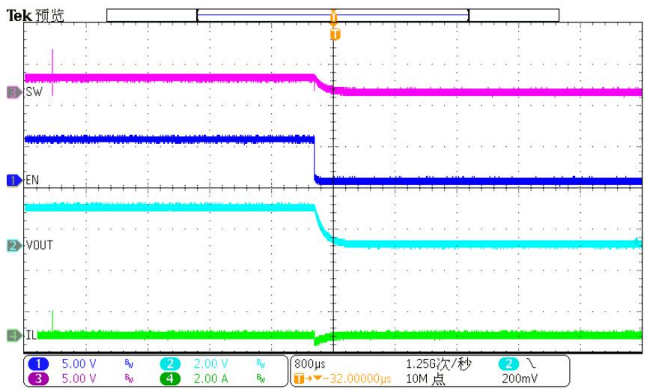


Figure 9. Disable, active output discharge at no load (Auto mode)

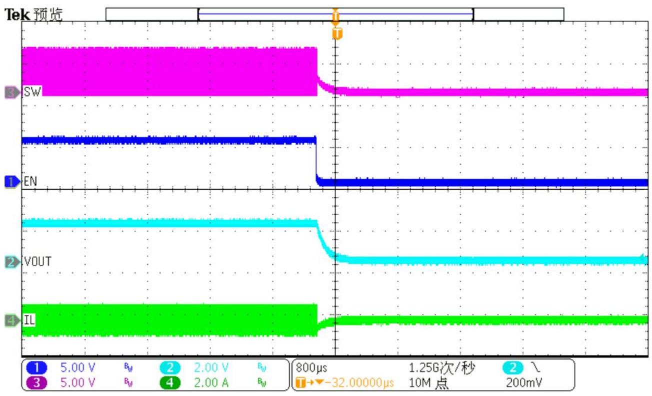
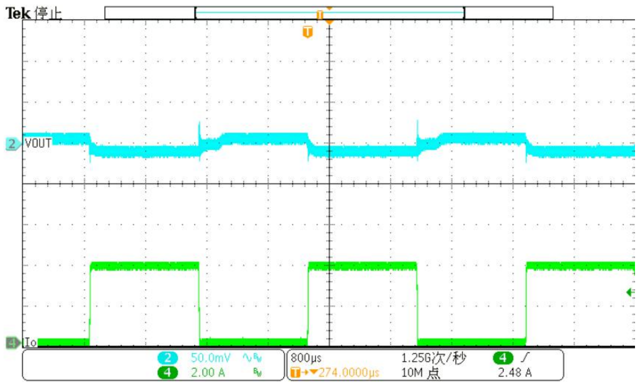
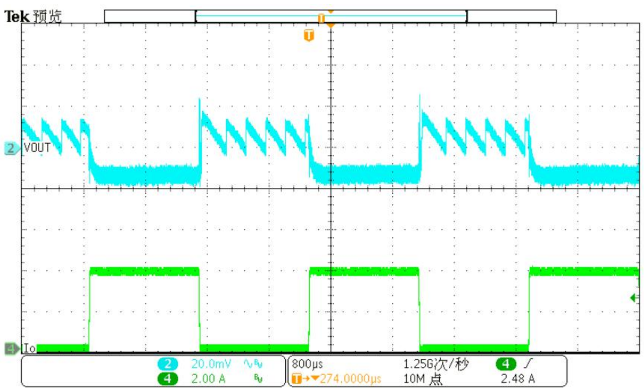


Figure 10. Disable, active output discharge at no load (FPWM)



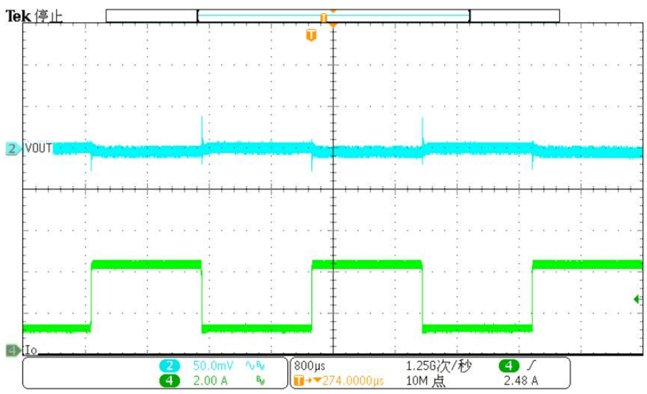
0.001 A -- 4 A

Figure 11. Load Transient (FPWM)



0.001 A -- 4 A

Figure 12. Load Transient (Auto mode)



1 A -- 4 A

Figure 13. Load Transient (FPWM & Auto mode)

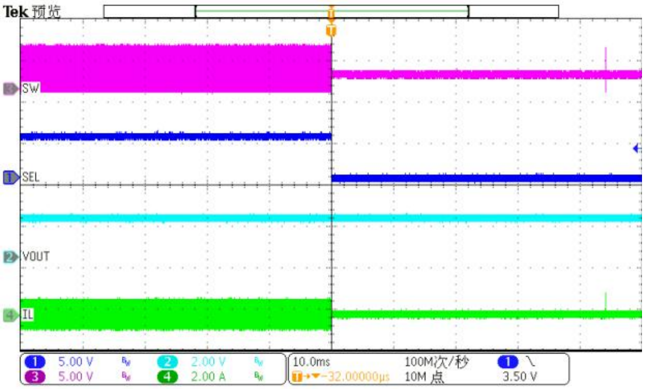
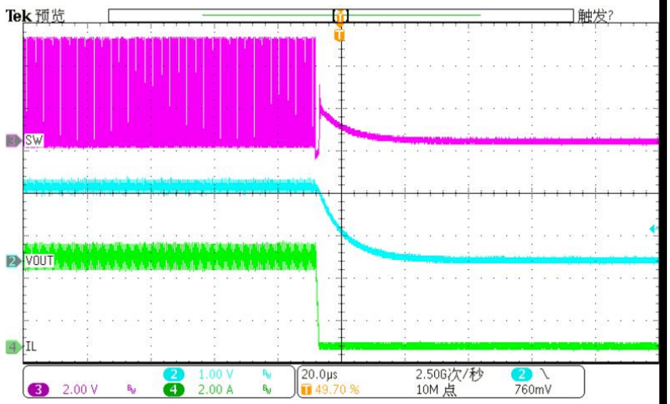
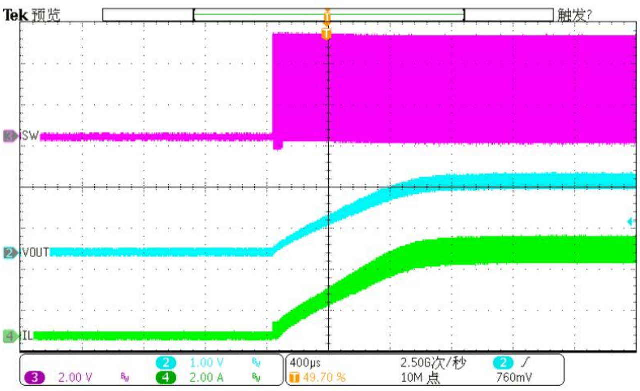


Figure 14. Mode change (FPWM & Auto mode)



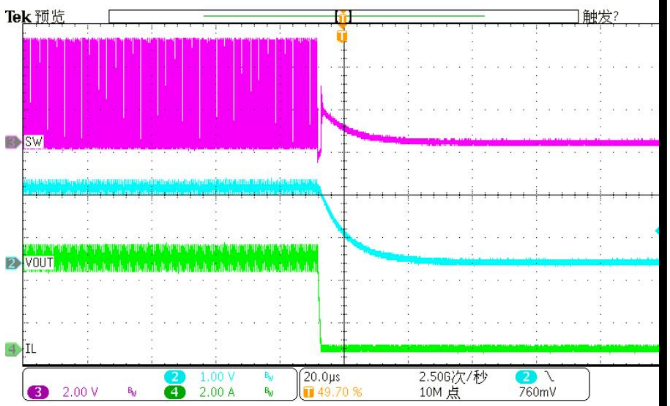
Load = 0.45 Ω

Figure 15. OTP (Auto mode)



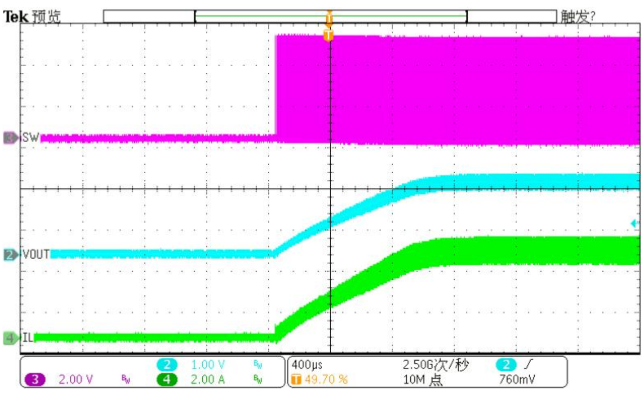
Load = 0.45 Ω

Figure 16. OTP recovery (Auto mode)



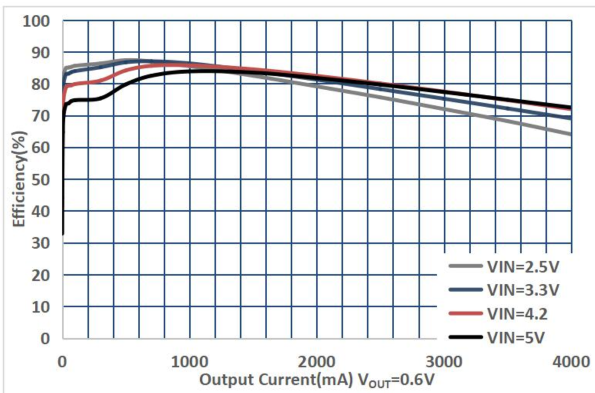
Load = 0.45 Ω

Figure 17. OTP (FPWM)



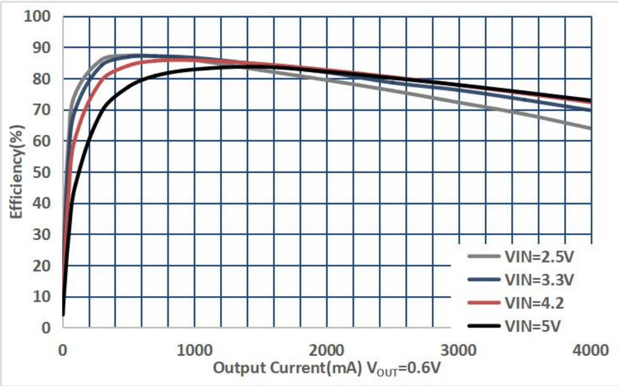
Load = 0.45 Ω

Figure 18. OTP recovery (FPWM)



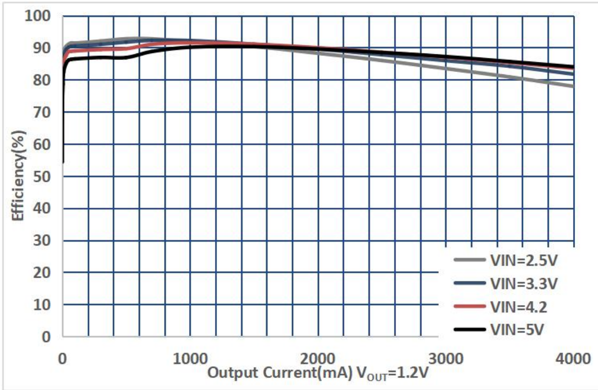
V_{OUT} = 0.6 V

Figure 19. Efficiency vs. Output current (Auto mode)



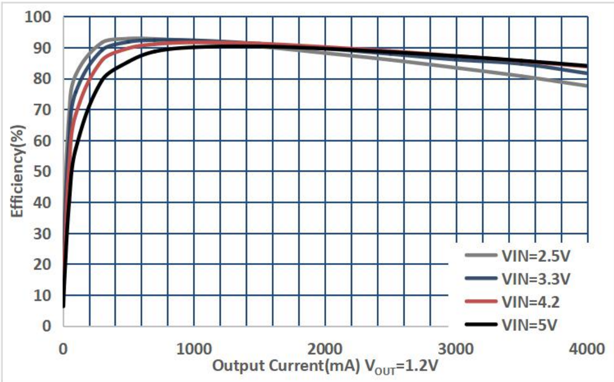
V_{OUT} = 0.6 V

Figure 20. Efficiency vs. Output current (FPWM)



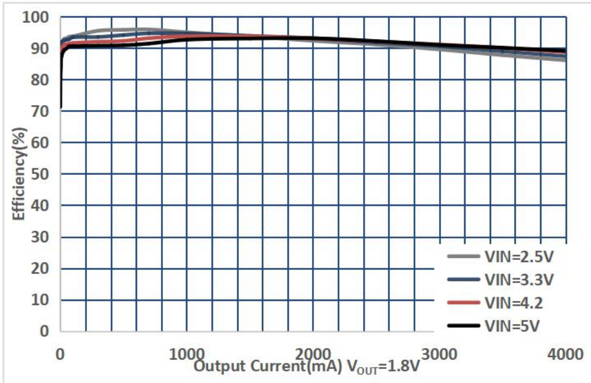
V_{OUT} = 1.2 V

Figure 21. Efficiency vs. *Output current* (Auto mode)



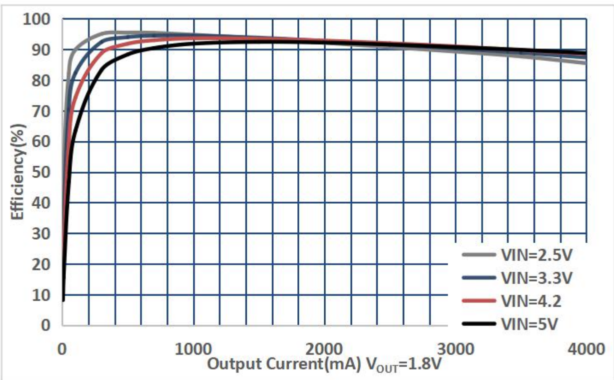
V_{OUT} = 1.2 V

Figure 22. Efficiency vs. Output current (FPWM)



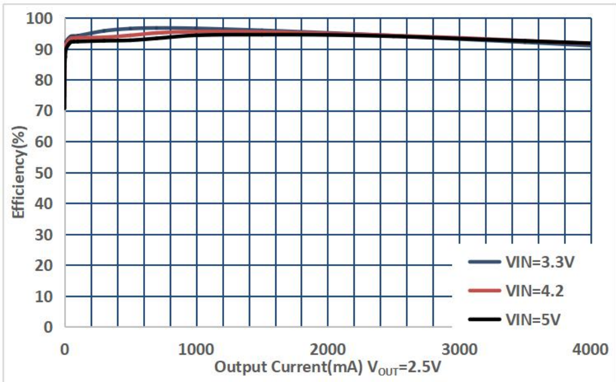
V_{OUT} = 1.8 V

Figure 23. Efficiency vs. Output current (Auto mode)



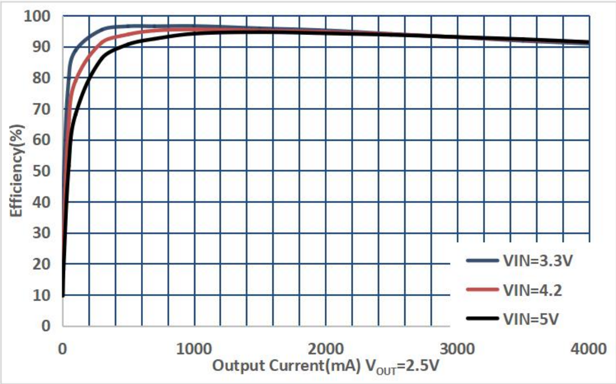
V_{OUT} = 1.8 V

Figure 24. Efficiency vs. Output current (FPWM)



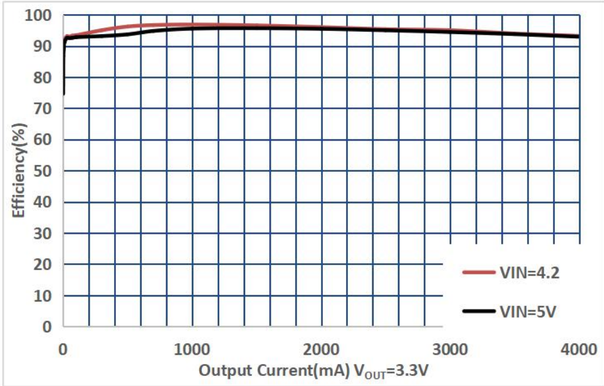
V_{OUT} = 2.5 V

Figure 25. Efficiency vs. Output current (Auto mode)



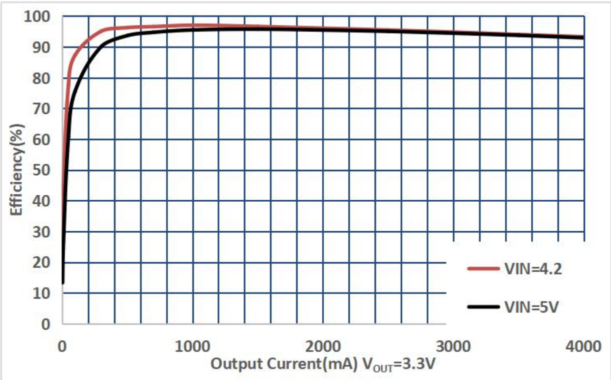
V_{OUT} = 2.5 V

Figure 26. Efficiency vs. Output current (FPWM)



V_{OUT} = 3.3 V

Figure 27. Efficiency vs. Output current (Auto mode)



V_{OUT} = 3.3 V

Figure 28. Efficiency vs. Output current (FPWM)

Block Diagram

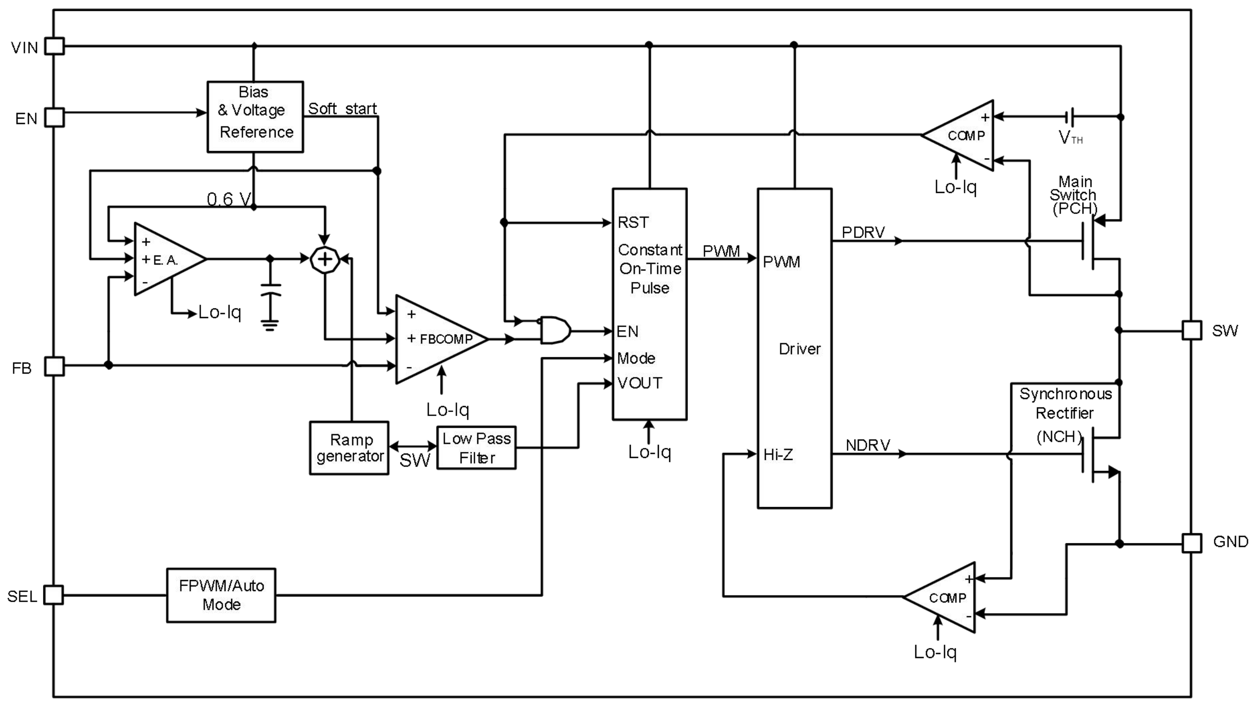


Figure 29. Block diagram

Detailed Description

Overview

The DIO6157 is a synchronous buck regulator IC with an adaptive constant on-time control and top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra-low $R_{DS(ON)}$ power switches and proprietary constant on-time control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size and thus achieve the minimum solution footprint.

The DIO6157 has a selection function, which can select forced pulse width modulation (FPWM) and auto mode. When the SEL pin is pulled to HIGH, the DIO6157 enters the forced pulse width modulation. If the SEL pin is driven LOW, it enters the automatic mode.

During FPWM mode, the converter maintains a continuous conduction mode operation and keeps the output voltage ripple very low across the whole load range. During auto mode, the DIO6157 enters PWM mode for medium to heavy load conditions or enters PSM (Power Save Mode) for a light load. Under PWM mode, the converter operates with a typical 2 MHz switching frequency to minimize the size of the inductor and capacitor. As the load current decreases, the converter enters PSM (Power Save Mode), reducing the switching frequency to keep high efficiency over the entire load current range.

Pulse width modulation (PWM) operation

The device will operate in continuous conduction mode(CCM) when the output current is high. In CCM operation, the switching frequency is fairly constant. This is called pulse-width modulation mode. The PWM operation is based on an adaptive constant on-time (COT) control with stabilized switching frequency. In a steady state condition, the on-time is calculated as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 500ns \quad (1)$$

Power save mode (PSM) operation

Under light load conditions, the DIO6157 enters power save mode to maintain high efficiency. Meanwhile, the device works continuously in discontinuous conduction mode (DCM). This happens when the output current becomes smaller than half of the ripple current of the inductor. The device operates now with a fixed on-time and the switching frequency further decreases proportionally to the load current. It can be calculated as:

$$f_{PSM} = \frac{2 \times I_{OUT}}{t^2{}_{ON} \times \frac{V_{IN}}{V_{OUT}} (\frac{V_{IN} - V_{OUT}}{L})} \quad (2)$$

In PSM, the output voltage rises slightly above the nominal target, which can be minimized using larger output capacitance. At duty cycles larger than 90%, the device may not enter PSM and can only maintain output regulation in PWM mode.

Soft-start

The DIO6157 employs a soft-start (SS) mechanism to ensure smooth output ramping during power-up. When EN goes high, an internal soft-start circuitry controls the output voltage during start-up. The device will initiate switching and the output voltage will smoothly ramp up to its targeted regulation voltage only after this ramp voltage is greater than the feedback voltage V_{FB}. This avoids excessive inrush current and ensures a controlled output voltage ramp.

Switch current limit

The protection function prevents the device from drawing excessive current in case of externally-caused over current. If the current limit threshold is reached, the device delivers its maximum output current. Detecting this condition for 32 switching cycles, the device turns off the high-side MOSFET for about 200 μs and then restarts again with a soft start cycle. As long as the overload condition is present, the device hiccups that way, limiting the output power.

In FPWM devices, a negative current limit (I_{LIMN}) is enabled to prevent excessive current flowing backward to the input. When the inductor current reaches I_{LIMN}, the low-side MOSFET turns off and the high-side MOSFET turns on and is kept on until T_{ON} time expires.

Undervoltage lockout

The DIO6157 being powered up, if the input voltage is larger than a typical 2.35 V, the DIO6157 starts switching. If the input voltage is lower than UVLO_falling with a 150 mV hysteresis, the DIO6157 will be shut down.

Thermal shutdown

The device goes into thermal shutdown as soon as the junction temperature exceeds a typical 150°C with a 20°C hysteresis.

Device functional modes

1. Enable, disable and output discharge

Pulling the EN pin LOW (< 0.4 V) will shut down the device. If the EN pin is driven HIGH (>1 V), the device will be turned on again. Always do not leave EN floating. Shutdown mode is forced if EN is pulled low with a shutdown current of a typical 150 nA. During shut down mode, the device is turned off and the output voltage is actively discharged through the SW pin by a current sink.

2. SEL

The DIO6157 has the selection function. Either forced pulse width modulation (FPWM) mode or Auto mode can be selected. When the SEL pin is pulled HIGH, the DIO6157 enters the forced pulse width modulation. When the SEL pin is driven LOW, the DIO6157 enters the Auto mode. (see Table 1).

Table 1. SEL pin Logic

Operation Mode	SEL Pin
FPWM	H
Auto mode	L

Typical Applications

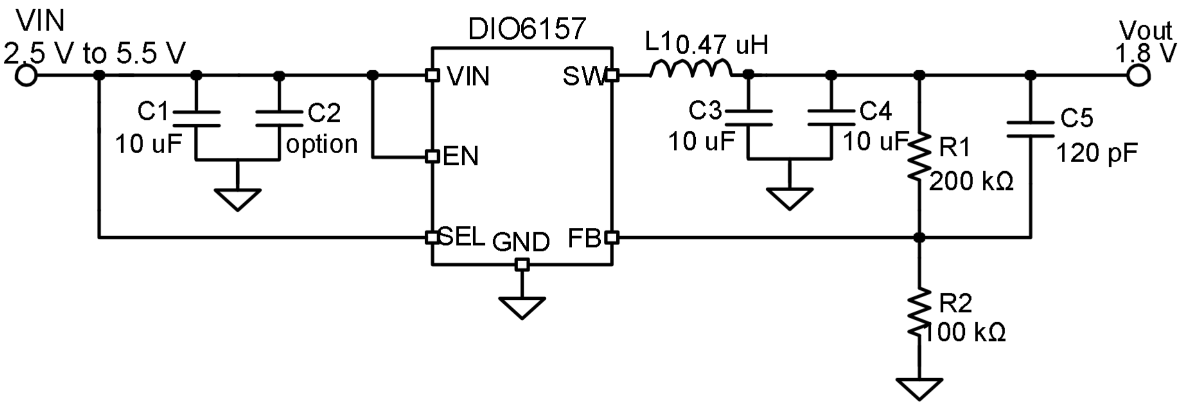


Figure 30. FPWM typical applications

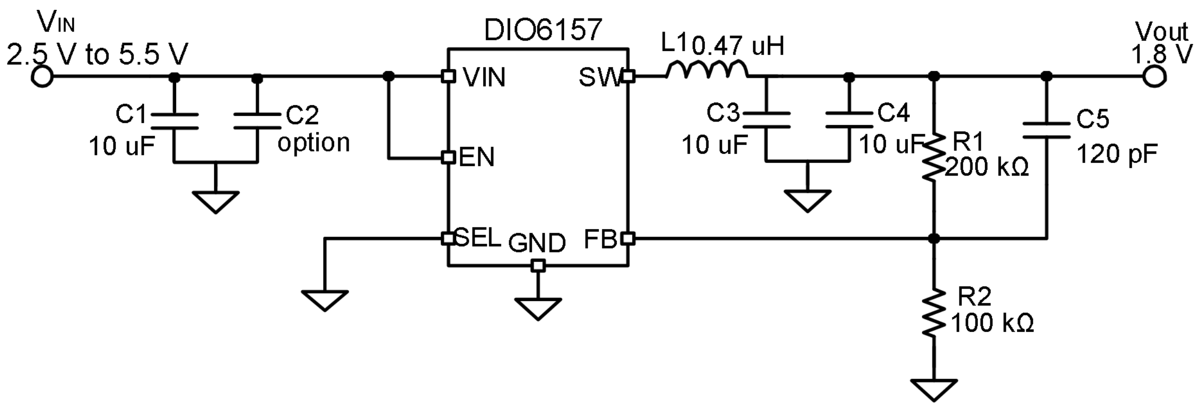


Figure 31. Auto mode typical applications

Application information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

Design requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design parameters

Design Parameter	Example Value
Input voltage	2.5 V to 5.5 V
Output voltage	1.8 V
Output ripple voltage	< 20 mV
Maximum output current	4 A

Table 3 lists the components used for the example.

Table 3. List of components

Reference	Description	Manufacturer
C1	10 μF, ceramic capacitor, 10 V, X7R, size 0603, GRM188Z71A106MA73D	Murata
C2	Option	-
C3	10 μF, ceramic capacitor, 10 V, X7R, size 0603, GRM188Z71A106MA73D	Murata
C4	10 μF, ceramic capacitor, 10 V, X7R, size 0603, GRM188Z71A106MA73D	Murata
C5	120 pF, ceramic capacitor, 50 V, size 0402	Std
L1	0.47 μH, power Inductor, XFL4015-471MEB	Coilcraft
R1	Depending on the output voltage, 1%, size 0402	Std
R2	100 kΩ, chip resistor, 1/16 W, 1%, size 0402	Std

Detailed Design Procedure

Setting the output voltage

Set the desired output voltage by using a resistive divider from the output to ground with the midpoint connected to FB. The output voltage is set by an external resistor divider according to Equation 3:

$$R1 = R2 \times (\frac{V_{OUT}}{V_{FB}} - 1) = R2 \times (\frac{V_{OUT}}{0.6V} - 1) \quad (3)$$

R2 must not be higher than 100 kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity. Equation 4 shows how to compute the value of the feedforward capacitor for a given R2 value. For the recommended 100 kΩ value for R2, a 120 pF feedforward capacitor is used.

$$C5 = \frac{12\mu}{R2} \quad (4)$$

Output filter design

The inductor and the output capacitor together provide a low-pass filter function. To simplify this process, Table 4 recommends the inductor and capacitor value combinations. Checked cells represent combinations that are proven for stability by simulation and lab tests. Further combinations should be checked for each individual application.

Table 4. Matrix of output capacitor and inductor combinations

Nominal L (μH)[2]	Nominal C_{OUT} (μF)[3]			
	10	2 × 10 or 22	47	100
0.33				
0.47	+	+ [1]	+	
1.0				

Note

(1) This LC combination is the standard value and recommended for most applications.

(2) Inductor tolerance and current de-rating are anticipated. The effective inductance can vary by 20% and -30%.

(3) Capacitance tolerance and bias voltage de-rating are anticipated. The effective capacitance can vary by 20% and -35%.

Inductor selection

Selecting an inductor involves specifying its inductance and also its required peak current. Lowering the inductor values helps to reduce the size and cost, thus improving the circuit's transient response. Meanwhile, it increases the inductor ripple current and output voltage ripple. Also lowering the inductor value reduces the efficiency due to the higher peak currents. To calculate the maximum inductor current under static load conditions, Equation 5 is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2} \quad (5)$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (6)$$

Where

- $I_{OUT,MAX}$ = Maximum output current
- ΔI_L = Inductor current ripple
- f_{SW} = Switching frequency
- L = Inductor value

It is recommended to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size should also be taken into account when selecting an appropriate inductor. Table 5 lists recommended inductors.

Table 5. List of recommended inductors

Inductance (μH)	Current Rating (A)	Dimensions (L x W x H mm)	MAX. DC Resistance (mΩ)	Manufacturer Part Number
0.47	4.8	2.0 x 1.6 x 1.0	32	HTEN20161T-R47MDR, Cyntec
	4.6	2.0 x 1.2 x 1.0	25	HTEH20121T-R47MSR, Cyntec
	4.8	2.0 x 1.6 x 1.0	32	DFE201610E-R47M, MuRata
	4.8	2.0 x 1.6 x 1.0	32	DFE201210S-R47M, MuRata
	5.1	2.0 x 1.6 x 1.0	34	TFM201610ALM-R47MTAA, TDK
	5.2	2.0 x 1.6 x 1.0	25	TFM201610ALC-R47MTAA, TDK
	6.6	4.0 x 4.0 x 1.6	8.36	XFL4015-471ME, Coilcraft
	8.0	3.5 x 3.2 x 2.0	10.85	XEL3520-471ME, Coilcraft
	6.8	4.5 x 4 x 1.8	11.2	WE-LHMI-744373240047, Würth

Capacitor selection

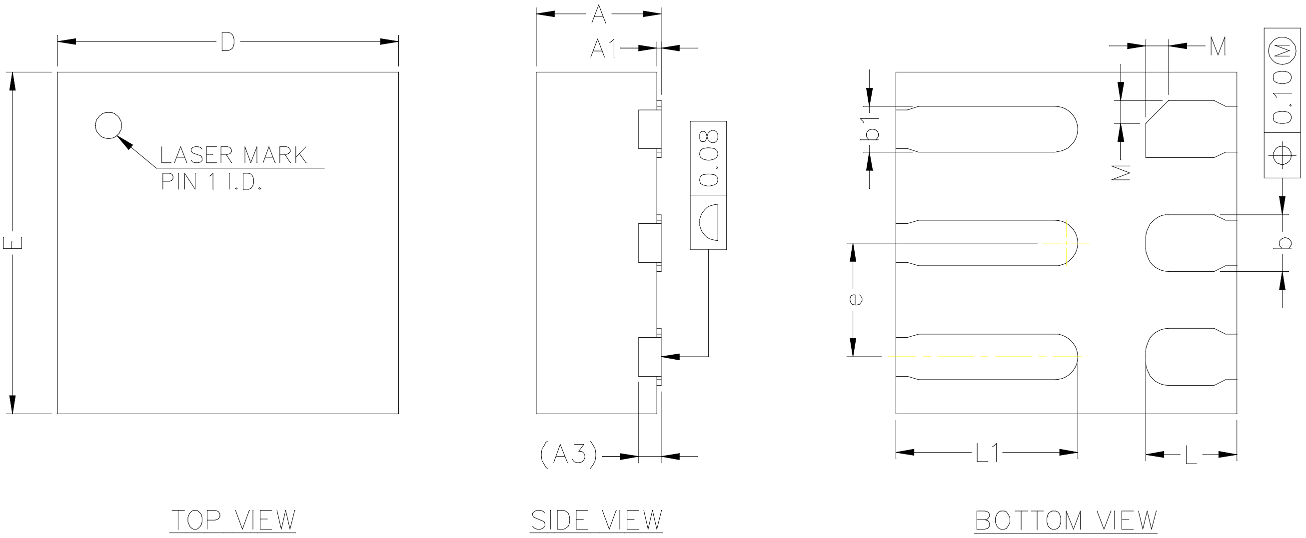
The IC is optimized for ceramic output capacitors. The input capacitor is the low-impedance energy source for the converters which helps to provide stable operation. A low-ESR multilayer ceramic capacitor is recommended for the best filtering and must be placed between VIN and GND as close as possible.

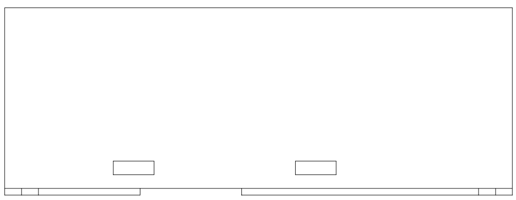
The architecture of the device allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple. DIOO recommends using X7R or X5R dielectrics.

Power supply recommendations

The device is designed to operate from an input voltage supply range from 2.5 V to 5.5 V. Ensure that the input power supply has a sufficient current rating for the application.

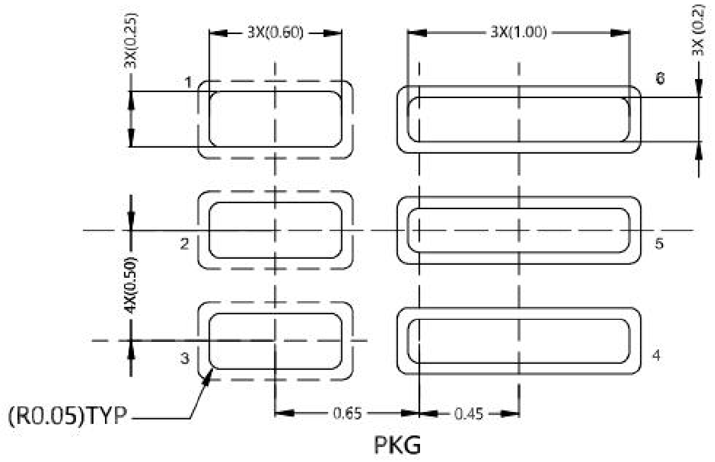
Physical Dimensions:DFN1.5*1.5-6



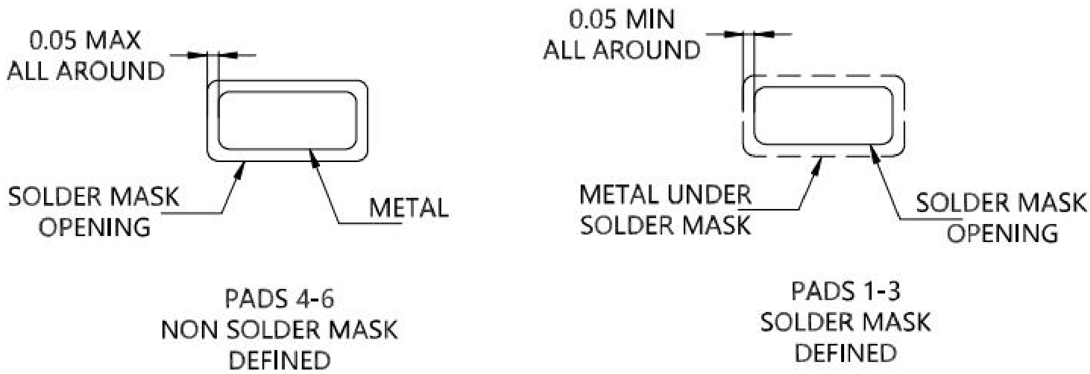


SIDE VIEW

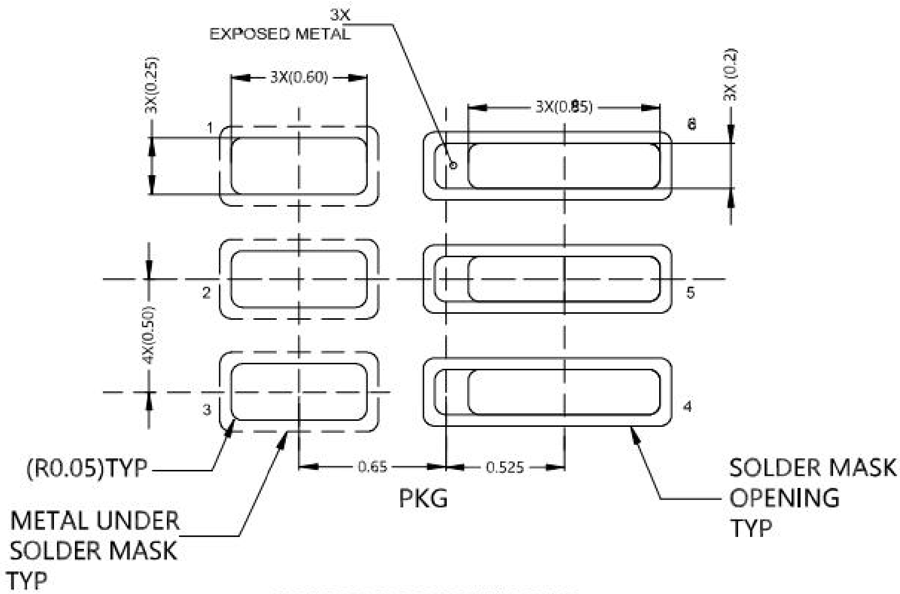
Common Dimensions (Units of measure = Millimeter)			
Symbol	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3		0.10 REF	
b	0.20	0.25	0.30
b1	0.15	0.20	0.25
D	1.40	1.50	1.60
E	1.40	1.50	1.60
e	0.40	0.50	0.60
L	0.30	0.40	0.50
L1	0.70	0.80	0.90
M		0.10 REF	



LAND PATTERN EXAMPLE



SOLDER MASK DETAILS



SOLDER PASTE EXAMPLE

Revision History

- **Revision 0.1 initial preliminary datasheet**
- **Revision 0.2 change the Adjustable output voltage from "0.6 V to 4 V"to "0.6 V to 5 V" ; change Human-body model (HBM) from ±5000 to ±3000.**
- **Revision 0.3 change the DC Electrical Characteristics-I_Q(EN = High, no load, FPWM devices, TYP) from "9 mA" to "10 mA",delete the I_Q (MAX).**
- **Revision 1.0 change Human-body model (HBM) from "±3000" to "±4000"; add Charge device model (CMD) (±2000); delete Ψ_{JT} and Ψ_{JB}; change the $R_{\theta JA}$ from "129.5" to "107.8",change the $R_{\theta JC(top)}$ from "103.9" to "24.2",change the $R_{\theta JA}$ from "33.1" to "20.5" ; Added the Typical Performance Characteristic.**

CONTACT US

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