

High-Efficiency 2 A, 20 V Input Synchronous Step-Down Converter

■ Features

- Low $R_{DS(ON)}$ for internal switches (top/bottom) 76 mΩ/43 mΩ, 2.0 A
- 4.5 to 20 V input voltage range
- Switching frequency: 800 kHz
- Feedback reference voltage: 0.8 V
- High-efficiency synchronous-mode
- Internal soft start limits the inrush current
- Overcurrent protection
- Thermal shutdown

■ Applications

- Portable navigation device
- Set top box
- Portable TV
- LCD TV

■ Package Information

Part Number	Package	Body Size
DIO6966	SOT563	1.6 mm × 1.2 mm

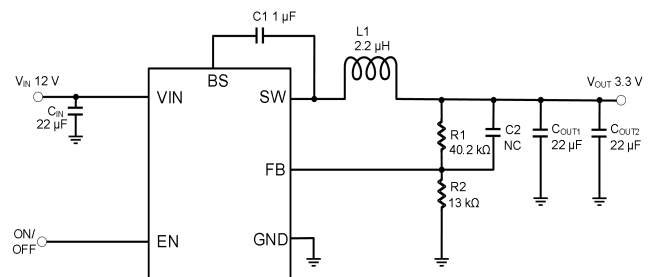
■ Description

The DIO6966 is a high-efficiency, high frequency synchronous step-down DC-DC regulator IC capable of delivering up to 2.0 A output currents. The DIO6966 operates over a wide input voltage range from 4.5 V to 20 V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The COT architecture with pseudo fixed switching frequency operation provides fast transient response and eases loop stabilization. Protection features include overcurrent protection and thermal shutdown.

The DIO6966 requires a minimal number of readily-available, standard, external components and is available in a space-saving SOT563 package.

■ Simplified Schematic



■ Ordering Information

Ordering Part No.	Top Marking	MSL	RoHS	T _A	Package	
DIO6966SH3	W6H	3	Green	-40 to 85°C	SOT563	Tape & Reel, 5000

If you encounter any issue in the process of using the device, please contact our customer service at marketing@dioo.com or phone us at (+86)-21-62116882. If you have any improvement suggestions regarding the datasheet, we encourage you to contact our technical writing team at docs@dioo.com. Your feedback is invaluable for us to provide a better user experience.

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1. Pin Assignment and Functions

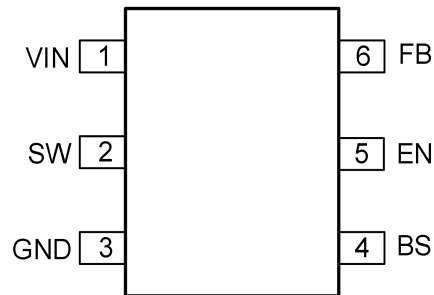


Figure 1. SOT563 (Top view)

Table1. Pin description

Pin Name	Description
VIN	Power input
SW	Inductor pin. Connect this pin to the switching node of inductor.
GND	Power ground
BS	Bootstrap. Connect a capacitor and a resistor between SW and BS pins to form a floating supply across the high-side switch driver.
EN	Enable control. Pull high to turn on. Do not float.
FB	Output feedback pin. Connect this pin to the center point of the output resistor divider to program the output voltage: $V_{OUT} = 0.8 \times (1 + R1/R2)$. Add optional C2 (10 pF ~ 47 pF) to speed up the transient response.

2. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter		Rating	Unit
V_{IN}	Supply voltage (V_+ – V_-)		22	V
	EN, SW voltage		$V_{IN} + 0.3$	V
V_{FB}	FB voltage		6	V
V_{BS}	BS voltage		$V_{SW} + 6$	V
P_D	Power dissipation, P_D at $T_A = 25^\circ\text{C}$, SOT563		1	W
θ_{JA}	Package thermal resistance		130	$^\circ\text{C/W}$
θ_{JC}			60	
T_{STG}	Storage temperature		-65 to 150	$^\circ\text{C}$
T_J	Junction temperature		150	$^\circ\text{C}$
T_L	Lead temperature range		260	$^\circ\text{C}$
ESD	HBM: JESD22-A114	All pins	± 2	kV

3. Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Rating	Unit
V_{IN}	Supply voltage		4.5 to 20	V
T_J	Junction temperature		-40 to 125	$^\circ\text{C}$
T_A	Ambient temperature		-40 to 85	$^\circ\text{C}$

4. Electrical Characteristics

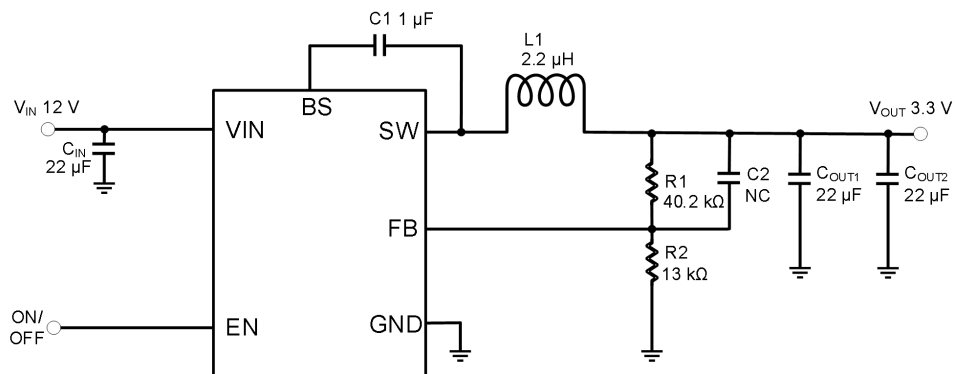
$V_{IN} = 12\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $L = 2.2\text{ }\mu\text{H}$, $C_{OUT} = 47\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$, $I_{OUT} = 1\text{ A}$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage range		4.5		20	V
I_Q	Quiescent current	$I_{OUT} = 0$, $V_{FB} = V_{REF} \times 105\%$		180		μA
I_{SHDN}	Shutdown current	$EN = 0$		10	15	μA
V_{REF}	Feedback reference voltage		0.79	0.8	0.81	V
I_{FB}	FB input current	$V_{FB} = 3.3\text{ V}$	-50		50	nA
$R_{DS(ON)}^{(1)}$	Top FET R_{ON}			76		m Ω
$R_{DS(ON)}^{(1)}$	Bottom FET R_{ON}			43		m Ω
I_{LIM}	Low side power FET current limit		2.5	3.5		A
V_{ENH}	EN rising threshold		1.12	1.2	1.28	V
V_{ENL}	EN hysteresis			60		mV
V_{UVLO}	V_{IN} under-voltage unlock threshold, rising			4	4.35	V
f_{SW}	Switching frequency			800		kHz
t_{ON}	Min ON time			40		ns
t_{OFF}	Min OFF time			180		ns
t_{SS}	Soft start time			0.6		ms
T_{SD}	Thermal shutdown temperature			160		$^\circ\text{C}$
T_{SD-HYS}	Thermal shutdown hysteresis			25		$^\circ\text{C}$

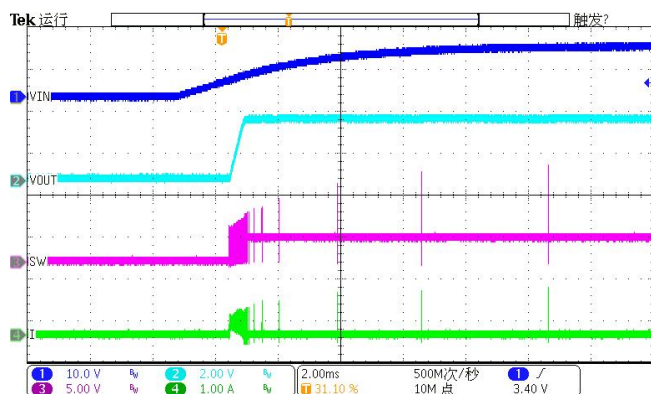
Note:

- (1) Guaranteed by design.
- (2) Specifications subject to change without notice.

5. Typical Application

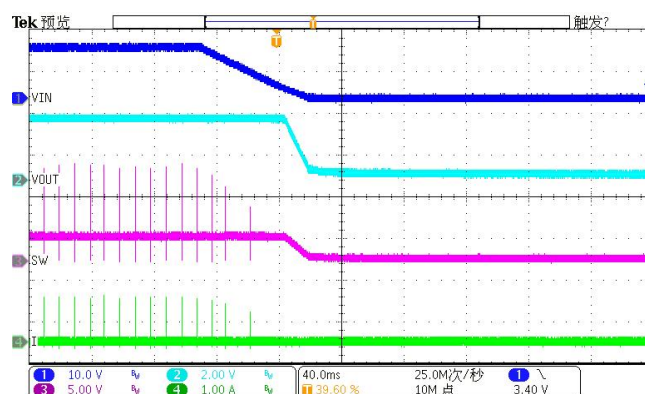


6. Typical Performance Characteristics



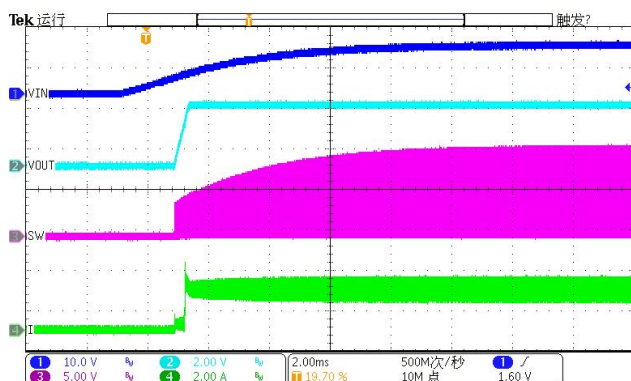
$V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, No load

Figure 2. Start up from V_{IN}



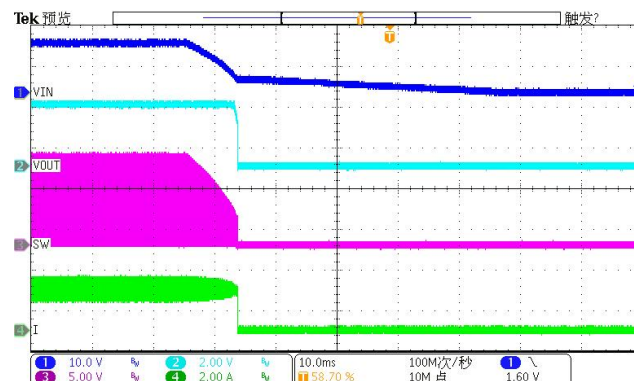
$V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, No load

Figure 3. Shutdown from V_{IN}



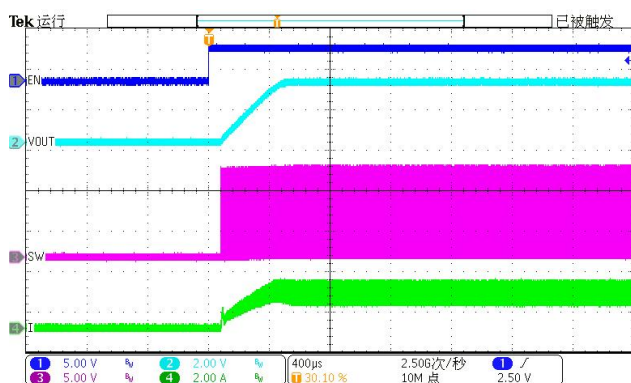
$V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, Load = 2 A

Figure 4. Start up from V_{IN}



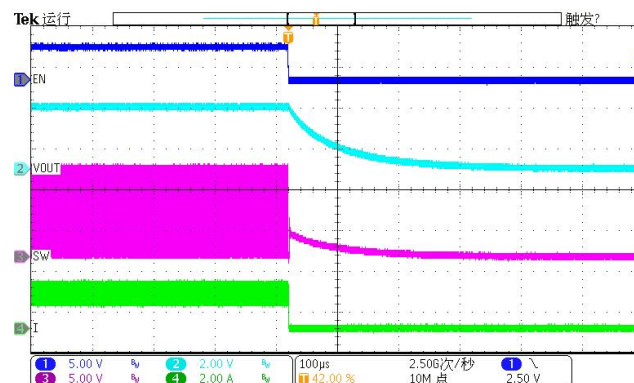
$V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, Load = 2 A

Figure 5. Shutdown from V_{IN}



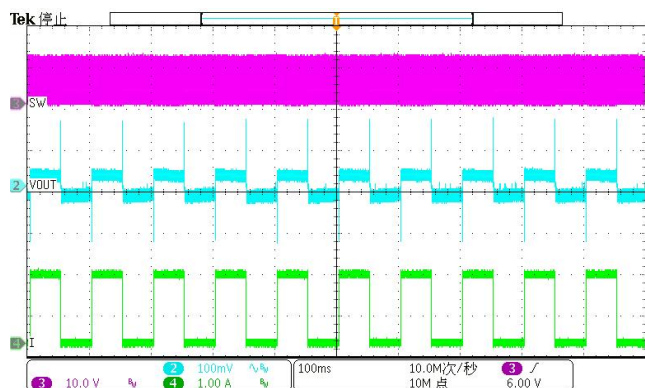
$V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, Load = 1.65 Ω

Figure 6. Start up from enable



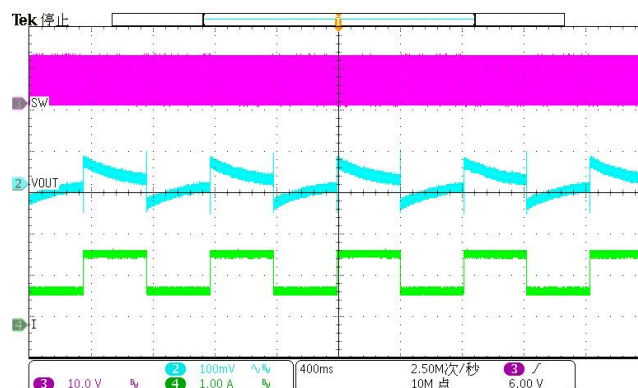
$V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, Load = 1.65 Ω

Figure 7. Shutdown from enable



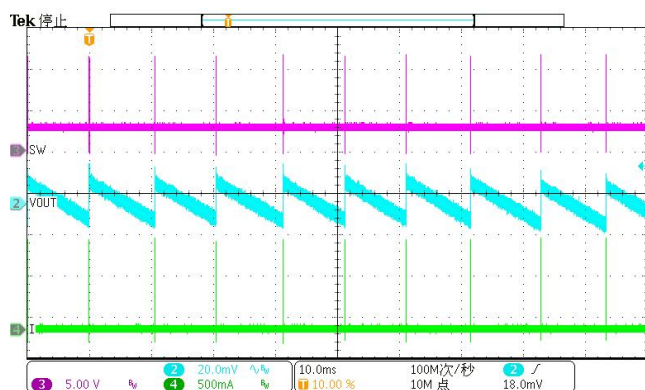
$V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, Load = 10 mA ~ 2 A

Figure 8. Load transient



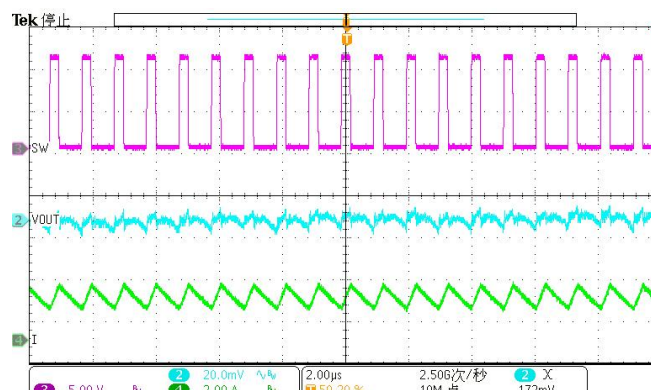
$V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, Load = 1 A ~ 2 A

Figure 9. Load transient



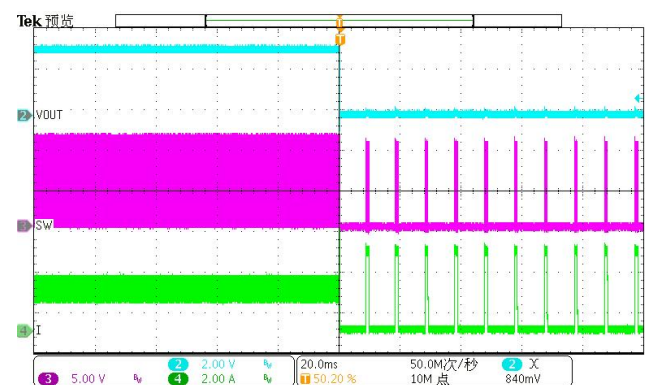
$V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, Load = 0 A

Figure 10. Ripple



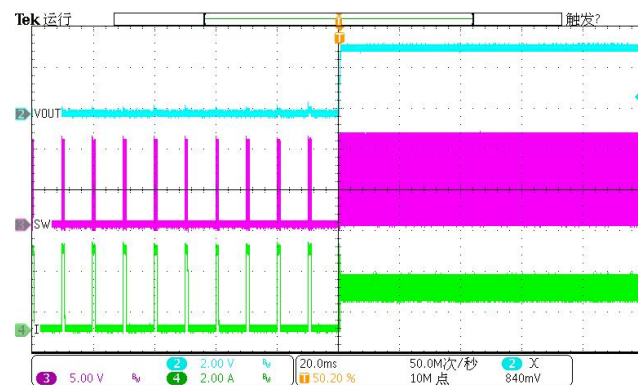
$V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, Load = 2 A

Figure 11. Ripple



$V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, Load = 2 A

Figure 12. Short circuit protection



$V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, Load = 2 A

Figure 13. Short circuit recovery

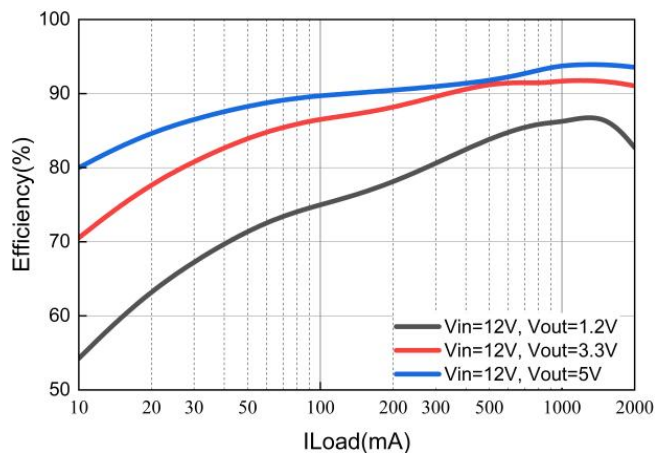


Figure 14. Efficiency vs. Output current

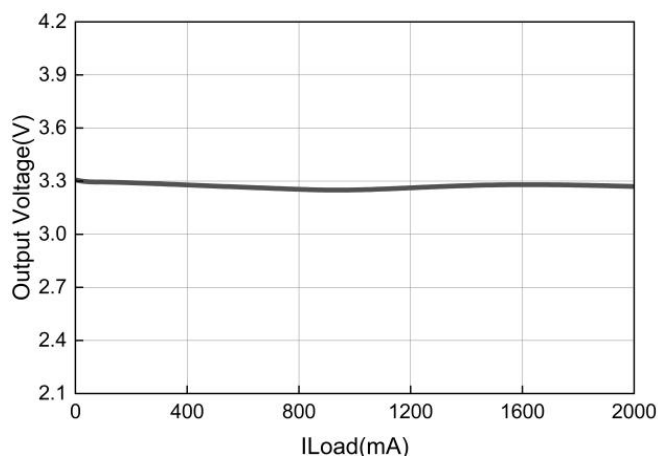


Figure 15. Output voltage vs. Output current

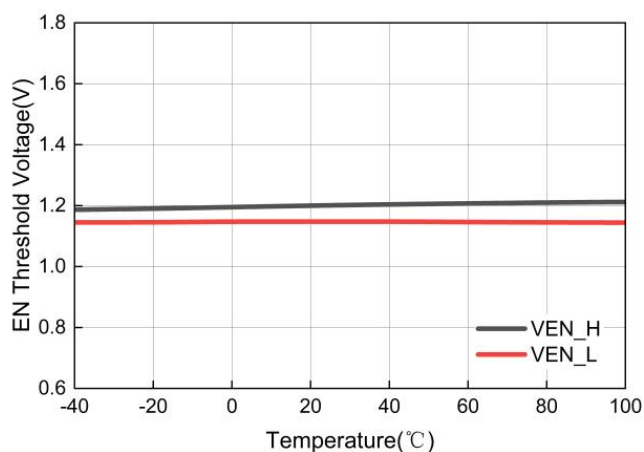


Figure 16. EN threshold voltage vs. Temperature

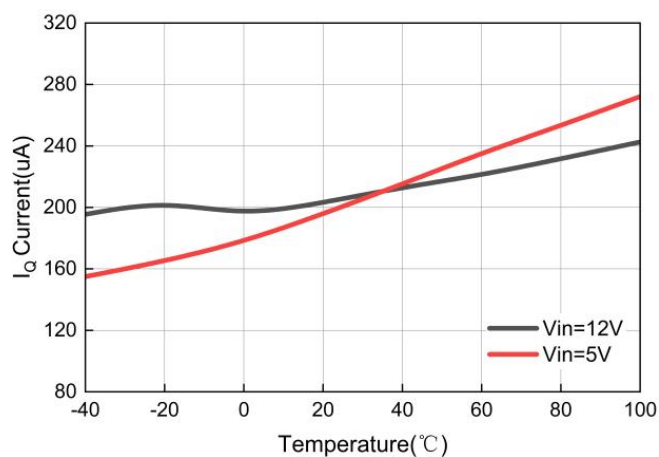


Figure 17. IQ vs. Temperature

7. Application Information

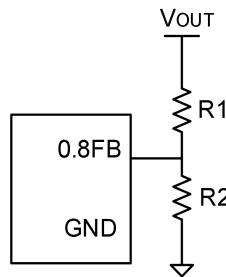
The DIO6966 is a synchronous buck regulator IC that integrates the COT control, top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra low $R_{DS(ON)}$ power switches and proprietary COT control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size, and thus achieving the minimum solution footprint.

Because of the high integration in the DIO6966 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN} , output capacitor C_{OUT} , output inductor L and feedback resistors (R1 and R2) need to be selected for the targeted applications specifications.

7.1. Feedback resistor dividers R1 and R2

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 10 k Ω and 1 M Ω is highly recommended for both resistors. If V_{OUT} is 3.3 V, $R_1 = 40.2$ k Ω is chosen, then R2 can be calculated to be 13 k Ω .

$$R_2 = \frac{0.8V}{V_{OUT} - 0.8V} R_1 \quad (1)$$



7.2. Input capacitor C_{IN}

This ripple current through input capacitor is calculated as:

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{D(1-D)} \quad (2)$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$ condition, where $I_{CIN_RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for DC/DC design.

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN} , and IN/GND pins. In this case, a 22 μ F low ESR ceramic capacitor is recommended.

7.3. Output capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor greater than 22 μ F capacitance.

7.4. Output inductor L

There are several considerations in choosing this inductor.

- 1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN, MAX})}{f_{SW} \times I_{OUT, MAX} \times 40\%} \quad (3)$$

where f_{SW} is the switching frequency and $I_{OUT, MAX}$ is the maximum load current. The DIO6966 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

- 2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT, MIN} > I_{OUT, MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN, MAX})}{2 \times f_{SW} \times L} \quad (4)$$

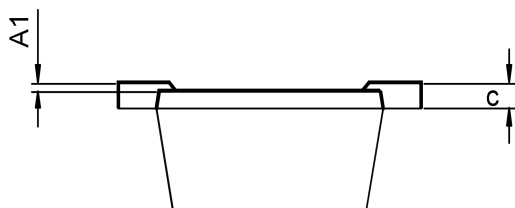
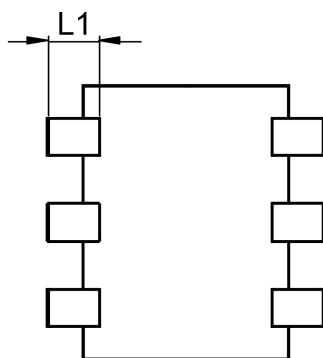
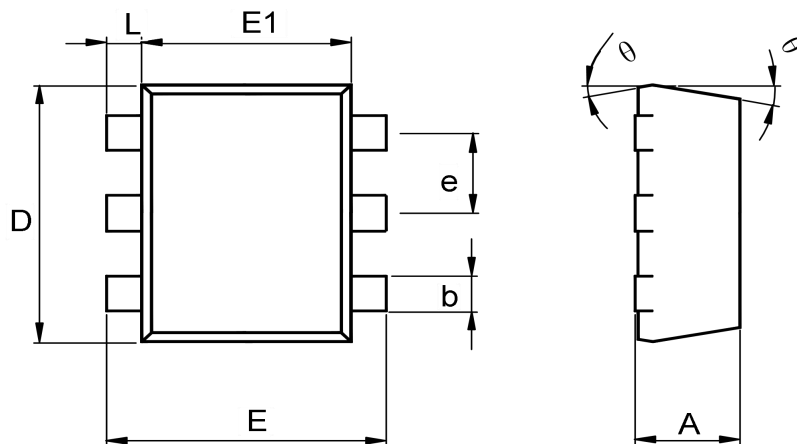
- 3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR < 50 mΩ to achieve a good overall efficiency.

7.5. Layout design

The layout design of DIO6966 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN} , L, R1 and R2.

- 1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.
- 2) C_{IN} must be close to pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.
- 3) The PCB copper area associated with SW pin must be minimized to avoid the potential noise problem.
- 4) The components R1 and R2, and the trace connecting to the FB pin must NOT be adjacent to the SW net on the PCB layout to avoid the noise problem.
- 5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1 MΩ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

8. Physical Dimensions: SOT563



Common Dimensions (Units of measure = Millimeter)		
Symbol	Min	Max
A	0.525	0.600
A1	0.000	0.050
e	0.450	0.550
c	0.090	0.180
D	1.500	1.700
b	0.170	0.270
E1	1.100	1.300
E	1.500	1.700
L	0.100	0.300
L1	0.200	0.400
θ	9° REF	

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