DIO6905C
2 A, Synchronous, Step-Down Converter with Low 15 µA Quiescent Current

Features

- Input voltage range from 2.3 V to 5.5 V
- Up to 2 A output current
- Low quiescent current: 15 µA
- Output adjustable from 0.6 V
- 1.65 MHz typical switching frequency
- EN for power sequencing
- Forced PWM operation
- Low $R_{DS(ON)}$ for internal switches (Top / Bottom): 120 mΩ / 80 mΩ
- Output discharge function
- 100% duty cycle in drop
- Hiccup for short-circuit protection (SCP)
- Stable with low ESR output ceramic capacitors
- Available in SOT563 package

Descriptions

The DIO6905C is a high-efficiency, 1.65 MHz synchronous step down DC / DC converter with power MOSFETs integrated. It can achieve an output current of 2 A under an input voltage of 2.3 V to 5.5 V, and has good load and line regulation. The output voltage can be adjusted from 0.6 V.

The DIO6905C adopts the COT architecture to achieve fast transient responses and simplifies loop stability. In addition, it operates full protection features include cycle-by-cycle current limit and thermal shutdown.

The DIO6905C is packaged in SOT563, which uses fewer external components, enabling a cost-effective solution.

Applications

- Wireless / Networking cards
- Portable and mobile devices
- Battery-powered devices
- Low-voltage I/O system power
- Solid-state drives (SSDs)

Ordering Information

Part Number	Top Marking	RoHS	T_A	Package	
DIO6905CSH3	W5C	Green	-40 to 85°C	SOT563	Tape & Reel, 5000

Pin Assignments

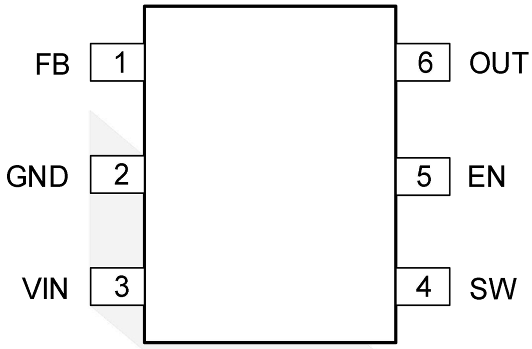


Figure 1. SOT563 (Top view)

Pin Definitions

Pin Name	Description
FB	**Feedback.** An external resistor divider from the output to GND tapped to FB sets the output voltage.
GND	**Power ground.**
VIN	**Supply voltage.** The DIO6905C operates from a 2.3 V to 5.5 V unregulated input. A decoupling capacitor is required to prevent large voltage spikes from appearing at the input.
SW	**Output switching node.** SW is the drain of the internal high-side P-channel MOSFET. Connect the inductor to SW to complete the converter.
EN	**On/off control.**
OUT	**Output voltage power rail and input sense for the output voltage.** Connect the load to OUT. An output capacitor is required to decrease the output voltage ripple.

Absolute Maximum Ratings

Stresses beyond those listed under the Absolute Maximum Rating table may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Rating	Unit
V_{CC}	Supply voltage (V_{IN})	6.0	V
V_{SW}		-0.3 (-5 V for < 20 ns) to 6.0 (8 V for < 20 ns or 10 V for < 10 ns)	V
	All other pins	-0.3 to 6.0	V
T_J	Junction temperature range	150	°C
T_L	Lead temperature range	260	°C
P_D	Continuous power dissipation (T_A = 25°C)	1	W
T_{STG}	Storage temperature	-65 to 150	°C
ESD	Human body mode	2000	V
	Latch-up	200	mA

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating	Unit
V_{IN}	Supply voltage	2.3 to 5.5	V
T_J	Operating junction temperature range	-40 to 125	°C
θ_{JA}	Package thermal resistance	130	°C/W
θ_{JC}		60	

Electrical Characteristics

V_{IN} = 3.6 V, T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{FB}	Feedback voltage	2.3 V ≤ V_{IN} ≤ 5.5 V, T_J = 25°C	594	600	606	mV
		T_J = -40°C to 125°C[2]	588		612	
V_{UVLO}	Under-voltage lockout threshold rising			2.1	2.3	V
	Under-voltage lockout threshold hysteresis			50		mV
V_{IL}	EN input logic low voltage				0.4	V
V_{IH}	EN input logic high voltage		1.2			V
I_{LKG_EN}	EN input current	V_{EN} = 2 V		2		µA
		V_{EN} = 0 V		0		µA
I_{SD}	Supply current (shutdown)	V_{EN} = 0 V, T_J = 25°C		0	1	µA
I_q	Supply current (quiescent)	V_{EN} = 2 V, V_{FB} = 0.63 V, V_{IN} = 3.6 V, 5 V, T_J = 25°C		15	30	µA
I_{FB}	Feedback current	V_{FB} = 0.63 V		50	100	nA
R_{DSON_P}	P-FET switch on resistance			120		mΩ
R_{DSON_N}	N-FET switch on resistance			80		mΩ
R_{DIS}	Output discharge resistor	V_{EN} = 0 V, V_{OUT} = 1.2 V		1		kΩ
I_{LKG_P}	Switch leakage current	V_{EN} = 0 V, V_{IN} = 6 V, V_{SW} = 0 V and 6 V, T_J = 25°C		0	1	µA
I_{LIM_P}	P-FET peak current limit	Sourcing	2.8	3.2		A
I_{LIM_N}	N-FET valley current limit	Sourcing, valley current limit		1.6		A
	ZCD			0		mA
T_{ON}	On time	V_{IN} = 5 V, V_{OUT} = 1.2 V		145		ns
		V_{IN} = 3.6 V, V_{OUT} = 1.2 V		202		
f_S	Switching frequency	V_{IN} = 5 V, V_{OUT} = 1.2 V, I_{OUT} = 500 mA, T_J = 25°C [1]	1300	1650	2000	kHz
		V_{IN} = 5 V, V_{OUT} = 1.2 V, I_{OUT} = 500 mA, T_J = -40°C to 125°C [1]	1230	1650	2070	kHz
$T_{MIN\text{-}OFF}$	Minimum off time			60		ns
$T_{MIN\text{-}ON}$	Minimum on time[1]			60		ns
$T_{SS\text{-}ON}$	Soft-start time	V_{OUT} rise from 10% to 90%		0.6		ms
	Thermal shutdown[2]			160		°C
	Thermal hysteresis[2]			30		°C
$\triangle V_{OUT}$	Load regulation			1		%/A

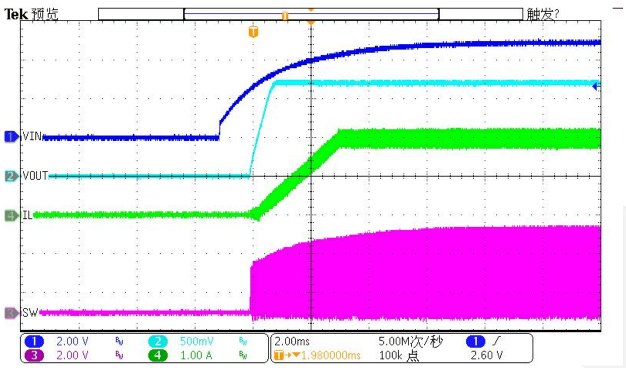
Note:

(1). Guaranteed by characterization.

(2). Guaranteed by design.

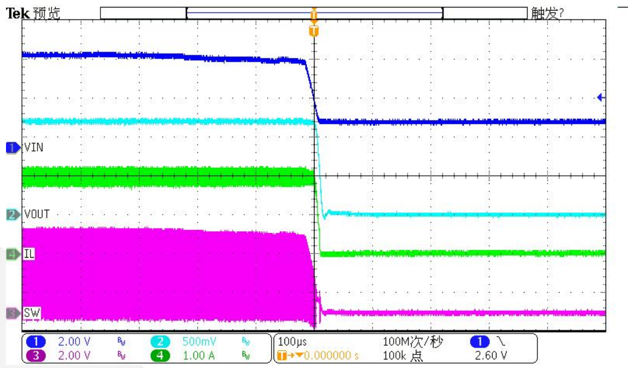
Typical Performance Characteristics

V_{IN} = 5 V, V_{OUT} = 1.2 V, L = 1.0 uH, C_{IN} = C_{OUT} = 10 uF, T_A = 25°C, unless otherwise specified.



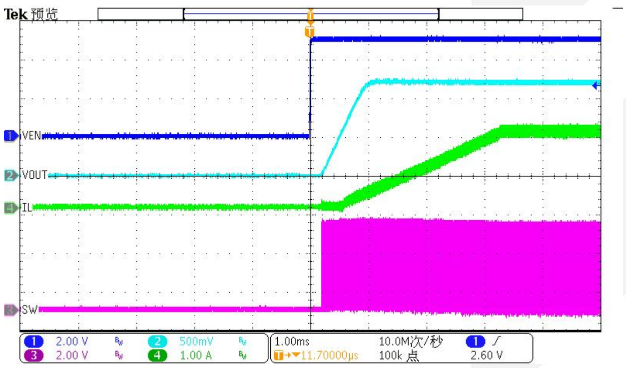
(V_{IN} = 5 V, V_{OUT} = 1.2 V with 2 A load)

Figure 2. V_{IN} start



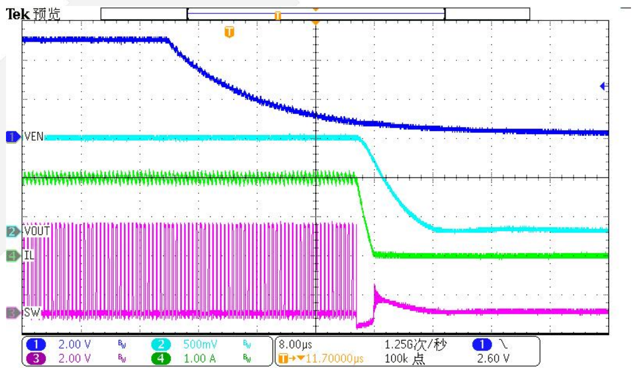
(V_{IN} = 5 V, V_{OUT} = 1.2 V with 2 A load)

Figure 3. V_{IN} drop



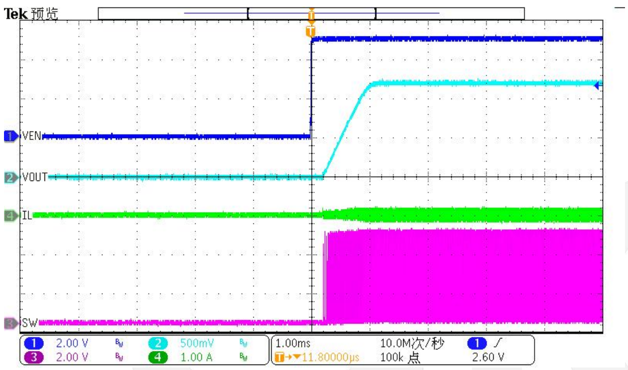
(V_{IN} = 5 V, V_{OUT} = 1.2 V with 2 A load)

Figure 4. V_{EN} start up



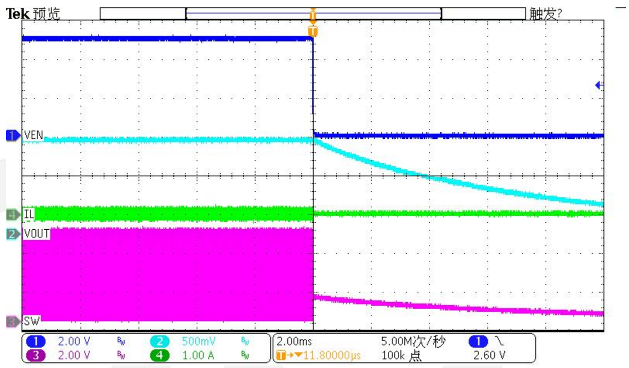
(V_{IN} = 5 V, V_{OUT} = 1.2 V with 2 A load)

Figure 5. V_{EN} drop



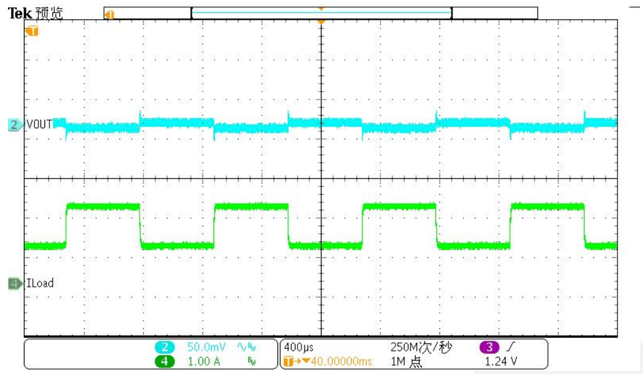
(V_{IN} = 5 V, V_{OUT} = 1.2 V without load)

Figure 6. V_{EN} start up



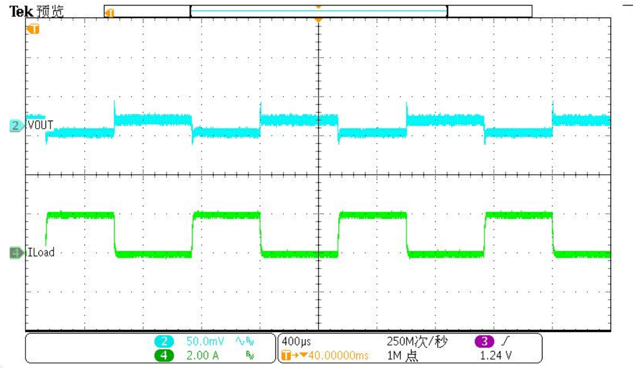
(V_{IN} = 5 V, V_{OUT} = 1.2 V without load)

Figure 7. V_{EN} drop



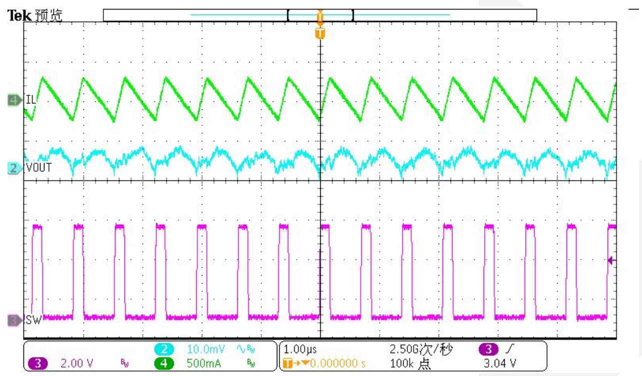
(V$_{IN}$ = 5 V, V$_{OUT}$ = 1.2 V 1 A ~ 2 A)

Figure 8. Load transient



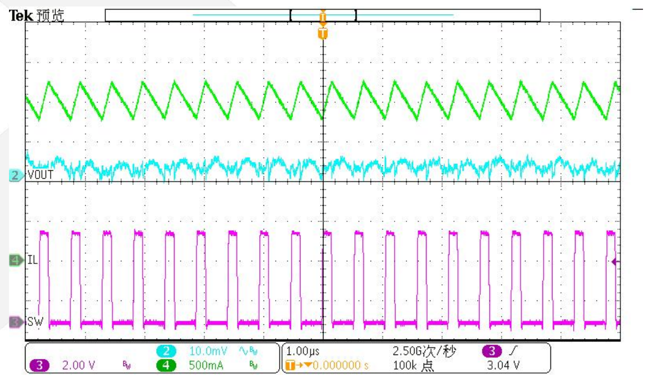
(V$_{IN}$ = 5 V, V$_{OUT}$ = 1.2 V 0 A ~ 2 A)

Figure 9. Load transient



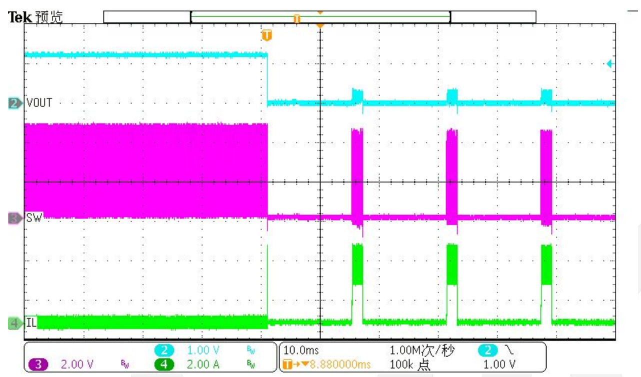
(V$_{IN}$ = 5 V, V$_{OUT}$ = 3.3 V I$_{load}$ = 0 A)

Figure 10. Ripple



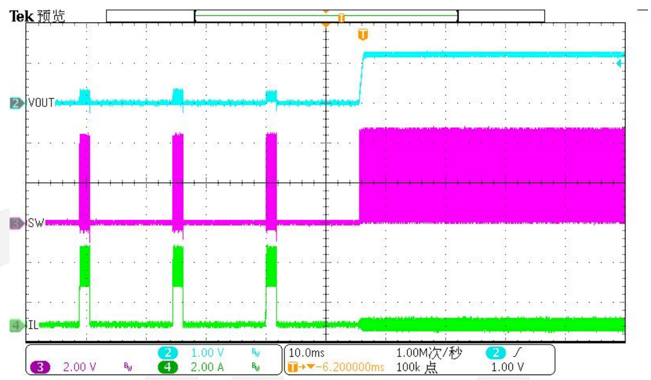
(V$_{IN}$ = 5 V, V$_{OUT}$ = 3.3 V I$_{load}$ = 2 A)

Figure 11. Ripple



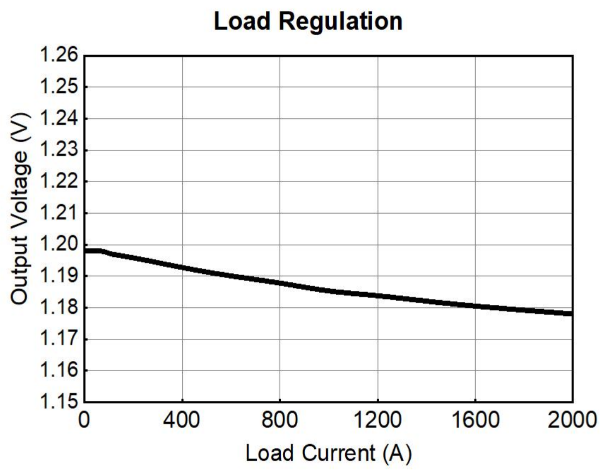
(V$_{IN}$ = 5 V, V$_{OUT}$ = 1.2 V No load -> short)

Figure 12. Short circuit protection



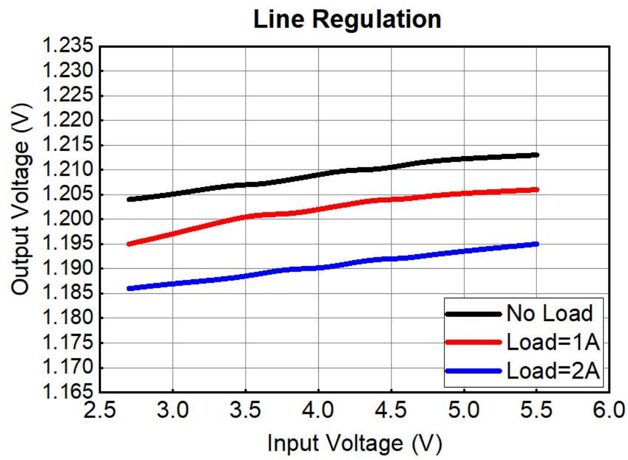
(V$_{IN}$ = 5 V, V$_{OUT}$ = 1.2 V short -> No load)

Figure 13. Short circuit recovery



(V_{IN} = 5 V, V_{OUT} = 1.2 V)

Figure 14.Load regulation



（V_{IN} = 5 V, V_{OUT} = 1.2 V）

Figure 15. Line regulation

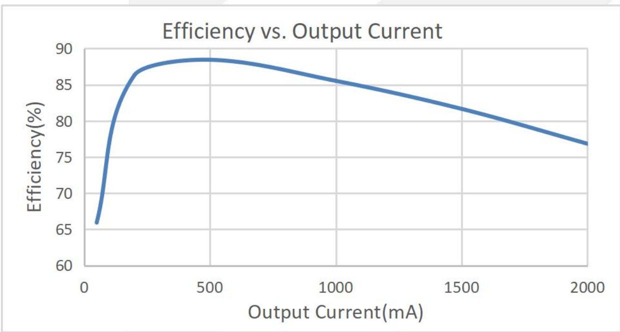


Figure 16. Efficiency vs. Output current

Block Diagram

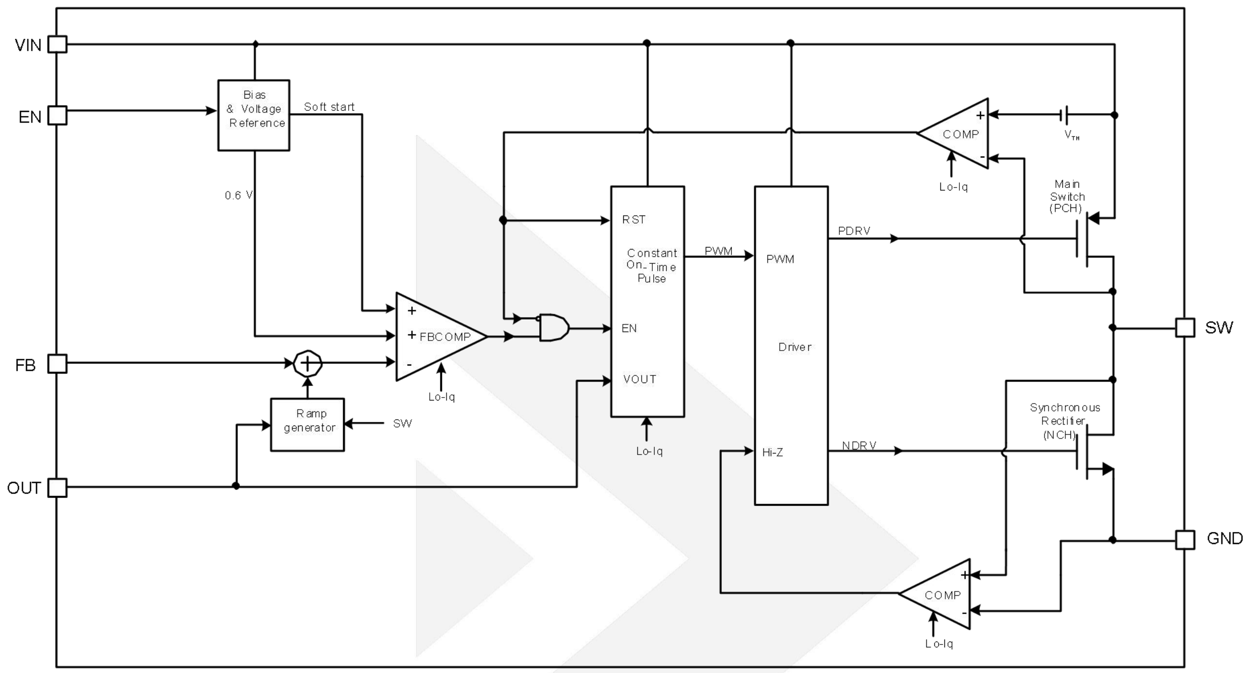


Figure 17. Block diagram

Typical Application

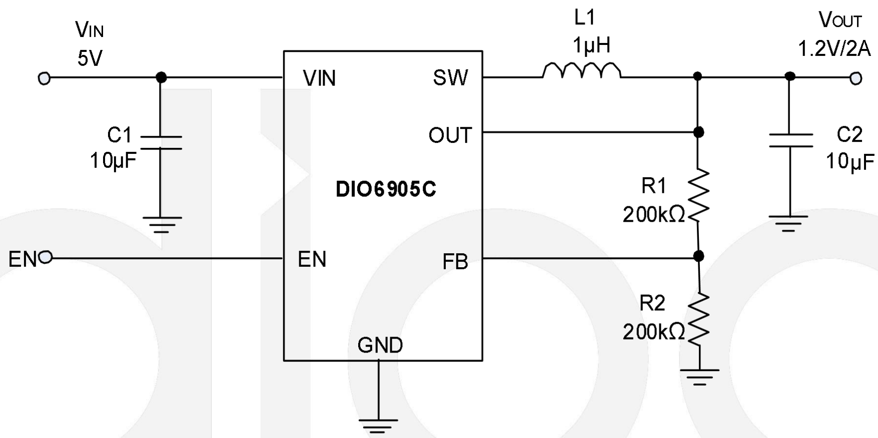


Figure 18. Typical application

Detailed Description

The DIO6905C uses constant on-time control with input voltage feed-forward to stabilize the switching frequency over its full input voltage range. It achieves 2 A of output current from a 2.3 V to 5.5 V input voltage range with excellent load and line regulation. The output voltage can be regulated as low as 0.6 V.

Constant-on-time control

When compared to fixed-frequency PWM control, COT control offers a simpler control loop and faster transient response. By using input voltage feed-forward, the DIO6905C maintains a nearly constant switching frequency across the input and output voltage ranges. The switching pulse on time can be estimated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} * 0.606us \qquad (1)$$

To prevent inductor current runaway during the load transient, the DIO6905C has a fixed minimum off time of 60 ns.

Enable (EN)

When the input voltage is greater than the under-voltage lockout (UVLO) threshold (typically 2.1 V), the DIO6905C can be enabled by pulling EN higher than 1.2 V. Leaving EN floating or pulling it down to ground disables the DIO6905C. There is an internal 1 MΩ resistor from EN to ground.

When the DIO6905C is disabled, the part goes into output discharge mode automatically. The internal discharge MOSFET provides a resistive discharge path for the output capacitor.

Soft-start

The DIO6905C has a built-in soft-start that ramps up the output voltage at a constant slew rate that avoids overshooting at startup. The soft- start time is typically about 0.6 ms.

Current limit

The DIO6905C has the 2.4 A current limit for the HS-FET. When the HS-FET hits its current limit, the DIO6905C enters current limit mode until the current drops to prevent the inductor current from rising and possibly damaging the components.

Short circuit protection and recovery

The DIO6905C enters short-circuit protection (SCP) mode when it reaches the current limit and attempts to recover from the short circuit by entering hiccup mode. In SCP, the DIO6905C disables the output power stage, discharges the soft-start capacitor, and then enacts a soft-start procedure. If the short-circuit condition still holds after the soft start ends, the DIO6905C repeats this cycle until the short circuit disappears and the output rises back to regulation levels.

Application Information

Setting the output voltage

The external resistor divider sets the output voltage. Select the feedback resistor R1 which reduces the V_{OUT} leakage current, typically between 40 kΩ to 200 kΩ. There is not strict requirement on the feedback resistor. R1 > 10 kΩ is reasoned for most application. R2 can be calculated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6} - 1} \quad (2)$$

The feedback circuit is shown as Figure 19:

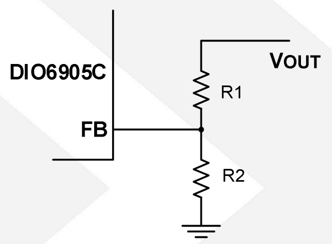


Figure 19. Feedback network

Table 1 lists the recommended resistor's values for common output voltages:

Table 1 Resistor values for common output voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	200(1%)	300(1%)
1.2	200(1%)	200(1%)
1.8	200(1%)	100(1%)
2.5	200(1%)	63.2(1%)
3.3	200(1%)	44.2(1%)

Selecting the inductor

Most applications work best with a 1 μH to 2.2 μH inductor. For highest efficiency, chose an inductor with a DC resistance less than 15 mΩ.

A high-frequency switch-mode power supply with a magnetic device has strong electronic magnetic inference. Any unshielded power inductors should be avoided. Metal alloy or multiplayer chip power inductors are ideal shielded inductors for the application since they can decrease the influence effectively. Table 2 lists some recommended inductors.

Table 2 Recommended inductors

Manufacturer P/N	Inductance (μH)	Manufacturer
PIFE25201B-1R0MS	1.0	CYNTEC CO. LTD.
1239AS-H-1R0M	1.0	Tokyo
744 777 002	2.2	Wurth

For most designs, the inductance value can be estimated with Equation (3):

$$L_1 = \frac{V_{OUT}*(V_{IN} - V_{OUT})}{V_{IN}*\triangle I_L * f_{OSC}} \quad (3)$$

Where ΔI_L is the inductor ripple current.

Choose an inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\triangle I_L}{2} \quad (4)$$

Selecting the input capacitor

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR values and small temperature coefficients. For most applications, a 10 μF capacitor is sufficient. Higher output voltages may require a 22 μF capacitor to increase system stability.

The input capacitor requires an adequate ripple current rating since it absorbs the input switching current. Estimate the RMS current in the input capacitor with Equation (5):

$$I_{C1} = I_{LOAD} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case scenario occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, 0.1 μF ceramic capacitor as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be estimated with Equation (7):

$$\triangle V_{IN} = \frac{I_{LOAD}}{f_S * C1} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

Selecting the output capacitor

The output capacitor (C2) stabilizes the DC output voltage. Ceramic capacitors are recommended. Use low ESR capacitors to limit the output voltage ripple. Estimate the output voltage ripple with Equation (8):

$$\triangle V_{OUT} = \frac{V_{OUT}}{f_S * L_1} * (1 - \frac{V_{OUT}}{V_{IN}}) * (R_{ESR} + \frac{1}{8 * f_S * C2}) \quad (8)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor. When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (9):

$$\triangle V_{OUT} = \frac{V_{OUT}}{8 * f_S^2 * L_1 * C2} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (10):

$$\triangle V_{OUT} = \frac{V_{OUT}}{f_S * L_1} * (1 - \frac{V_{OUT}}{V_{IN}}) * R_{ESR} \quad (10)$$

The characteristics of the output capacitor also affect the stability of the regulation system.

PCB layout recommendation

Efficient PCB layout is critical for stable operation. For the high-frequency switching converter, a poor layout design can result in poor line or load regulation and stability issues. For best results, refer to Figure 20 and follow the guidelines below.

(1) Place the high-current paths (GND, IN, and SW) as close to the device as possible with short, direct, and wide traces.

(2) Keep the input capacitor as close to IN and GND as possible.

(3) Place the external feedback resistors next to FB.

(4) Keep the switching node SW short and away from the feedback network.

(5) Keep the VOUT sense line as short as possible or keep it away from the power inductor and the surrounding inductors.

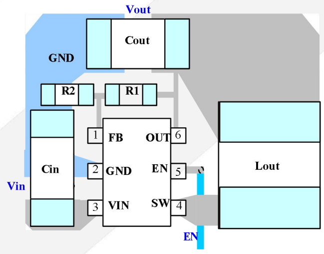
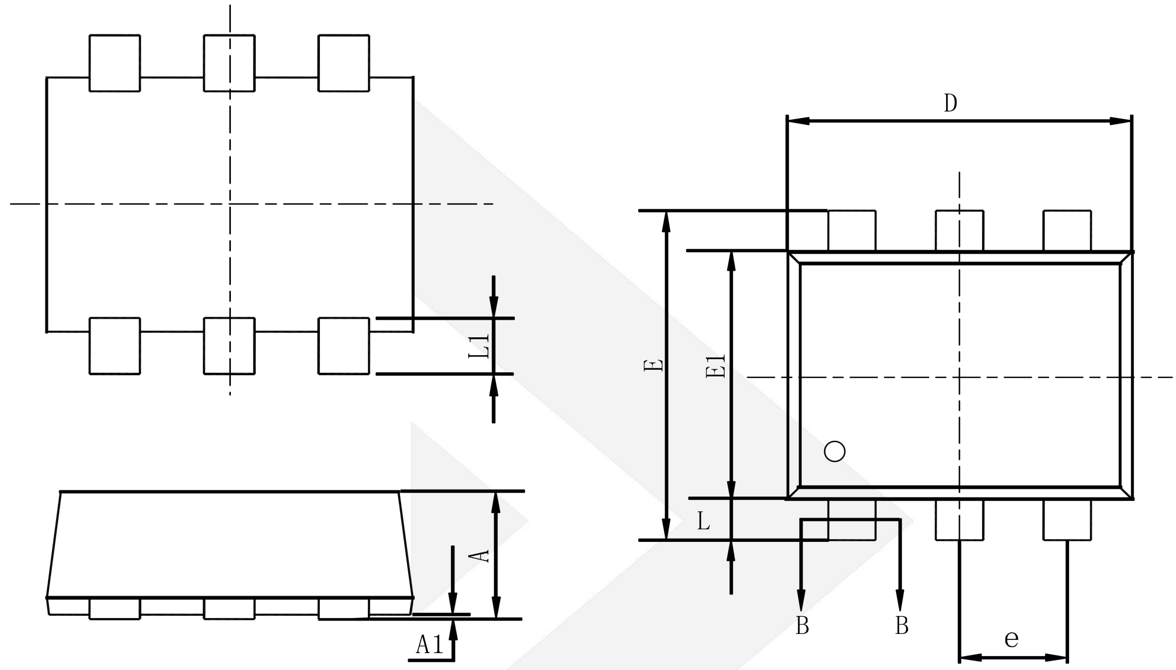
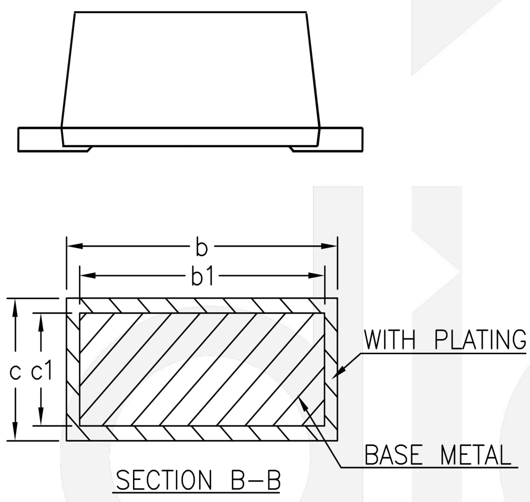


Figure 20. Two ends of input decoupling capacitor close to pin 2 and pin 3

Physical Dimensions: SOT563





Common Dimensions (Units of Measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.53	-	0.60
A1	0.00	-	0.05
b	0.19	-	0.27
b1	0.18	0.20	0.23
c	0.11	-	0.16
c1	0.10	0.11	0.12
D	1.50	1.60	1.70
E	1.50	1.60	1.70
E1	1.10	1.20	1.30
e	0.50 BSC		
L	0.10	0.20	0.30
L1	0.20	0.30	0.40

CONTACT US

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