

DIO6690/N

2A, Synchronous, Step-Down Converter with PFM

Features

- 1.8MHz Switching Frequency
- EN for Power Sequencing
- Wide 3V to 5.5V Operating Input Range
- Output Adjustable from 0.6V
- Up to 2A Output Current
- 120mΩ and 80mΩ Internal Power MOSFET Switches
- PFM Operation
- DIO6690: With Output Discharge
DIO6690N: Without Output Discharge
- Short-Circuit Protection (SCP) with Hiccup Mode
- Stable with Low ESR Output Ceramic Capacitors
- 100% Duty Cycle
- Available in DFN2*1.5-8 Package

Descriptions

The DIO6690/N is a monolithic, step-down, switch-mode converter with built-in, internal power MOSFETs. It achieves 2A of output current from a 3V to 5.5V input voltage with excellent load and line regulation. The output voltage can be regulated as low as 0.6V. DIO6690/N adopts sleep-mode to achieve high efficiency under extremely light load condition.

The constant-on-time control scheme provides a fast transient response and eases loop stabilization. Full protection features include cycle-by-cycle current limiting and thermal shutdown.

The DIO6690/N is available in DFN2*1.5-8 package and requires a minimal number of readily available, standard, external components.

Applications

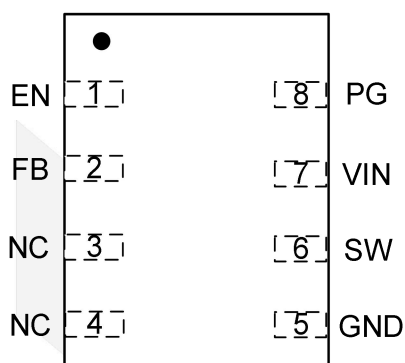
- Wireless/Networking Cards
- Portable and Mobile Devices
- Battery-Powered Devices
- Low-Voltage I/O System Power
- Solid-State Drives (SSDs)

The DIO6690/N is ideal for a wide range of applications, including high-performance DSPs, wireless power, portable and mobile devices, and other low-power systems.

Ordering Information

Order Part Number	Top Marking		T _A	Package	
DIO6690MN8	9VYW	Green	-40 to 85°C	DFN2*1.5-8	Tape & Reel, 3000
DIO6690NMN8	9NYW	Green	-40 to 85°C	DFN2*1.5-8	Tape & Reel, 3000

Pin Assignments



DIO6690MN8 / DIO6690NMN8
DFN2*1.5-8

Figure 1. Pin Assignment (Top View)

Pin Definitions

Pin Name	Description
FB	Feedback. An external resistor divider from the output to GND tapped to FB sets the output voltage.
GND	Power ground.
VIN	Supply voltage. The DIO6690/N operates from a 3V to 5.5V unregulated input. A decoupling capacitor is required to prevent large voltage spikes from appearing at the input.
SW	Output switching node. SW is the drain of the internal high-side P-channel MOSFET. Connect the inductor to SW to complete the converter.
EN	On/off control.
PG	Power good indicator. Power good indicator (open drain output). Low if the output < 90% or the output >120% of regulation voltage; High otherwise. Connect a pull-up resistor to the input.
NC	No connection.

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Rating	Unit
Supply Voltage (V_{IN})	6.0	V
V_{SW}	-0.3 (-5V for <20ns) to 6.0 (8V for <20ns or 10V for <10ns)	V
All Other Pins	-0.3 to 6.0	V
Junction Temperature Range	150	°C
Lead Temperature Range	260	°C
Continuous Power Dissipation ($T_A = 25^{\circ}\text{C}$)	1	W
Storage temperature	-65 to 150	°C

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not recommend exceeding them or designing to Absolute Maximum Ratings.

Parameter	Rating	Unit
Supply Voltage (V_{IN})	3 to 5.5	V
Operating Junction Temperature Range	-40 to 125	°C
Package Thermal Resistance	Θ_{JA}	°C/W
	Θ_{JC}	



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Electrical Characteristics

$V_{IN} = 3.6V$, $T_A = 25^{\circ}C$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{FB}	Feedback voltage	$3V \leq V_{IN} \leq 5.5V$, $T_J = 25^{\circ}C$	594	600	606	mV
I_{FB}	Feedback current	$V_{FB} = 0.63V$		50	100	nA
$R_{DS(on)_P}$	P-FET switch on resistance			120		m Ω
$R_{DS(on)_N}$	N-FET switch on resistance			80		m Ω
I_{LKG_P}	SW pin leakage current (6690N)	$V_{EN} = 0V$, $V_{IN} = 6V$, $V_{SW} = 0V$ and $6V$, $T_J = 25^{\circ}C$		0	5	μA
I_{LIM_P}	P-FET peak current limit	Sourcing	2.4			A
I_{LIM_N}	N-FET valley current limit	Sourcing, valley current limit		1.6		A
T_{ON}	On time	$V_{IN} = 5V$, $V_{OUT} = 1.2V$		133		ns
		$V_{IN} = 3.6V$, $V_{OUT} = 1.2V$		185		
f_s	Switching frequency	$V_{IN} = 5V$, $V_{OUT} = 1.2V$, $I_{OUT} = 500mA$, $T_J = 25^{\circ}C$ ⁽¹⁾	1400	1800	2200	kHz
		$V_{IN} = 5V$, $V_{OUT} = 1.2V$, $I_{OUT} = 500mA$, $T_J = -40^{\circ}C$ to $125^{\circ}C$ ⁽¹⁾	1400	1800	2200	kHz
$T_{MIN-OFF}$	Minimum off time			60		ns
T_{MIN-ON}	Minimum on time ⁽¹⁾			60		ns
T_{SS-ON}	Soft-start time	V_{OUT} rise from 10% to 90%		0.6		ms
V_{UVLO}	Under-voltage lockout threshold rising			2.1	2.3	V
	Under-voltage lockout threshold hysteresis			50		mV
V_{IL}	EN input logic low voltage				0.4	V
V_{IH}	EN input logic high voltage		1.2			V
R_{DIS}	Output discharge resistor	$V_{EN} = 0V$, $V_{OUT} = 1.2V$		1		k Ω
I_{LKG_EN}	EN input current	$V_{EN} = 2V$		2		μA
		$V_{EN} = 0V$		0		μA
I_{SD}	Supply current (shutdown)	$V_{EN} = 0V$, $T_J = 25^{\circ}C$		0.1	1	μA
I_q	Supply current (quiescent)	$V_{EN} = 2V$, $V_{FB} = 0.63V$, $V_{IN} = 3.6V$, $5V$, $T_J = 25^{\circ}C$		30	60	μA
	Thermal shutdown ⁽²⁾			160		$^{\circ}C$
	Thermal hysteresis ⁽²⁾			30		$^{\circ}C$

Note:

(1). Guaranteed by characterization.

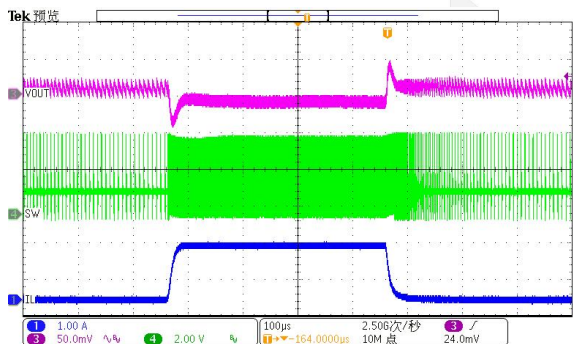
(2). Guaranteed by design.

Typical Performance Characteristics

$V_{IN}=5V$, $V_{OUT}=1.2V$, $L=2.2\mu H$, $C_{IN}=C_{OUT}=10\mu F$, $T_A=25^\circ C$, unless otherwise specified.

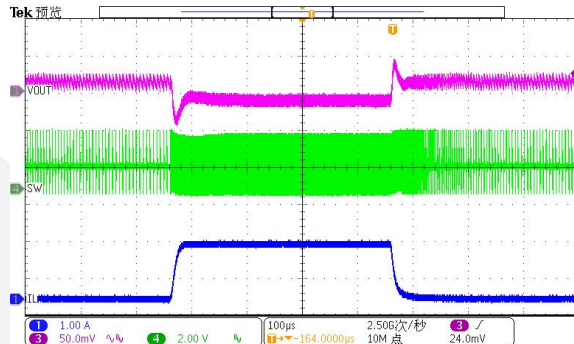
Load Transient

$V_{IN}=5V, V_{OUT}=1.2V, \text{LOAD}=10mA-1.5A$



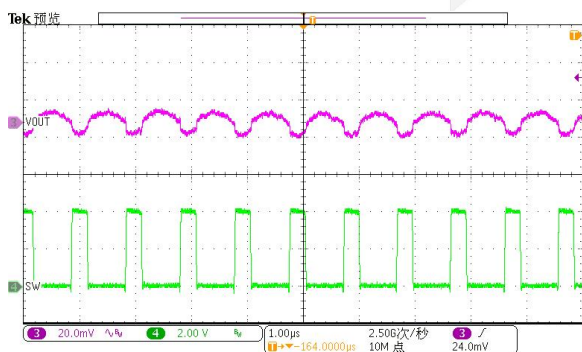
Load Transient

$V_{IN}=3.5V, V_{OUT}=1.2V, \text{LOAD}=10mA-1.5A$



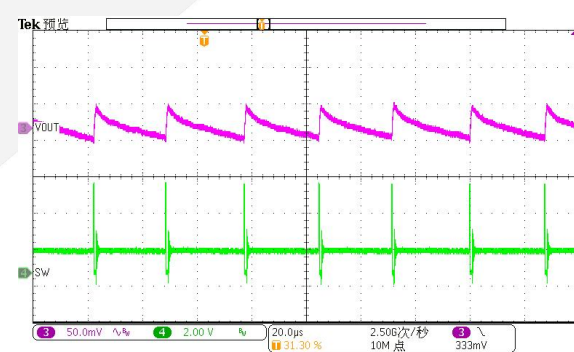
Ripple

$V_{IN}=5V, V_{OUT}=1.2V, \text{LOAD}=2A$



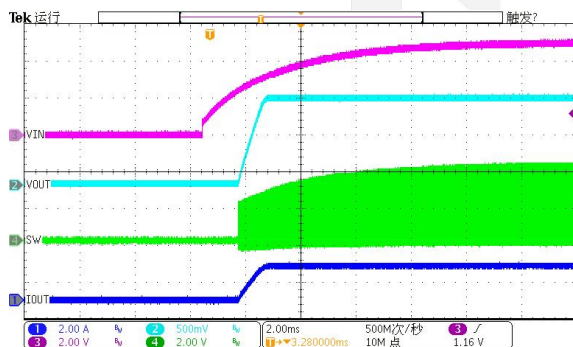
Ripple

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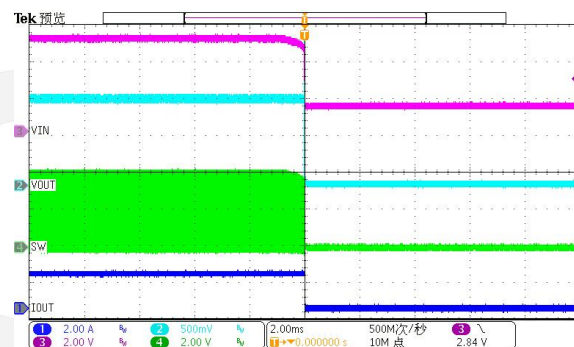
VIN Power on

$V_{IN}=5V, V_{OUT}=1.2V, \text{LOAD}=2A$

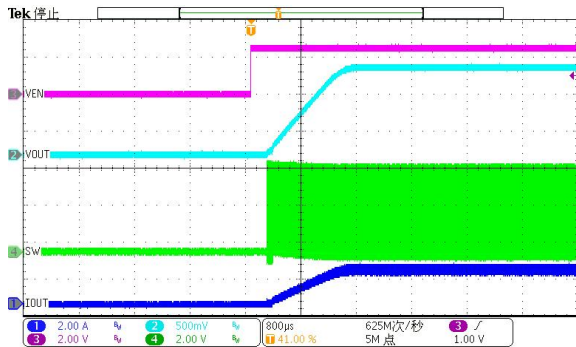


VIN Power off

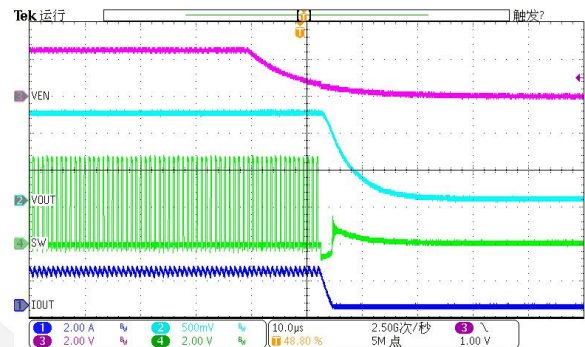
$V_{IN}=5V, V_{OUT}=1.2V, \text{LOAD}=2A$



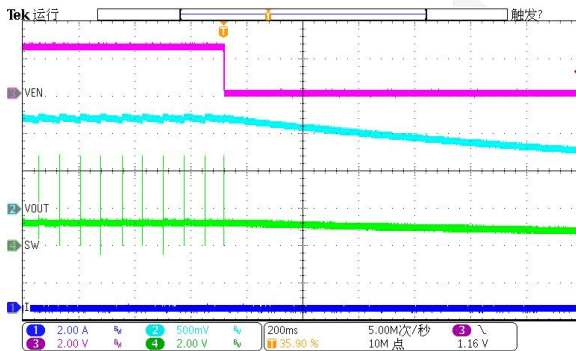
EN Power on
VIN=5V,VOUT=1.2V,LOAD=2A



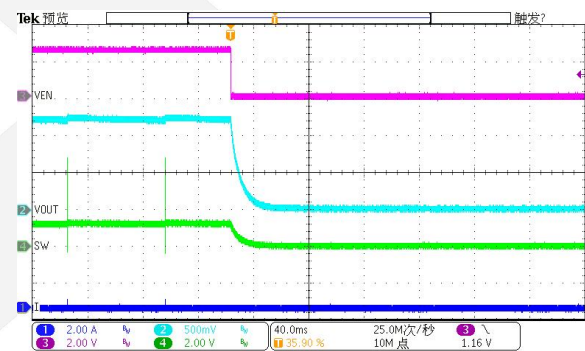
EN Power off
VIN=5V,VOUT=1.2V,LOAD=2A



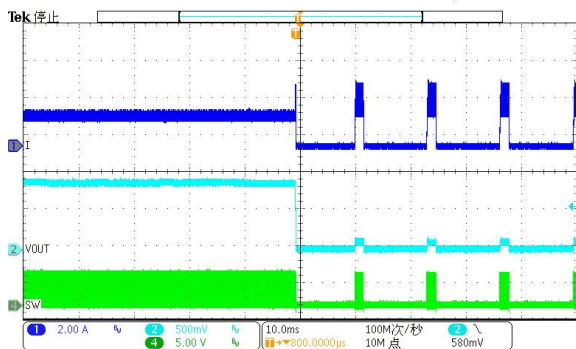
DIO6690N EN Power off
VIN=5V,VOUT=1.2V,NO LOAD



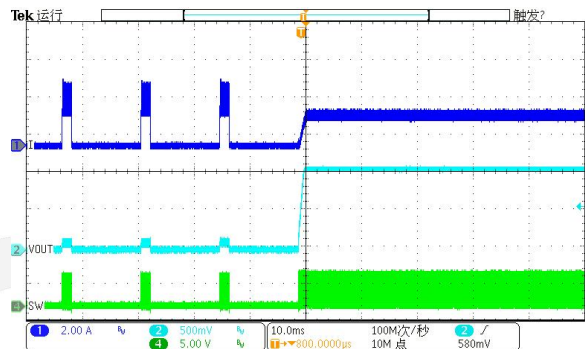
DIO6690 EN Power off
VIN=5V,VOUT=1.2V,NO LOAD

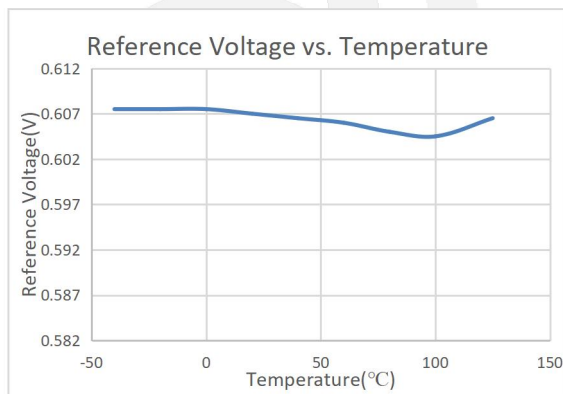
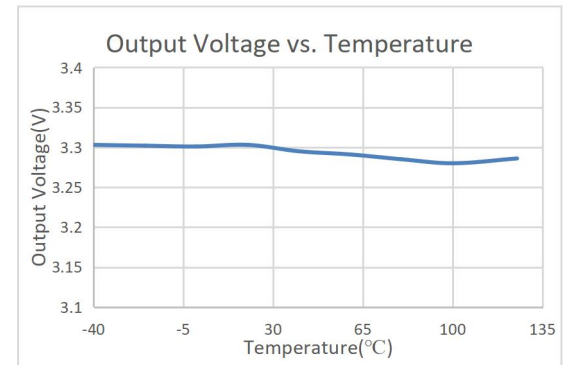
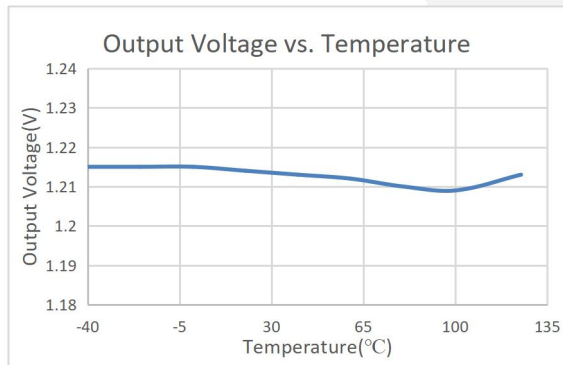
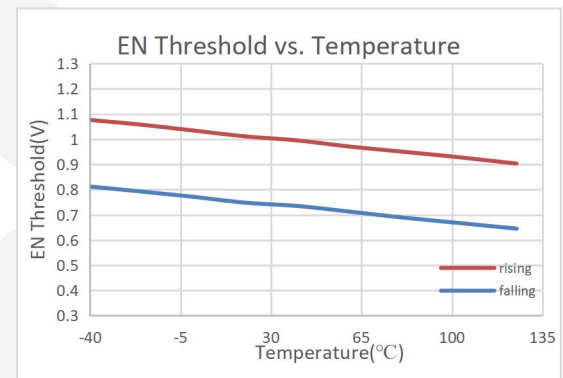
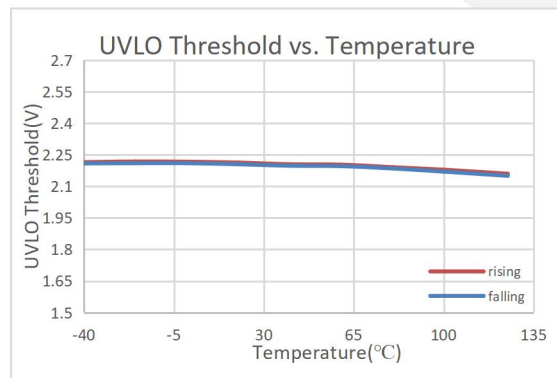
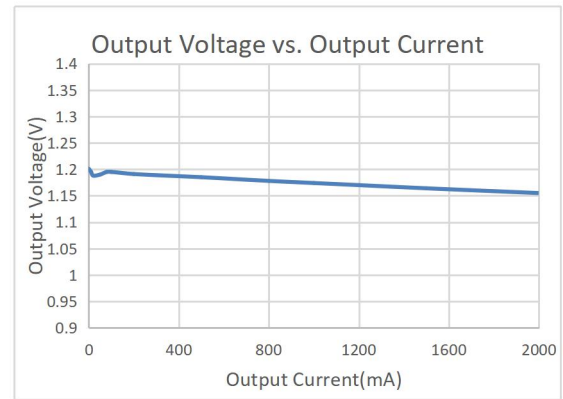
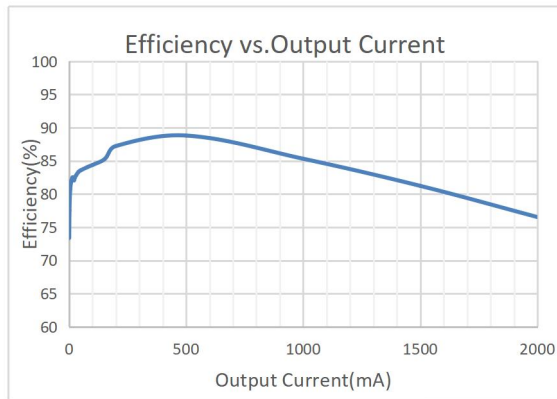


Short Circuit Protection
VIN=5V,VOUT=1.2V,LOAD=2A



Short Circuit Recovery
VIN=5V,VOUT=1.2V,LOAD=2A





The block diagram illustrates the control system for the UCC28950 synchronous buck converter. Key components and their interconnections include:

- Inputs:** VIN (input voltage), EN (enable), FB (feedback), IN (inductor current sense), and PG (power good).
- Control Blocks:**
 - Bias & Voltage Reference:** Provides a 0.6V reference and soft start signal.
 - + E. A. (Error Amplifier):** Receives VIN and FB inputs, with a feedback loop (Lo-Iq) and a 0.6V reference.
 - + FB COMP (Feedback Compensation):** Receives the output of the error amplifier and the FB input, with a feedback loop (Lo-Iq).
 - Ramp generator:** Receives the SW signal and provides a ramp to the FB COMP block.
 - COMP (Comparator):** Receives the output of the FB COMP block and the FB input, with a feedback loop (Lo-Iq).
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 - COMP (Comparator):** Receives the output of the FB COMP block and the FB input, with a feedback loop (Lo-Iq).
- Driver and Switching:**
 - Driver:** Receives the output of the FB COMP block and provides a PWM signal to the Main Switch (PCH) and the Synchronous Rectifier (NCH).
 - Main Switch (PCH):** A MOSFET that switches the input voltage VIN to the load.
 - Synchronous Rectifier (NCH):** A MOSFET that provides a low-resistance path for the inductor current during the off-time.
- Feedback and Protection:**
 - FB (Feedback):** The output voltage is divided by a feedback network (0.6V and 0.54V) and fed back to the FB input.
 - PG (Power Good):** A signal indicating that the output voltage is within regulation.

The diagram shows the DIO6690/N DC-DC converter circuit. The input voltage V_{IN} is 3-5.5V. The input capacitor C_{IN} is 10 μ F/10V. The input resistor R_{PG} is 100k. The output voltage V_{OUT} is 1.8V. The output capacitor C_{OUT} is 22 μ F/6.3V. The feedback network consists of R_1 (200k) and R_2 (100k). The inductor L_1 is 2.2 μ H. The converter is controlled by an ON/OFF signal.

Detailed Description

The DIO6690/N uses constant on-time control with input voltage feed-forward to stabilize the switching frequency over its full input Voltage range. It achieves 2A of output current from a 3V to 5.5V input voltage range with excellent load and line regulation. The output voltage can be regulated as low as 0.6V.

Constant-On-Time Control

Constant-on-time control offers a simpler control loop and faster transient response. By using input voltage feed-forward, the DIO6690/N maintains a nearly constant switching frequency across the input and output voltage ranges. The switching pulse on time can be estimated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} * 0.556\mu s \quad (1)$$

To prevent inductor current runaway during the load transient, the DIO6690/N has a fixed minimum off time of 60ns.

Sleep Mode Operation

DIO6690/N adopts sleep-mode to achieve high efficiency under extremely light load condition. In such sleep-mode, most of the circuitry is turned off, except the EA (error amplifier) and the PWM comparator, which results in minimum operation current as shown in Figure 2.

When the loading gets lighter, the ripple of the output voltage is bigger, DIO6690/N enters sleep mode. Under sleep-mode situation, the valley of the FB pin voltage is regulated to the internal reference voltage. Therefore, the average output voltage is slightly higher than the output voltage in DCM or CCM. The on-time pulse at sleep mode is around 40% larger than that on DCM or CCM mode. Figure 3 shows the average FB pin voltage relationship with the internal reference at sleep mode.

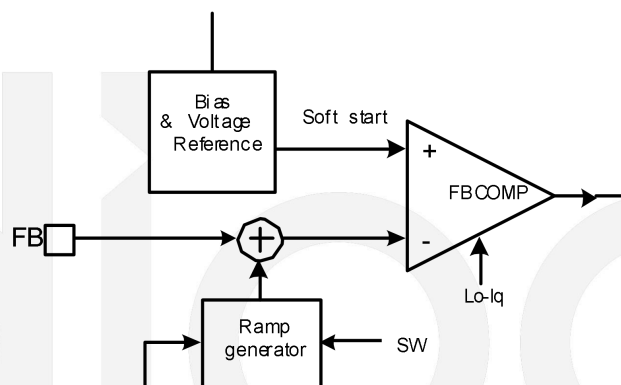


Figure 2. Operation Blocks at Sleep Mode

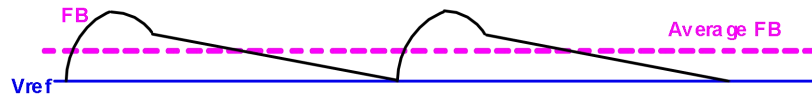


Figure 3. FB Average Voltage at Sleep Mode

When DIO6690/N is in sleep mode, the average output voltage is higher than the internal reference voltage. The EAO is kept low and clamped in sleep mode. When the loading increases, the PWM switching period decreases to keep the output voltage regulated and the output voltage ripple decreases relatively. Once EAO is more than internal low threshold, DIO6690/N will be out of sleep mode and enter DCM or CCM mode depending on the loading. In DCM or CCM mode, the EA regulates the average output voltage to the internal reference which is shown in Figure 4.

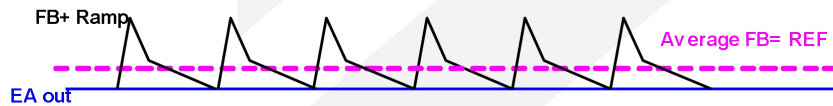


Figure 4. DCM Mode Control

There is always a loading hysteresis of entering sleep mode and leaving sleep mode due to the error amplifier clamping response time.

Operation at Light-Load Operation

The DIO6690/N uses advanced asynchronous modulation power-save mode with zero current cross detection (ZCD) circuit for light load.

The DIO6690/N uses advanced asynchronous modulation power-save mode for light load. The simplified advanced asynchronous modulation control theory is shown in Figure 5. The advanced asynchronous modulation current (I_{AAM}) is set internally. The SW on pulse time is determined by the on-time generator and advanced asynchronous modulation comparator. At light-load condition, the SW on pulse time is longer. If the advanced asynchronous modulation comparator pulse is longer than the on-time generator, the operation mode is as shown in Figure 6.

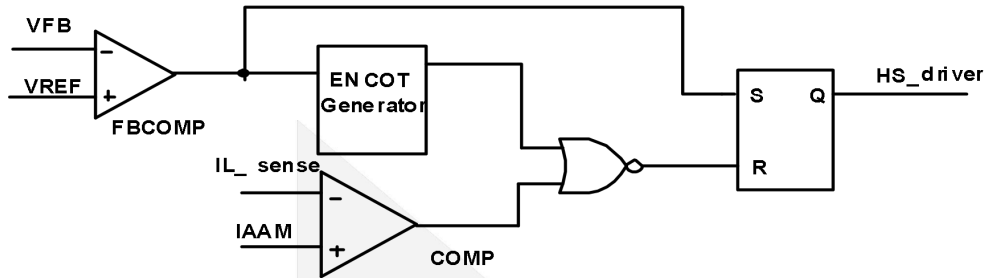


Figure 5. Simplified Advanced Asynchronous Modulation Control Logic

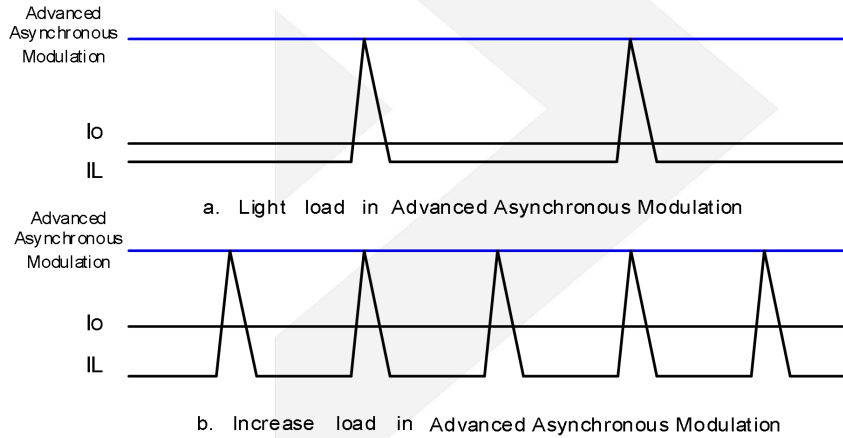


Figure 6. Advanced Asynchronous Modulation Comparator Control T_{ON}

If the advanced asynchronous modulation comparator pulse is shorter than the on-time generator, the operation mode is as shown in Figure 7. This usually occurs when using a very small inductance.

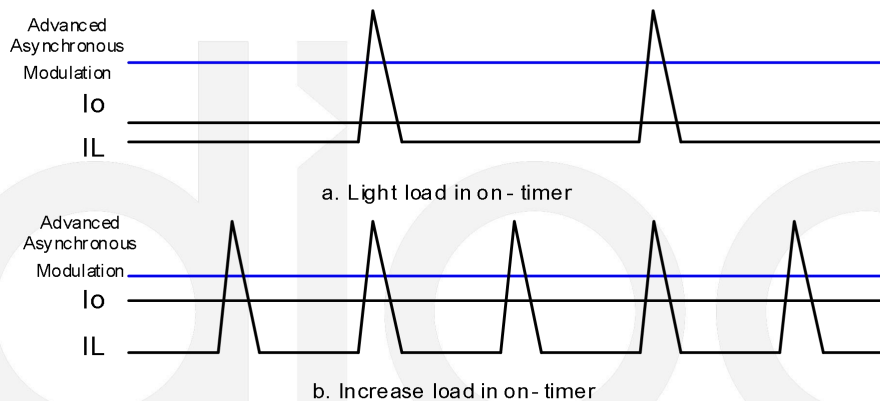


Figure 7. On-Timer Control T_{ON}

The advanced asynchronous modulation circuit has another 150ns of advanced asynchronous modulation blank time in sleep mode. If the on-timer is less than 150ns, the high-side MOSFET may turn off after the on-time generator pulse without advanced asynchronous modulation control. The on-time pulse at sleep mode is about 40% larger than in DCM or CCM. In this condition, I_L may not reach the advanced asynchronous modulation threshold (see Figure 8).

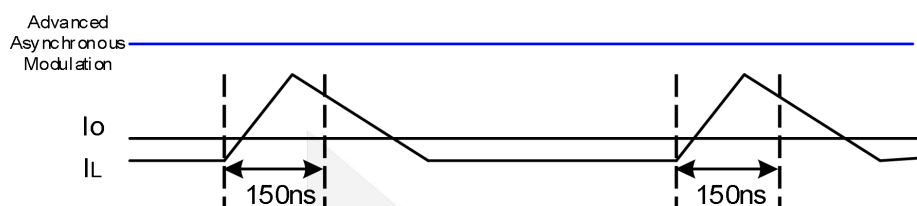


Figure 8. Advanced Asynchronous Modulation Blank Time in Sleep Mode

The advanced asynchronous modulation threshold decreases as T_{ON} increases (see Figure 9). For CCM state, I_{OUT} requires more than half of the advanced asynchronous modulation threshold.

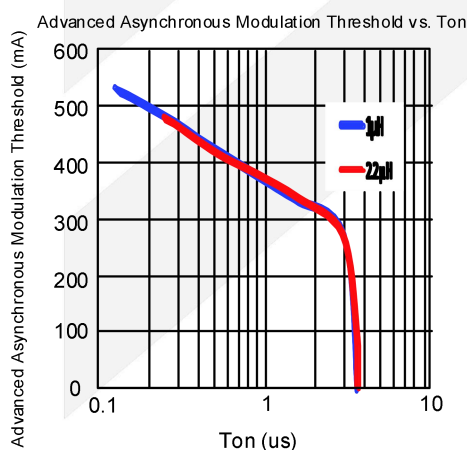


Figure 9. Advanced Asynchronous Modulation Threshold Decreases as T_{ON} Increases

The DIO6690/N uses a zero current cross detect circuit (ZCD) to determine when the inductor current begins reversing. When the inductor current reaches the ZCD threshold, the low-side switch is turned off.

advanced asynchronous modulation mode with the ZCD circuit makes the DIO6690/N work continuously in DCM at light load, even if V_{OUT} is close to V_{IN} .

Enable (EN)

When the input voltage is greater than the under-voltage lockout (UVLO) threshold (typically 2.1V), the DIO6690/N can be enabled by pulling EN higher than 1.2V. Leaving EN floating or pulling it down to ground disables the DIO6690/N. There is an internal 1M Ω resistor from EN to ground.

When the DIO6690/N is disabled, the part goes into output discharge mode automatically. The internal discharge MOSFET provides a resistive discharge path for the output capacitor.

Soft-Start

The DIO6690/N uses a built-in soft start (SS) that ramps up the output voltage at a controlled slew rate to avoid overshooting at start-up. The soft- start time is about 0.6ms, typically.



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Current Limit

The DIO6690/N has a 2.4A, minimum, high-side, switch-current limit. When the high-side switch reaches its current limit, the DIO6690/N remains in hiccup mode until the current drops. This prevents the inductor current from continuing to rise and damaging components.

Short Circuit and Recovery

The DIO6690/N enters short-circuit protection (SCP) mode when it reaches the current limit and attempts to recover with hiccup mode. The DIO6690/N disables the output power stage, discharges the soft-start capacitor, and attempts to soft start again automatically. If the short circuit condition remains after the soft start ends, the DIO6690/N repeats this cycle until the short circuit disappears and the output rises back to regulation levels.

Application Information

Setting the Output Voltage

The external resistor divider sets the output voltage. Select the feedback resistor R1 which reduces the V_{OUT} leakage current, typically between 40kΩ to 200kΩ. There is not strict requirement on the feedback resistor. $R1 > 10kΩ$ is reasoned for most application. R2 can be calculated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6} - 1} \quad (2)$$

The feedback circuit is shown as Figure 10:

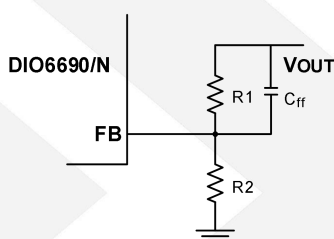


Figure 10. Feedback Network

Table 1 lists the recommended resistor's values for common output voltages:

Table 1 Resistor Values for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L(μH)	C_{OUT} (μF)	C_{ff} (pF)
1.2	200	200	2.2	10	47
1.8	200	100	2.2	10	47
2.5	200	63.2	2.2	10	47
3.3	200	44.2	2.2	10	47
4.2	200	33	2.2	10	47

Selecting the Inductor

Most applications work best with a 1μH to 2.2μH inductor. Select an inductor with a DC resistance less than 15mΩ to optimize efficiency.

A high-frequency switch-mode power supply with a magnetic device has strong electronic magnetic inference. Any unshielded power inductors should be avoided. Metal alloy or multilayer chip power inductors are ideal shielded inductors for the application since they can decrease the influence effectively. Table 2 lists some recommended inductors.

Table 2 Recommended Inductors

Manufacturer P/N	Inductance(μH)	Manufacturer
744 777 002	2.2	Wurth

For most designs, the inductance value can be estimated with Equation (3):

$$L_1 = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * \Delta I_L * f_{OSC}} \quad (3)$$

Where ΔI_L is the inductor ripple current.

Choose an inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR values and small temperature coefficients. For most applications, a 10 μ F capacitor is sufficient. Higher output voltages may require a 22 μ F capacitor to increase system stability.

The input capacitor requires an adequate ripple current rating since it absorbs the input switching current. Estimate the RMS current in the input capacitor with Equation (5):

$$I_{C1} = I_{LOAD} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case scenario occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, 0.1 μ F ceramic capacitor as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S * C1} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

Selecting the Output Capacitor

The output capacitor stabilizes the DC output voltage. Ceramic capacitors are recommended. Use low ESR capacitors to limit the output voltage ripple. Estimate the output voltage ripple with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S * L_1} * (1 - \frac{V_{OUT}}{V_{IN}}) * (R_{ESR} + \frac{1}{8 * f_S * C2}) \quad (8)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor. When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 * f_s^2 * L_1 * C_2} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s * L_1} * (1 - \frac{V_{OUT}}{V_{IN}}) * R_{ESR} \quad (10)$$

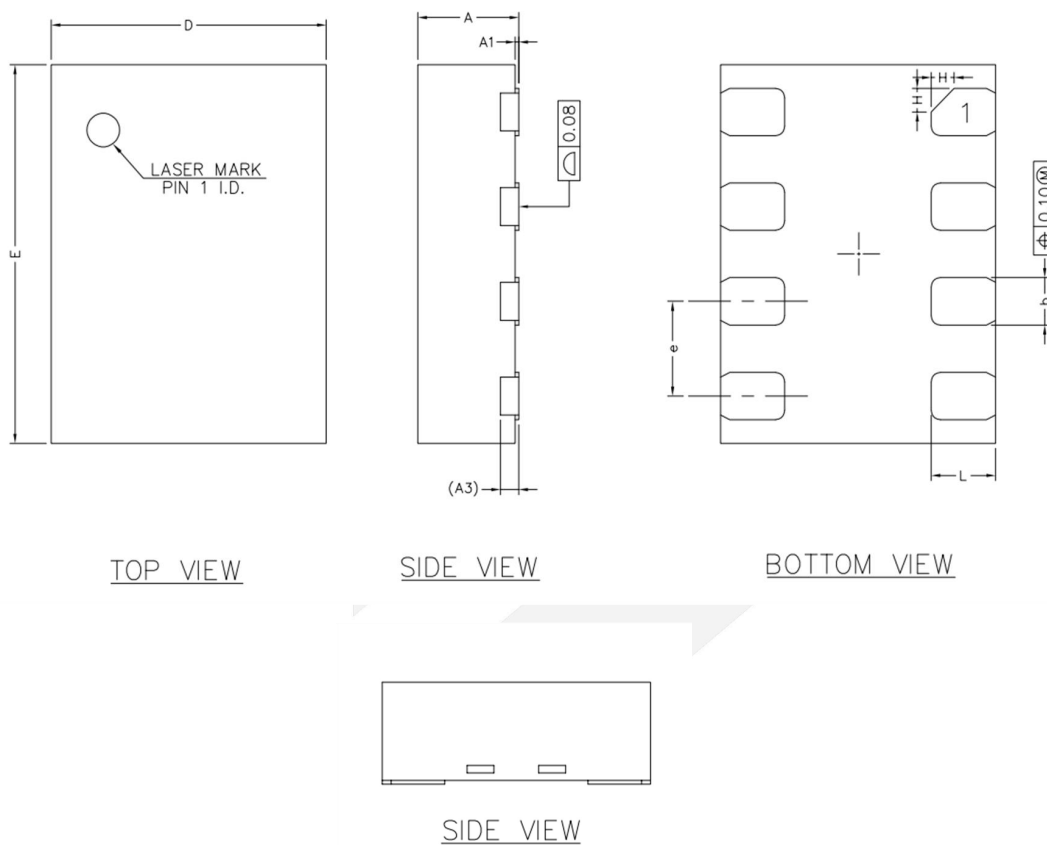
The characteristics of the output capacitor also affect the stability of the regulation system.

PCB Layout Recommendation

Efficient PCB layout is critical for stable operation. For the high-frequency switching converter, a poor layout design can result in poor line or load regulation and stability issues.

- (1) Place the high-current paths (GND, IN, and SW) as close to the device as possible with short, direct, and wide traces.
- (2) Keep the input capacitor as close to IN and GND as possible.
- (3) Place the external feedback resistors next to FB.
- (4) Keep the switching node SW short and away from the feedback network.

Physical Dimensions: DFN2*1.5-8



Symbol	Dimensions in Millimeters		
	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	0.100REF		
b	0.20	0.25	0.30
D	1.40	1.50	1.60
E	1.90	2.00	2.10
e	0.40	0.50	0.60
L	0.30	0.35	0.40
H	0.125REF		



DIO6690/N

2A, Synchronous, Step-Down Converter with PFM

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