DIO7939
Ultra-Low Dropout, CMOS, Bias Rail 1.5 A LDO Regulator

Features

- Operating input voltage range: (V_{OUT} + V_{DO}) to 4 V
- Operating bias voltage range: 2.5 V to 5.5 V
- Adjustable and fixed voltage version available
- Output voltage range:
  0.4 V to 1.8 V (fixed voltage version)
  0.5 V to 3.3 V (adjustable voltage version)
- ±1% accuracy at 25°C
- Ultra−low dropout voltage:
  43 mV (Typ.) at 1.5 A (WLCSP-6)
  110 mV (Typ.) at 1.5 A (DFN2*2-6)
- Very low bias input current of 50 μA (Typ.)
- Very low bias input current in disable mode:
  0.5 μA (Typ.)
- Logic level enable input for ON/OFF control
- Quick output discharge resistance:
  150 Ω (Typ.)
- Stable with a 10 μF ceramic capacitor
- Available in WLCSP−6 1.2 mm x 0.8 mm,
  0.4 mm pitch and DFN2*2-6 packages
- Pb−free, halogen free/BFR free
- RoHS and green compliant.

Descriptions

The DIO7939 is an ultra low dropout 1.5 A LDO, equipped with NMOS pass transistors and a separate bias supply voltage (V_{BIAS}). The device is suitable for space-constrained, noise-sensitive applications for it provides very stable, accurate output voltage with low noise, noise-sensitive applications.

The DIO7939 features a low I_Q consumption to optimize performance for battery-operated portable applications. The device is available in the WLCSP-6 (1.2 mm x 0.8 mm chip, 0.4 mm pitch) and DFN2*2-6 packages.

Applications

- Battery−powered equipment
- Smartphones
- Tablets
- Cameras
- DVRs, STB and camcorders

Typical Application

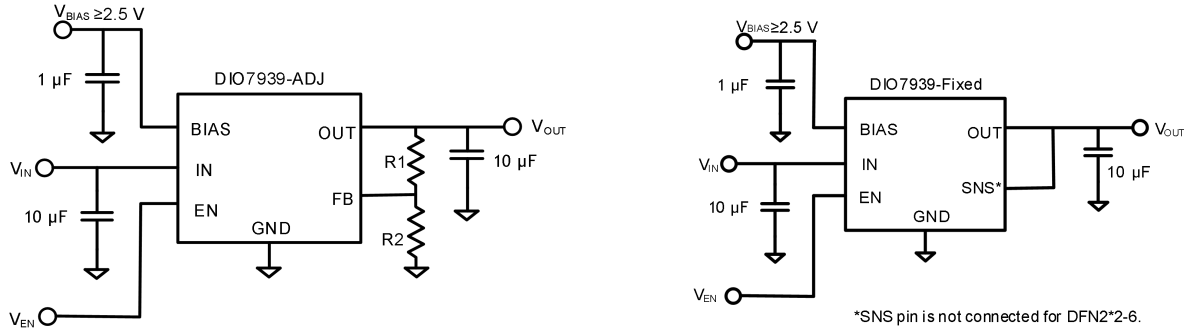
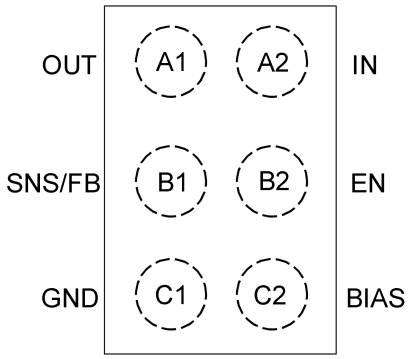


Figure1. Typical application

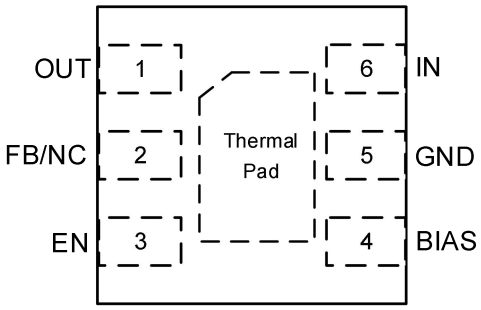
Ordering Information

Ordering Part No.	Top Marking	MSL	RoHS	T_A	Package	
DIO7939A05ADJWL6	CJ5A	1	Green	-40 to 85°C	WLCSP-6	Tape & Reel, 3000
DIO7939A06ADJWL6	CJ6A	1	Green	-40 to 85°C	WLCSP-6	Tape & Reel, 3000
DIO7939A100WL6	CJAV	1	Green	-40 to 85°C	WLCSP-6	Tape & Reel, 3000
DIO7939A105WL6	CJAE	1	Green	-40 to 85°C	WLCSP-6	Tape & Reel, 3000
DIO7939A110WL6	CJAL	1	Green	-40 to 85°C	WLCSP-6	Tape & Reel, 3000
DIO7939A120WL6	CJAM	1	Green	-40 to 85°C	WLCSP-6	Tape & Reel, 3000
DIO7939A180WL6	CJAT	1	Green	-40 to 85°C	WLCSP-6	Tape & Reel, 3000
DIO7939A05ADJCD6	CJ5A	3	Green	-40 to 85°C	DFN2*2-6	Tape & Reel, 3000
DIO7939A06ADJCD6	CJ6A	3	Green	-40 to 85°C	DFN2*2-6	Tape & Reel, 3000
DIO7939A100CD6	CJAV	3	Green	-40 to 85°C	DFN2*2-6	Tape & Reel, 3000
DIO7939A105CD6	CJAE	3	Green	-40 to 85°C	DFN2*2-6	Tape & Reel, 3000
DIO7939A110CD6	CJAL	3	Green	-40 to 85°C	DFN2*2-6	Tape & Reel, 3000
DIO7939A120CD6	CJAM	3	Green	-40 to 85°C	DFN2*2-6	Tape & Reel, 3000
DIO7939A180CD6	CJAT	3	Green	-40 to 85°C	DFN2*2-6	Tape & Reel, 3000

Pin Assignment



WLCSP-6



DFN2*2-6

Figure 2. Pin assignment (Top view)

Pin Descriptions

Pin Name	Description
OUT	Regulated output voltage pin.
IN	Input voltage supply pin.
FB	Adjustable regulator feedback input. Connect to output voltage resistor divider central node.
SNS	Output voltage sensing input. Connect to output on the PCB to output the voltage corresponding to the part version.
EN	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode.
GND	Ground pin.
BIAS	Bias voltage supply for internal control circuits. This pin is monitored by an internal under-voltage lockout circuit.
Thermal pad	Recommend to connect to the GND plane for improved thermal performance.
NC	Not connected.

Absolute Maximum Ratings

Stresses beyond those listed under the Absolute Maximum Rating table may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Rating	Unit
V_{IN}	Input voltage	−0.3 to 5	V
V_{OUT}	Output voltage	−0.3 to (V_{IN} + 0.3) ≤ 5	V
V_{EN}, V_{BIAS}, V_{FB}, V_{SNS}	EN, BIAS, FB and SNS input	−0.3 to 5.5	V
t_{SC}	Output short circuit duration	unlimited	s
T_J	Maximum junction temperature	150	ºC
T_{STG}	Storage temperature	−55 to 150	ºC
ESD	Human body model	±2000	V
	Charged device model	±2000	V
$R_{\theta JA}$	Thermal resistance, Junction−to−air	69	°C/W

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating	Unit
V_{IN}	Operating input voltage range	V_{OUT} + V_{DO} to 4	V
V_{BIAS}	Operating bias voltage range	2.5 to 5.5	V
T_A	Operating free-air temperature	-40 to 85	°C

Electrical Characteristics

V_{BIAS} = 2.5 V or (V_{OUT} + 1.6 V), whichever is higher, V_{IN} = $V_{OUT(NOM)}$ +0.3 V, I_{OUT} = 1 mA, V_{EN} = 1 V, C_{IN} = 10 µF, C_{OUT} = 10 µF, C_{BIAS} = 1 µF, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operating input voltage range		V_{OUT} + V_{DO}		4	V
V_{BIAS}	Operating bias voltage range		(V_{OUT} + 1.60) ≥ 2.5		5.5	V
V_{UVLO}	UVLO threshold			1.8		V
	UVLO hysteresis			0.2		V
V_{REF}	Reference voltage (adjustable voltage version)	DIO7939A05ADJWL6		0.5		V
		DIO7939A06ADJWL6		0.6		
V_{OUT}	Output voltage accuracy	I_L = 1 mA, $V_{OUT(NOM)}$ < 1.0 V	-10		10	mV
		I_L = 1 mA, $V_{OUT(NOM)}$ ≥ 1.0 V	-1		1	%
$Line_{Reg}$	V_{IN} line regulation	$V_{OUT(NOM)}$ + 0.3 V ≤ V_{IN} ≤ 4.0 V		0.01		%/V
	V_{BIAS} line regulation	2.5 V or ($V_{OUT(NOM)}$ + 1.6 V), whichever is higher < V_{BIAS} < 5.5 V		0.01		%/V
$Load_{Reg}$	Load regulation	I_{OUT} = 1 mA to 1.5 A		2		mV
V_{DO}	V_{IN} dropout voltage (WLCSP-6)	I_{OUT} = 1.5 A (1), V_{BIAS} = 3 V, V_{OUT} = 0.5 V		43	80	mV
	V_{BIAS} dropout voltage (WLCSP-6)	I_{OUT} = 1.5 A, V_{IN} = V_{BIAS} (1, 2, 3)		1		V
	V_{IN} dropout voltage (DFN2*2-6)	I_{OUT} = 1.5 A (1), V_{BIAS} = 3 V, V_{OUT} = 0.8 V		110	120	mV
	V_{BIAS} dropout voltage (DFN2*2-6)	I_{OUT} = 1.5 A, V_{IN} = V_{BIAS} (1, 2, 3)		1		V
I_{CL}	Output current limit	V_{OUT} = 90% $V_{OUT(NOM)}$	1600	2000		mA
I_{SC}	Short-circuit current limit	V_{OUT} = 0	550	600	750	mA
I_{FB}, I_{SNS}	FB/SNS pin operating current			0.1	0.5	µA
I_{BIASQ}	V_{BIAS} pin quiescent current	V_{BIAS} = 2.5 V, I_{OUT} = 0 mA		50	75	µA
$I_{BIAS(DIS)}$	V_{BIAS} pin disable current	V_{EN} ≤ 0.4 V		0.5	1	µA
$I_{IN(DIS)}$	IN pin disable current	V_{EN} ≤ 0.4 V		0.5	1	µA
$V_{EN(H)}$	EN pin threshold voltage	EN input voltage “H”	0.8			V
$V_{EN(L)}$		EN input voltage “L”			0.4	

I_{EN}	EN pull down current	V_{EN} = 5.5 V		0.3	1	μA
t_{ON}	Turn−On time	From assertion of V_{EN} to V_{OUT} = 90% $V_{OUT(NOM)}$. $V_{OUT(NOM)}$ = 1.0 V, C_{OUT} = 10 μF	140	350	750	μs
PSRR (V_{IN})	Power supply rejection ratio (adjustable voltage version)	V_{IN} to V_{OUT}, f = 1 kHz, I_{OUT} = 10 mA, V_{IN} ≥ V_{OUT} +0.5 V, $V_{OUT(NOM)}$ = 0.5 V, C_{OUT} = 10 μF		70		dB
PSRR (V_{BIAS})		V_{BIAS} to V_{OUT}, f = 1 kHz, I_{OUT} = 10 mA, V_{IN} ≥ V_{OUT} +0.5 V, $V_{OUT(NOM)}$ = 0.5 V, C_{OUT} = 10 μF		65		
V_N	Output noise voltage (adjustable voltage version)	V_{IN} = V_{OUT} +0.5 V, f = 10 Hz to 100 kHz, $V_{OUT(NOM)}$ = 1.0 V, C_{OUT} = 10 μF		35 × V_{OUT}/V_{FB}		μV_{RMS}
PSRR (V_{IN})	Power supply rejection ratio (fixed voltage version)	V_{IN} to V_{OUT}, f = 1 kHz, I_{OUT} = 10 mA, V_{IN} ≥ V_{OUT} +0.5 V, $V_{OUT(NOM)}$ = 1.2 V, C_{OUT} = 10 μF		80		dB
PSRR (V_{BIAS})		V_{BIAS} to V_{OUT}, f = 1 kHz, I_{OUT} = 10 mA, V_{IN} ≥ V_{OUT} +0.5 V, $V_{OUT(NOM)}$ = 1.2 V, V_{BIAS} = 4.0 V, C_{OUT} = 10 μF		65		dB
V_N	Output noise voltage (fixed voltage version)	V_{IN} = V_{OUT} +0.5 V, f = 10 Hz to 100 kHz, $V_{OUT(NOM)}$ = 1.0 V, C_{OUT} = 10 μF		40		μV_{RMS}
T_{SD}	Thermal shutdown threshold	Temperature increasing		140		°C
		Temperature decreasing		95		
R_{DIS}	Output discharge pull−down	V_{EN} ≤ 0.4 V, V_{OUT} = 0.5 V		150		Ω

Note：

1. Dropout voltage is characterized when V_{OUT} falls 3% below $V_{OUT(NOM)}$.
2. For the adjustable voltage version, V_{BIAS} dropout voltage tested at $V_{OUT(NOM)}$ = 2 x V_{FB} due to a minimum V_{BIAS} operating voltage of 2.5 V.
3. For fixed voltages below 1.8 V, V_{BIAS} dropout voltage does not apply due to a minimum bias operating voltage of 2.5 V.
4. Specification subject to change without notice.

Typical Characteristics

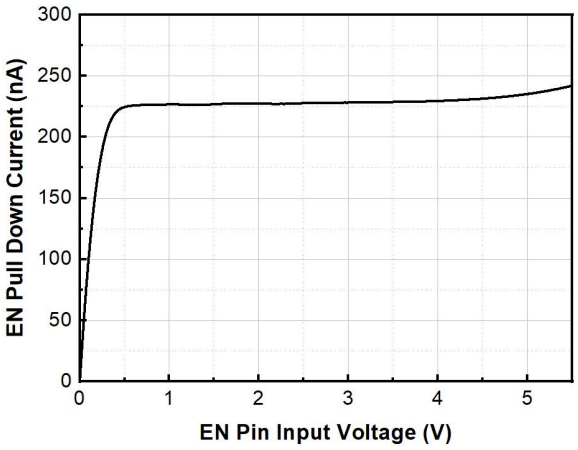


Figure 3. I_{EN} vs. Input voltage

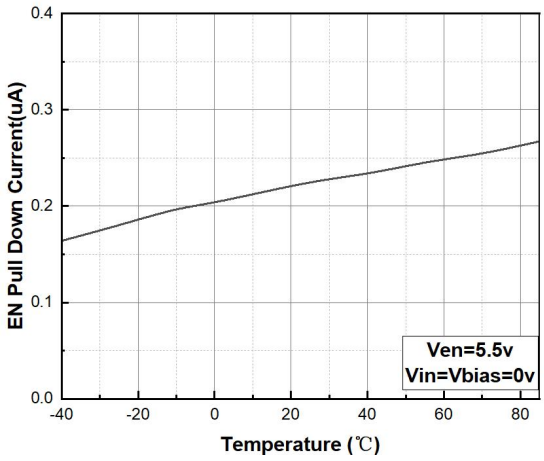


Figure 4. I_{EN} vs. Temp

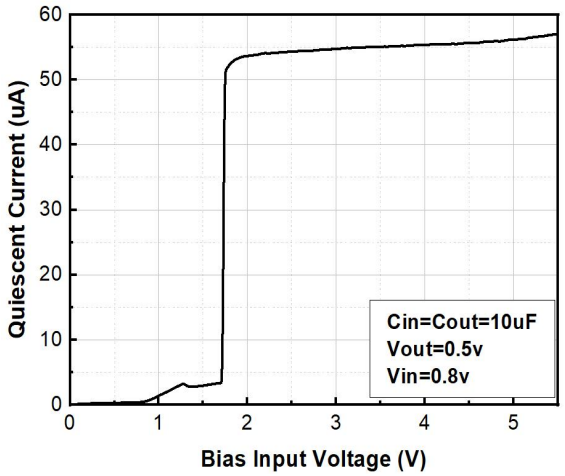


Figure 5. I_{BIASQ} vs. Bias input voltage

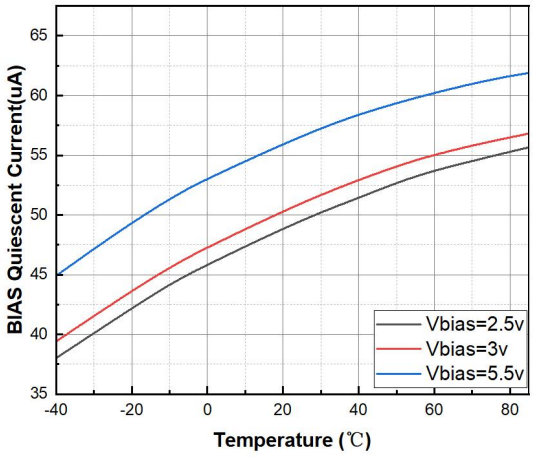


Figure 6. I_{BIASQ} vs. Temp

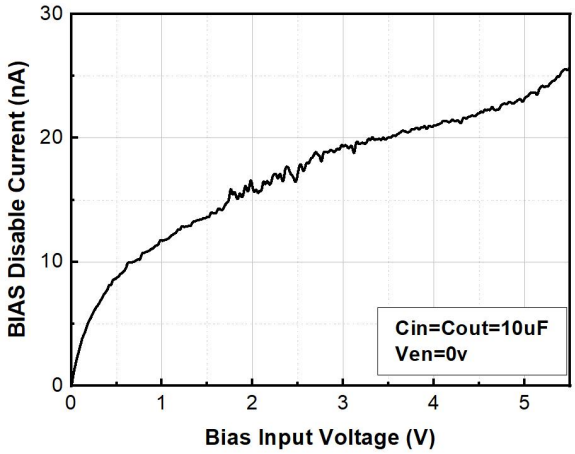


Figure 7. $I_{BIAS(DIS)}$ vs. Input voltage

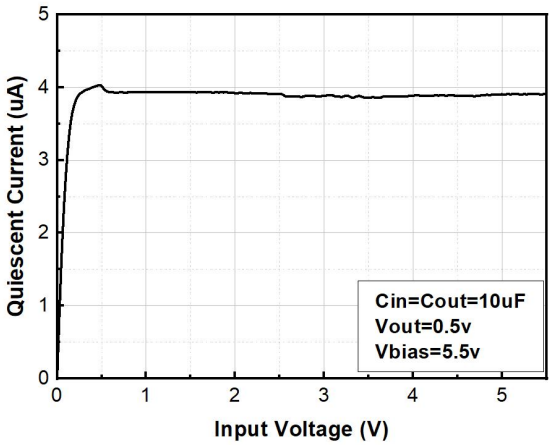


Figure 8. $I_{Q(IN)}$ vs. Input voltage

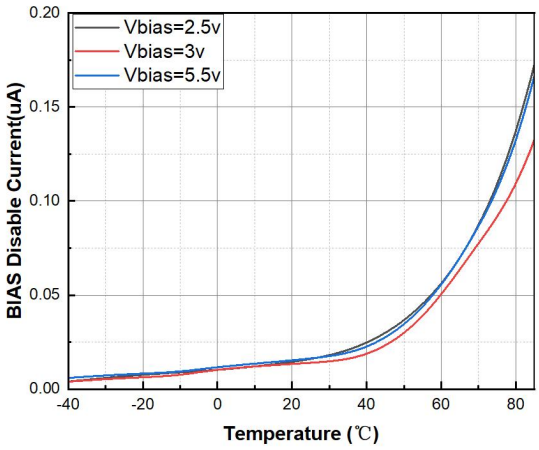


Figure 9. $I_{BIAS(DIS)}$ vs. Temp

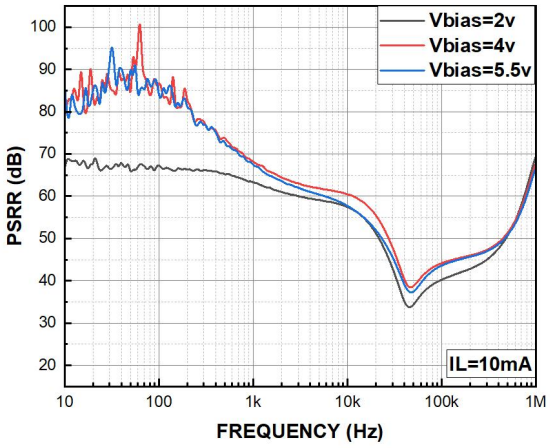


Figure 10. PSRR vs. V_{BIAS}

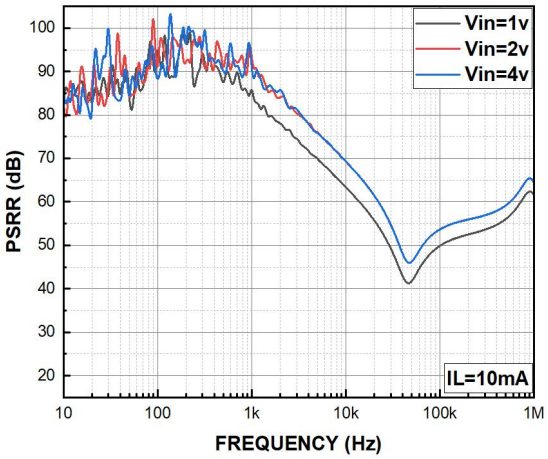


Figure 11. PSRR vs. V_{IN}

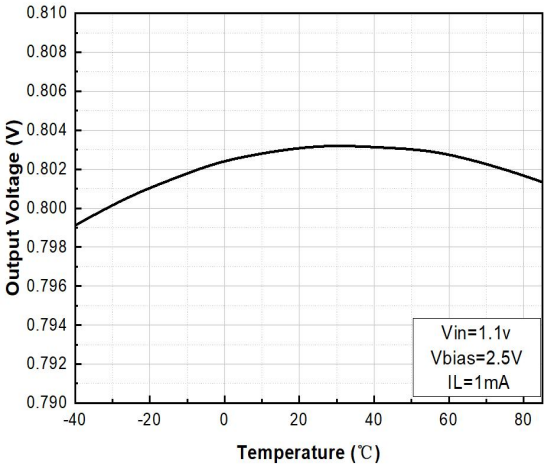


Figure 12. V_{OUT} vs. Temp

Block Diagram

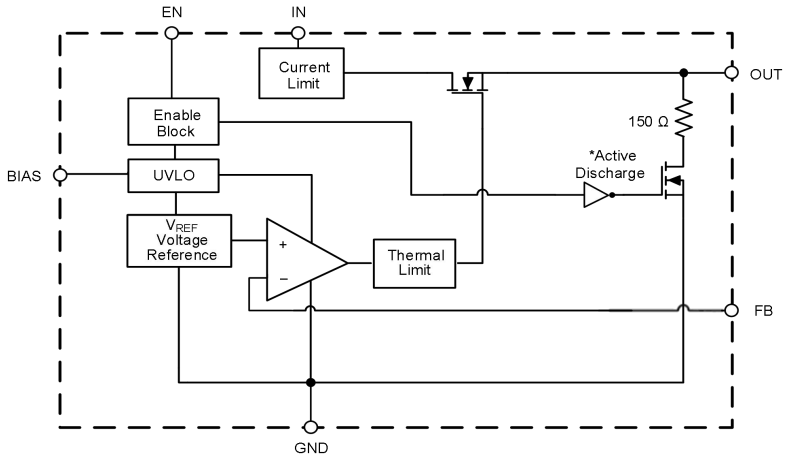


Figure 13. Block diagram − adjustable voltage version

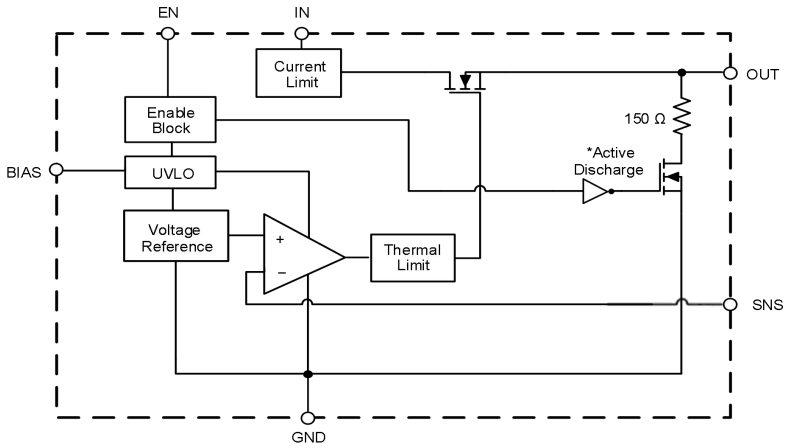


Figure 14. Block diagram − fixed voltage version

Note: (1) SNS pin is not connected for DFN2*2-6.

Typical Application

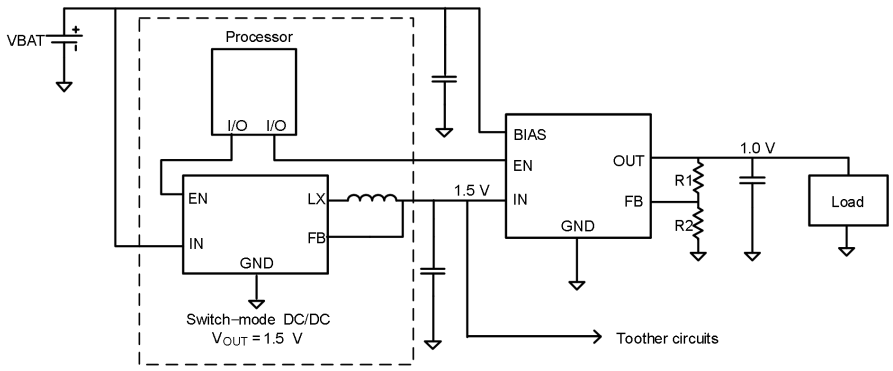


Figure 15. Typical application : low−voltage DC/DC post−regulator with ON/OFF functionality

Note: (1) The recommended power-on sequence is that BIAS and IN start first, and EN starts last.

Application Information

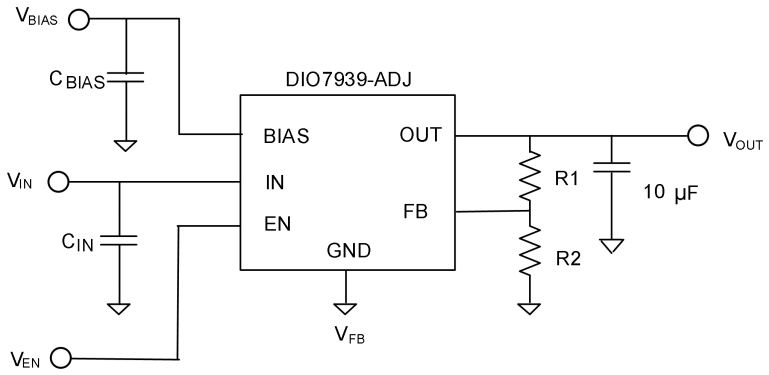
Overview

The DIO7939 is a dual−rail very low dropout voltage regulator that uses NMOS pass transistor for output voltage regulation from V_{IN} voltage. All the low current internal control circuitry is powered by the V_{BIAS} voltage.

The use of an NMOS pass transistor offers several advantages in applications. Unlike PMOS topology devices, the output capacitor has a reduced impact on loop stability. V_{IN} to V_{OUT} operating voltage difference can be very low compared with standard PMOS regulators in very low V_{IN} applications. The DIO7939 offers a smooth monotonic start-up. The controlled voltage rising limits the inrush current. The enable (EN) input is equipped with internal hysteresis. The DIO7939 voltage linear regulator Fixed and Adjustable version is available.

Output voltage adjustable

The required output voltage of adjustable devices can be adjusted from 0.5 V to 3.3 V using two external resistors. Typical application schematics are shown in Figure 16.



$$V_{OUT} = V_{FB} \times (1 + R1/R2)$$

Figure 16. Typical application

It is recommended to keep the total serial resistance of resistors (R1 + R2) no greater than 100 kΩ.

Dropout voltage

There are two dropout voltages specified since there are two power supply inputs V_{IN} and V_{BIAS} and one V_{OUT} regulator output. The first is the V_{IN} dropout voltage and the second is the V_{BIAS} dropout voltage. The V_{IN} dropout voltage is the voltage differencial (V_{IN} – V_{OUT}) when V_{OUT} starts to decrease by the percent specified in the Electrical Characteristics table while V_{BIAS} is high enough. Refer to the Electrical Characteristics table for a specific value. The V_{BIAS} dropout voltage is the voltage differencial (V_{BIAS} – V_{OUT}) when V_{IN} and V_{BIAS} pins are joined together and V_{OUT} starts to decrease.

Input and output capacitors

The device is suitable for multiple capacitors in parallel and ceramic output capacitors with effective capacitance in the range from 10 μF to 22 μF. In applications where no low input supplies impedance available (PCB inductance in V_{IN} and/or V_{BIAS} inputs example). Ceramic capacitors are recommended. Ideally, all capacitors should be connected directly to the DIO7939 respective pins in the device PCB copper layer, not through vias with an impedance that cannot be neglected. The capacitance of small ceramic capacitors varies with the applied DC biasing voltage, temperature, and tolerance. Negative temperatures and higher LDO output voltages can result in much lower capacitance values than their nominal values. That is why the recommended output capacitor capacitance value is specified as the effective value in the specific application conditions.

Enable operation

The enable pin controls the regulator's operation. Refer to the electrical characteristics table in this datasheet for the threshold limits. Tie the pin to V_{IN} or V_{BIAS} when it is not needed.

Current limit

The internal current limitation circuitry allows the device to supply the full 1.5 A nominal current. When the device is at the current limit, the output voltage is not regulated. The gadget starts to heat up when a current limit event happens due to the rise in power dissipation. The device shuts down if the thermal shutdown occurs. The inbuilt thermal shutdown circuit restarts the device once it has cooled down. The device alternates between the current limit and thermal shutdown if the output current fault situation persists. Therefore, after the thermal protection is triggered, it is recommended that the load is preferably lower than the I_{SC} at startup.

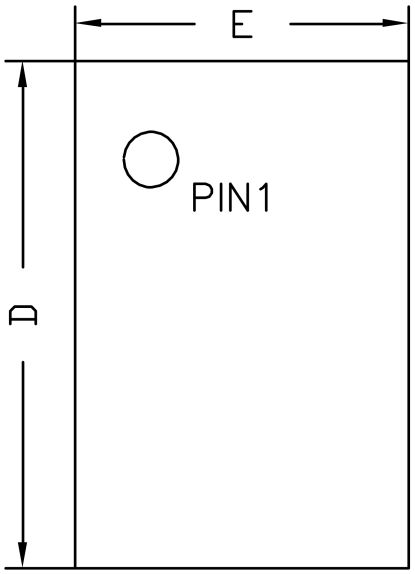
Thermal protection

The regulator output is turned off when internal thermal shutdown (T_{SD}) is activated. As soon as the device temperature drops below the low-temperature threshold, the output is activated again. This T_{SD} feature can prevent failures from accidental overheating. Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. To ensure reliable operation, the junction temperature needs to be limited to 85°C.

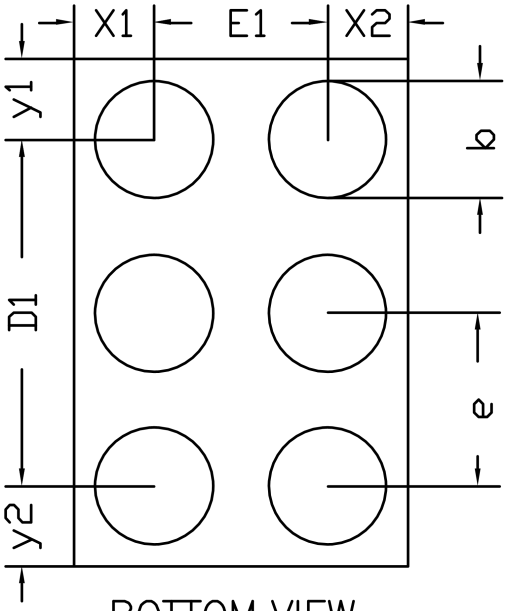
PCB layout recommendations

An optimal layout can significantly improve transient performance, PSR, and noise. Make the PCB traces widely spaced and place the C_{IN} and C_{OUT} capacitors close to the device pins for excellent performance and superior regulation. Place around return connections to the input and output capacitors. Also, a larger copper area in contact with the pins will improve the thermal resistance of the device. The exposed pad can be tied to the GND pin for better power dissipation and lower device temperatures.

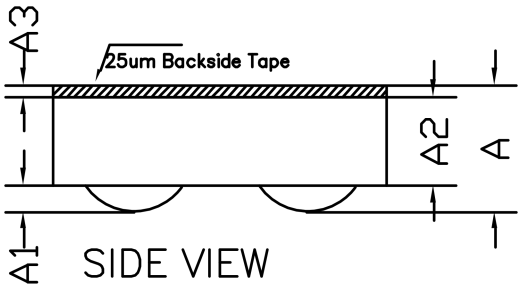
Physical Dimensions: WLCSP-6



TOP VIEW
(MARK SIDE)



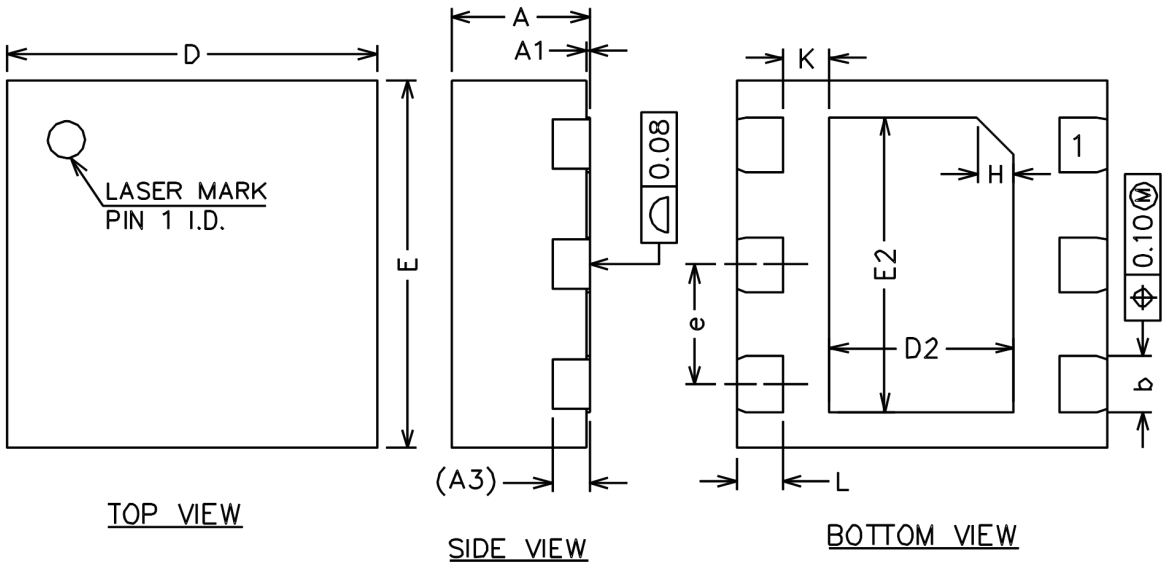
BOTTOM VIEW
(BALL SIDE)



SIDE VIEW

Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.270	0.290	0.310
A1	0.040	0.060	0.080
A2		0.205 REF	
A3		0.025 REF	
D	1.140	1.170	1.200
D1		0.800 BSC	
E	0.740	0.770	0.800
E1		0.400 BSC	
b	0.240	0.270	0.300
e		0.400 BSC	
x1		0.185 REF	
x2		0.185 REF	
y1		0.185 REF	
y2		0.185 REF	

Physical Dimensions: DFN2*2-6



Common Dimensions (Units of Measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.90	1.00	1.10
E2	1.50	1.60	1.70
e	0.55	0.65	0.75
K	0.15	0.25	0.35
L	0.20	0.25	0.30
H		0.20 REF	

CONTACT US

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For additional product information or full datasheet, please contact our sales department or representatives.