DIO7495

28 V, Over-Voltage, Over-Current Protection Load Switch with Adjustable Current-Limit Control

Description

The DIO7495 load-management switch is designed for applications that demand a highly integrated solution. It disconnects loads powered from the DC power rail (< 5.5 V) with high load-capacitance and strict off-state current targets. The DIO7495 has both over-current protection and over-voltage protection.

Unwanted reverse current from V_{OUT} to V_{IN} during ON and OFF states is stopped by the real reverse-current blocking (RRCB) function. The low off-state current drain (< 2 μA maximum) is utilized to help meet standby power conditions. To support a wide range of applications in storage, such as medical, consumer, optical, and industrial-device power management, the input voltage will operate from 2.5 V to 5.5 V DC. Switch control is handled by a logic input (Active HIGH) that can interact directly with low-voltage control signal/general-purpose input/output (GPIO) without the assistance of an external pull-down resistor. The DIO7495 is packaged in flip-chip QFN1.2*1.2-9.

Feature

- RRCB function
- Operating input voltage range: 2.5 V to 5.5 V
- Absolute rating at output voltage: 28 V
- Current capability: 2 A
- Adjustable current limit: 0.05 A to 2 A (Typ.)
  - 0.1 A to 2 A with 10% accuracy
  - < 0.1 A with 15% accuracy
- Maximum on-resistance of 81 mΩ at 5 V input voltage and 1 A output current at T_A = 25°C
- Output OVP (Typ.): 5.8 V
- No output discharge during off-state
- Open-drain OCP on FLAGB
- Thermal shutdown
- Undervoltage lockout (UVLO)
- Package: QFN1.2*1.2-9

Applications

- Smart phones
- Tablets
- Storage devices
- Cameras
- Portable devices

Ordering Information

Part Number	Top Marking	RoHS	T_A	Package	
DIO7495ED9	W5	Green	-40 to 85°C	QFN1.2*1.2-9	Tape & Reel, 5000

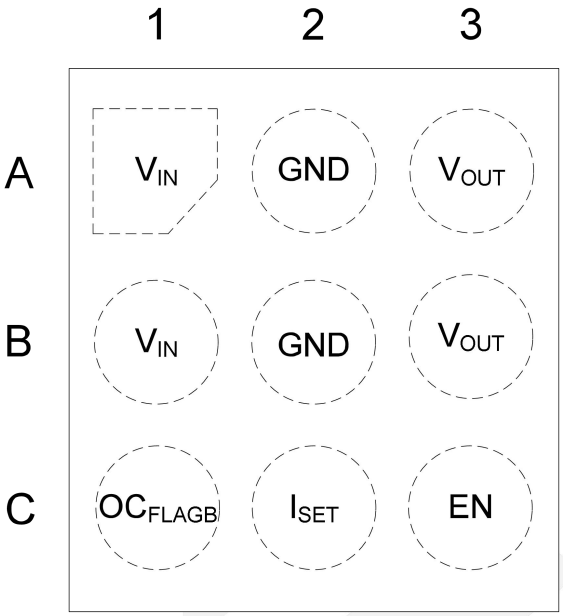
If you encounter any issue in the process of using the device, please contact our customer service at marketing@dioo.com or phone us at (+86)-21-62116882. If you have any improvement suggestions regarding the datasheet, we encourage you to contact our technical writing team at docs@dioo.com. Your feedback is invaluable for us to provide a better user experience.

Table of Contents

List of Figures

List of Tables

Pin Assignment and Functions



QFN1.2*1.2-9
Top view

Pin No.	Pin Name	Description
A1, B1	V_{IN}	Supply input. Input to the power switch.
A2, B2	GND	Ground
A3, B3	V_{OUT}	Switch output.
C1	OC_{FLAGB}	Fault output. Active LOW, open-drain output that indicates an input over current. External pull-up resistor to V_{IN} is required.
C2	I_{SET}	Current limit set input. A resistor from I_{SET} to ground sets the current limit for the switch.
C3	EN	ON/OFF control input. Active HIGH – GPIO compatible, Logic HIGH = switch enable, Logic LOW = switch disable

1. Absolute Maximum Ratings

Exceeding the maximum ratings listed under Absolute Maximum Ratings when designing is likely to damage the device permanently. Do not design to the maximum limits because long-time exposure to them might impact the device's reliability. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameters	Min	Max	Unit
V_{PIN}	V_{OUT} to GND, V_{OUT} to V_{IN}	-0.3	28	V
	EN, V_{IN}, FLAGB, I_{SET} to GND	-0.3	6	
I_{SW}	Maximum continuous switch current(1)		2.2	A
P_D	Total power dissipation at T_A = 25ºC		1	W
T_J	Operating junction temperature	-40	150	ºC
T_{STG}	Storage junction temperature	-65	150	ºC

Note:

(1) $T_{J(MAX)}$ = 85ºC

2. Recommended Operating Condition

Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature	-40	85	ºC

3. ESD Ratings

When a statically-charged person or object touches an electrostatic discharge sensitive device, the electrostatic charge might be drained through sensitive circuitry in the device. If the electrostatic discharge possesses sufficient energy, damage might occur to the device due to localized overheating.

Model	Condition	Value	Unit
HBM	ANSI/ESDA/JEDEC JS-001	±7000	V
CDM	ANSI/ESDA/JEDEC JS-002	±2000	V
Latch up	JEDEC JESD78F.01	±200	mA

4. Thermal Considerations

The thermal resistance determines the heat insulation property of a material. The higher the thermal resistance is, the lower the heat loss. Accumulation of heat energy degrades the performance of semiconductor components.

Symbol	Metric	Value	Unit
θ_{JA}	Thermal resistance, junction-to-ambient	94	°C/W

5. Electrical Characteristics

V_{IN} = 2.5 V to 5.5 V; typical values are at V_{IN} = 5 V and T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Basic operation						
V_{IN}	Input voltage		2.5		5.5	V
$I_{Q(OFF)}$	Off supply current	V_{EN} = GND, V_{OUT} = Open		0.5	2	μA
$I_{SD(OFF)}$	Shutdown current	V_{IN} = 5.5 V, V_{OUT} = 0 V, V_{EN} = GND		0.5	2	μA
I_Q	Quiescent current	I_{OUT} = 0 mA		65	100	μA
R_{ON}	On resistance	V_{IN} = 5.0 V, I_{OUT} = 1 A		70		mΩ
		V_{IN} = 3.7 V, I_{OUT} = 1 A		75		
		V_{IN} = 5.0 V, I_{OUT} = 1.5 A		70		mΩ
V_{IH}	EN input logic HIGH voltage	V_{IN} = 2.5 V to 5.5 V	0.8			V
V_{IL}	EN input logic LOW voltage	V_{IN} = 2.5 V to 5.5 V			0.35	V
V_{IL_FLAG}	FLAGB output logic LOW voltage	V_{IN} = 5 V, I_{SINK} = 10 mA		0.1	0.2	V
		V_{IN} = 2.5 V, I_{SINK} = 10 mA		0.15	0.3	
I_{FLAGB_LK}	FLAGB output HIGH leakage current	V_{IN} = 5 V, switch on			1	μA
I_{EN}	En input leakage	V_{EN} = 0 V to V_{IN}			1	μA
R_{EN_PD}	Pull-down resistance at EN pin	V_{IN} = 2.5 to 5.5 V, V_{EN} = HIGH		18		MΩ
Over-voltage protection						
V_{OUT_OVP}	Output OVP lockout	V_{OUT} rising threshold	5.5	5.8	6	V
		V_{OUT} falling threshold		5.7		
V_{OUTOVP_HYS}	Output OVP hysteresis	V_{OUT} falling threshold		0.1		V
t_{OVP} (2)	OVP response time	I_{OUT} = 0.5 A, C_L = 1 μF, T_A = 25°C, V_{OUT} from 5.5 V to 6.0 V		0.2		μs

Over-current protection

I_{LIM}	Current limit	V_{IN} = 5 V, R_{SET} = 20 kΩ, V_{OUT} = 1.68 to 5 V with 15% accuracy(1)	43	50	58	mA
		V_{IN} = 5 V, R_{SET} = 2 kΩ, V_{OUT} = 1.68 to 5 V with 10% accuracy(1)	450	500	550	
		V_{IN} = 5 V, R_{SET} = 1 kΩ V_{OUT} = 1.68 to 5 V with 10% accuracy(1)	907	1008	1109	
V_{UVLO}	Under–voltage lockout	V_{IN} increasing		2.4		V
		V_{IN} decreasing		2.2		
V_{UVLO_HYS}	UVLO hysteresis			200		mV
V_{T_RCB}	RCB protection trip point	V_{OUT} - V_{IN}		50		mV
V_{R_RCB}	RCB protection release trip point	V_{IN} - V_{OUT}		50		mV
V_{RCB_HYS}	RCB hysteresis			100		mV
t_{RCB}	Default RCB response time	V_{IN} = 5 V, V_{EN} = HIGH/LOW		0.3		μs
I_{RCB}	RCB current	V_{EN} = 0 V, V_{OUT} = 5.5 V		7		μA
t_{HOCP}	Hard over-current response time	Moderate over-current condition $I_{OUT} \geq I_{LIM}$, V_{OUT} = 0 V, C_{IN} = 10 uF, R_{SET} = 10.7 kΩ		6		μs
t_{OCP}	Over-current response time	Moderate over-current condition $I_{OUT} \geq I_{LIM}$, $V_{OUT} \leq V_{IN}$, C_{IN} = 10 uF, R_{SET} = 10.7 kΩ		7		μs
t_{OC_FLAG}	Over-current flag response time	When over-current occurs to flag pulling low		10		ms
T_{SD}	Thermal shutdown	Shutdown threshold		150		ºC
		Return from shutdown		130		
		Hysteresis		20		

Dynamic characteristics

t_{DON}	Turn-on delay(2,3)	V_{IN} = 5 V, R_L = 100 Ω, C_L = 1 μF, T_A = 25°C, R_{SET} = 2 kΩ		0.88		ms
t_R	V_{OUT} rise time(2,3)			1.29		ms
t_{ON}	Turn-on time(2,3)			2.17		ms
t_{DOFF}	Turn-off delay(2,3)			0.01		ms
t_F	V_{OUT} fall time(2,3)			0.28		ms
t_{OFF}	Turn-off time(2,3)			0.29		ms

Note:

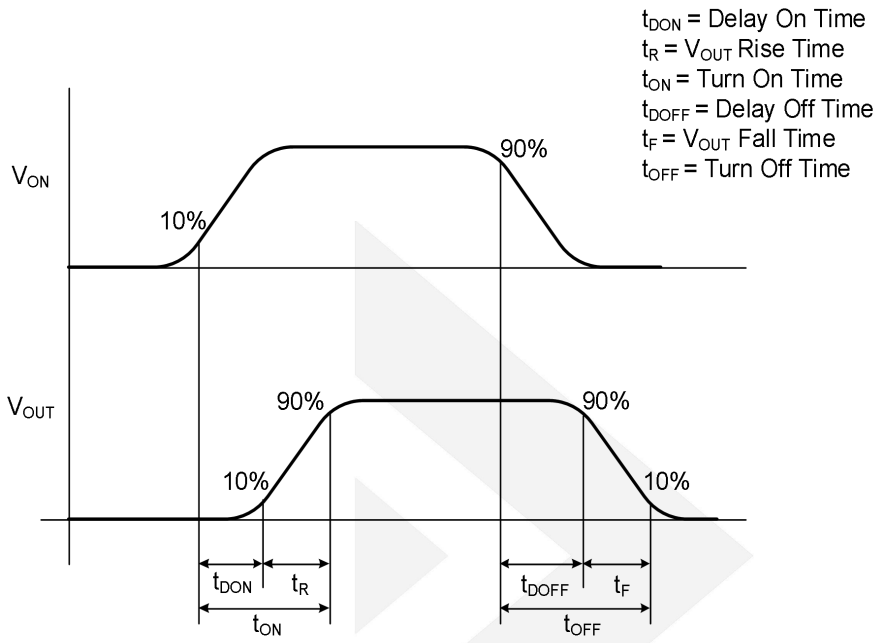
(1) Characterization based on 1% tolerance resistor.

(2) Guaranteed by design; not production tested.

(3) t_{DON}/t_{DOFF}/t_R/t_F are defined in the Timing Diagram below, t_{ON} = t_R + t_{DON}, t_{OFF} = t_F + t_{DOFF}.

(4) Specifications subject to change without notice.

6. Timing Diagram



7. Typical Performance Characteristics

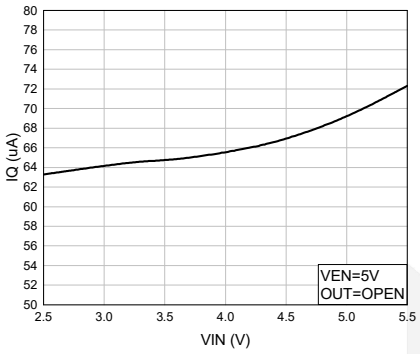


Figure 1. I_Q vs. V_{IN}

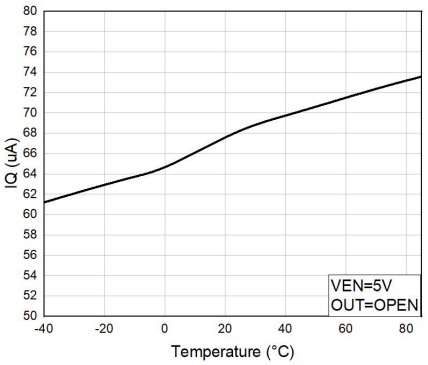


Figure 2. I_Q vs. Temperature

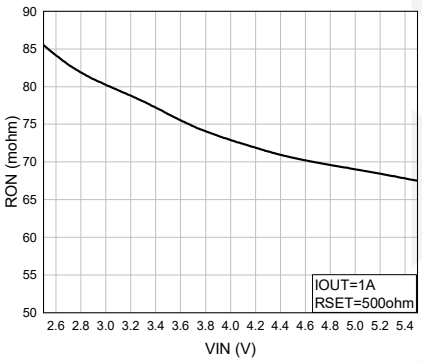


Figure 3. R_{ON} vs. V_{IN}

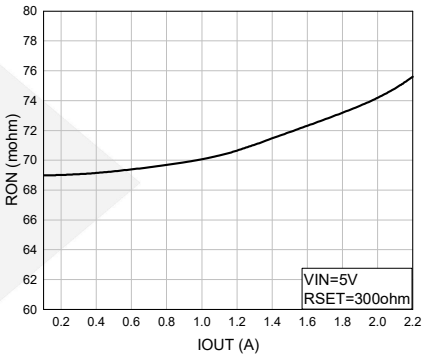


Figure 4. R_{ON} vs. I_{OUT}

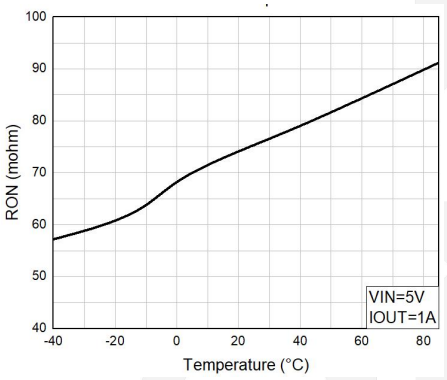
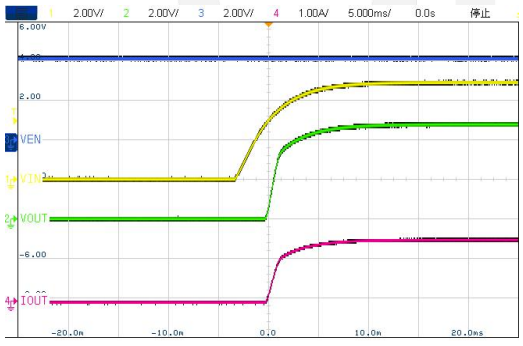
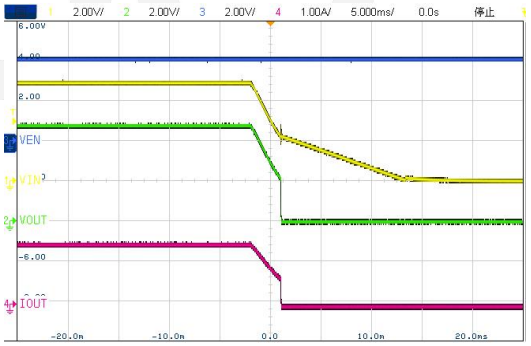


Figure 5. R_{ON} vs. Temperature



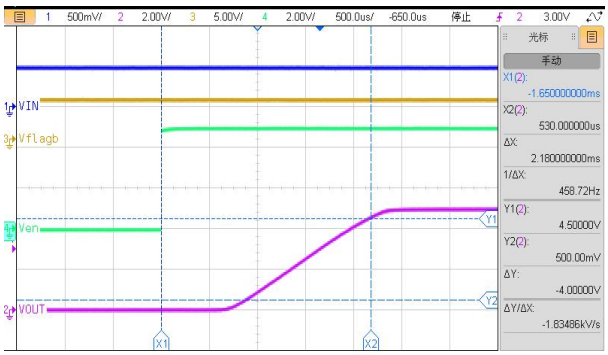
V_{IN} = 5 V, R_L = 3 Ω, C_{IN} = C_{OUT} = 1 μF, R_{SET} = 510 Ω

Figure 6. Power on



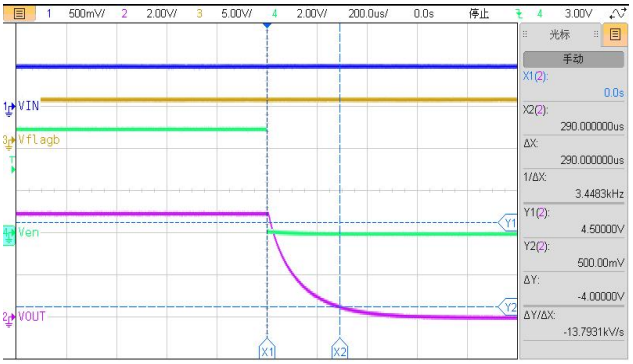
V_{IN} = 5 V, R_L = 3 Ω, C_{IN} = C_{OUT} = 1 μF, R_{SET} = 510 Ω

Figure 7. Power off



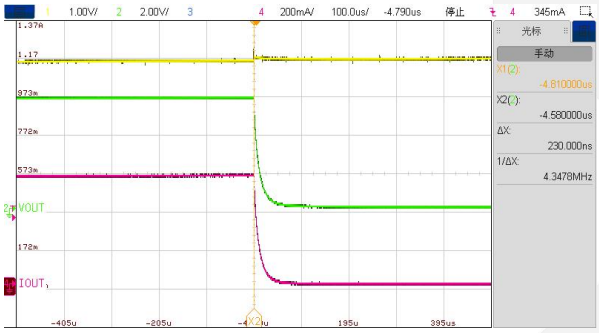
V_{IN} = 5 V, R_L = 100 Ω, C_L = 1 µF, R_{SET} = 2 kΩ

Figure 8. Turn on



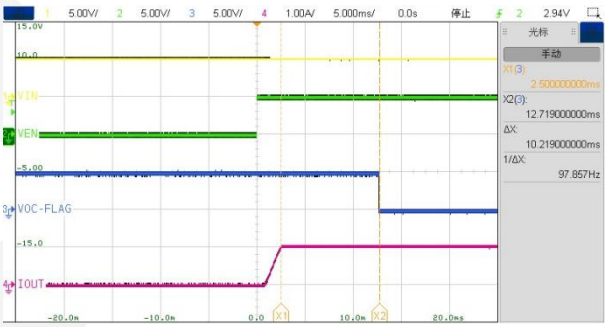
V_{IN} = 5 V, R_L = 100 Ω, C_L = 1 µF, R_{SET} = 2 kΩ

Figure 9. Turn off



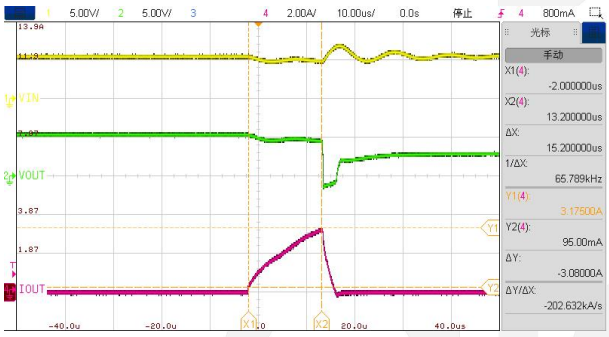
Increase V_{OUT} to OVP trip point

Figure 10. OVP response time



V_{IN} = 5.5 V, V_{OUT} = 4.5 V, R_{SET} = 2 kΩ

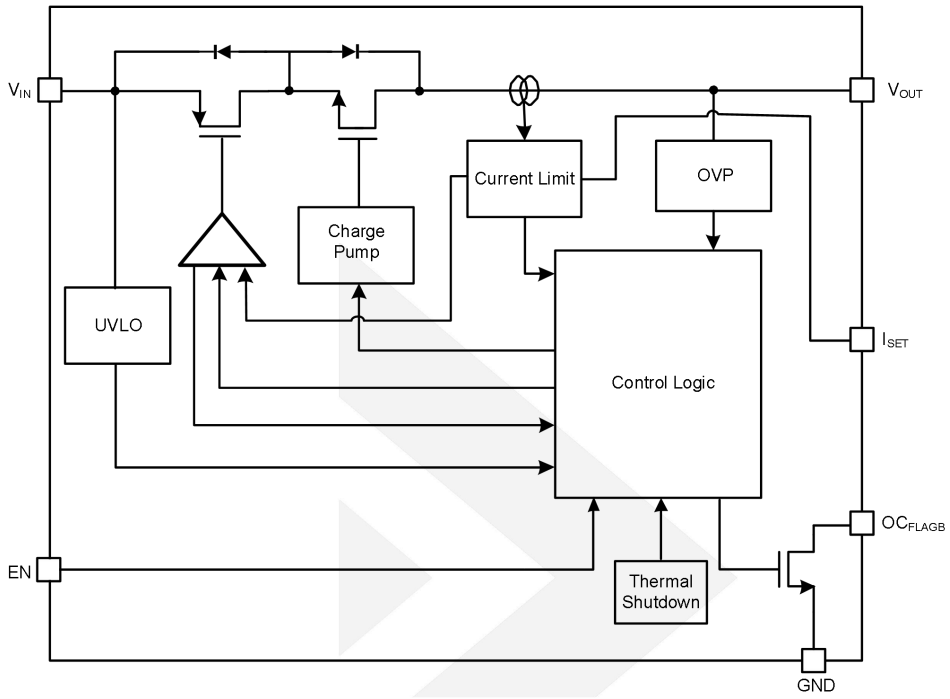
Figure 11. OC_flag response time



V_{IN} = 5.5 V, V_{OUT} = 3 V, R_{SET} = 10.7 kΩ

Figure 12. t_{OCP}

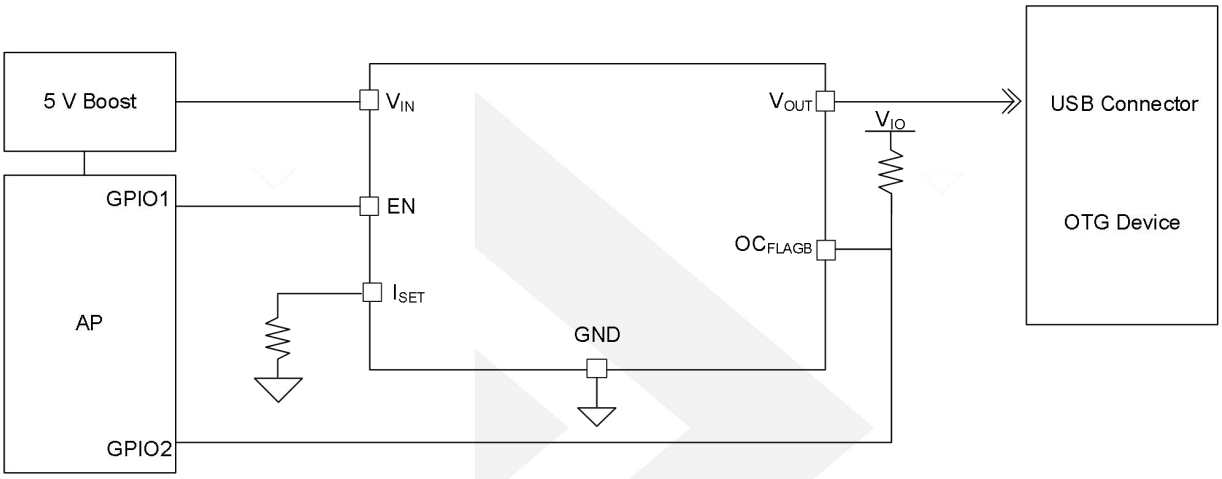
8. Block Diagram



9. Application Information

Important notice: Validation and testing are the most reliable ways to confirm system functionality. The application information is not part of the specification and is for reference purposes only.

9.1. Application example



9.2. Input capacitor

Place a capacitor between the GND and V_{IN} pins to restrict the voltage drop on the input supply created by the transient inrush current when the switch turns on into a discharge load capacitor; to limit the voltage drop in high-current applications, implement a high-value capacitor on C_{IN}.

9.3. Output capacitor

Place an output capacitor between V_{OUT} and GND pins to prevent parasitic board inductance from forcing V_{OUT} below GND when the switch is on. Using an output capacitor also provides the additional benefit of preventing reverse inrush current from causing a voltage spike that could be detrimental to the device in the case of a V_{OUT} short.

9.4. Fault reporting

OC_FLAGB signals the fault by activating LOW when it detects an over-current.

9.5. Current limiting

Current limit prevents the current from going over the maximum set value and does not limit the minimum value. Using the external resistor connected to the I_{SET} pin to determine the current that the part limits.

Information regarding resistor selection is found in Table 1. Until thermal shutdown occurs, the device acts as a constant-current source when the load draws more than the maximum value set by the device. Once the die temperature is within the threshold temperature, the device will recover. When the output voltage is below 0.7 V, the current limiting value will decrease, thereby protecting the chip.

9.6. Undervoltage lockout (UVLO)

If the input voltage drops below the lockout threshold, the undervoltage lockout will activate to turn the switch off. The switch will be enabled if the input voltage rises above the undervoltage lockout threshold while the EN pin is active.

9.7. Real reverse-current blocking (RRCB)

Regardless of whether the load switch is on or off, the real reverse-current blocking function protects the input source against the current flow from output to input.

9.8. Thermal shutdown

A thermal shutdown occurs when the switch turns off to protect the die from internally or externally generated temperature that exceeds over-temperature conditions. The switch will turn back on as soon as the temperature of the die cools down and is within the threshold temperature.

9.9. Setting current limit

Using the external resistor connected between the I_{SET} and GND pins to set the current limit. Use Table 1 to select the resistor. Resistor tolerance of 1% or less is recommended.

Table 1. Current limit setting by R_{SET}(1)

R_{SET} (Ω)	Min current limit (mA)	Typ current limit (mA)	Max current limit (mA)
510	1793	1992	2191
604	1494	1660	1826
680	1337	1485	1634
820	1102	1224	1346
1000	907	1008	1109
1200	748	831	914
1500	596	662	728
2000	450	500	550
2200	413	459	505
2490	364	405	445
3000	303	336	370
3300	276	306	337
4020	226	251	276
5110	179	199	218
8200	110	123	135
10000	80	94	109
15000	57	67	77
18000	47	56	64
20000	43	50	58

Note:

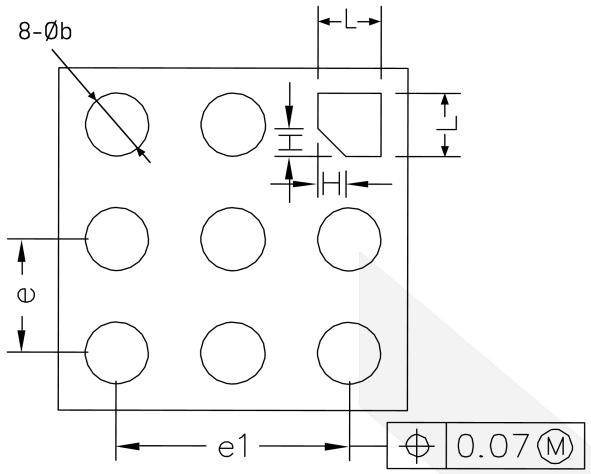
(1) Table values based on 1% tolerance resistor.

(2) For settings under 100 mA, tolerance is ±15% with 1%.

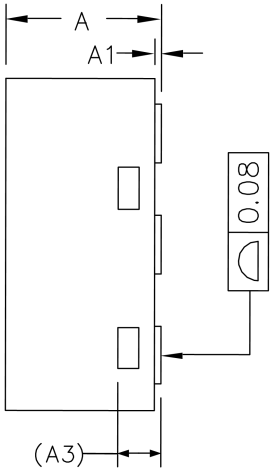
10. Layout Guidelines

For optimal performance, minimize the length of traces as much as possible. It is also recommended to place the input and output capacitors close to the device to maximize effectiveness and minimize the effect of potential parasitic trace inductance may have on normal and short-circuit operations. To minimize parasitic electrical effects and case-to-ambient thermal impedance, use wide traces for V_{IN}, V_{OUT}, and GND.

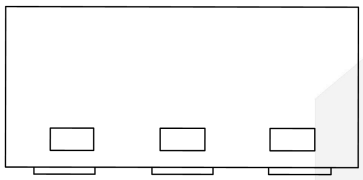
11. Physical Dimensions: QFN1.2*1.2-9



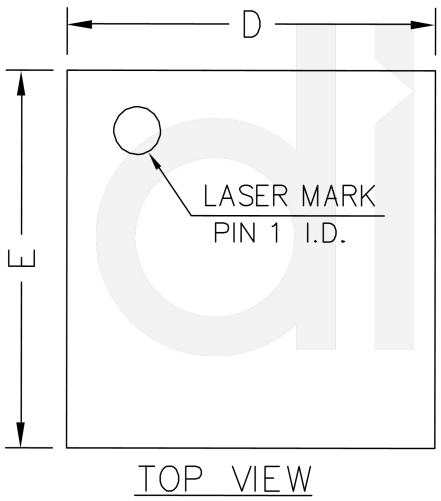
BOTTOM VIEW



SIDE VIEW



SIDE VIEW



TOP VIEW

Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3		0.152 REF	
b	0.17	0.22	0.27
D	1.10	1.20	1.30
E	1.10	1.20	1.30
e	0.35	0.40	0.45
e1	0.75	0.80	0.90
H		0.10 REF	
L	0.17	0.22	0.27

Disclaimer

This specification and information contained herein are provided on an “AS IS” basis and WITH ALL FAULTS. All product specifications, statements, information, and data (collectively, the “Information”) in this datasheet or made available on the website of www.dioo.com are subject to change without notice. The customer is responsible for checking and verifying the extent to which the Information contained in this publication is applicable to his/her application. All Information given herein is believed to be accurate and reliable, but it is presented without guarantee, warranty, or responsibility of any kind, express or implied.

