DIO5907x
Standalone 1-Cell 1.1 A Linear Battery Charger with Power Path

Features

- Fully compliant USB charger
  - Selectable 100 mA and 500 mA maximum input current
  - 100 mA maximum current limit ensures compliance to USB-IF standard
  - Input-based dynamic power management (V_{IN}- DPM) for protection against poor USB sources
- 10% charge current accuracy
- 0.7% charge voltage accuracy
- 28 V input rating with overvoltage protection
- Integrated dynamic power path management (DPPM) function simultaneously and independently powers the system and charges the battery
- Supports up to 1.1 A charge current with current monitoring output (ISET)
- Programmable input current limit up to 1.1 A for wall adapters
- Programmable termination current (DIO59078)
- Programmable pre-charge and fast-charge safety timers
- Reverse current, short-circuit and thermal protection
- NTC thermistor input
- Proprietary start-up sequence limits inrush current
- Status indication–charging/done, power good

Descriptions

The DIO5907x series of devices are integrated Li-Ion linear chargers and system power path management devices targeted at space-limited portable applications. The devices operate from either a USB port or an AC adapter and support charge currents up to 1.1 A. The input voltage range with input overvoltage protection supports unregulated adapters. The USB input current limit accuracy and start up sequence allow the DIO5907x to meet USB-IF inrush current specifications. Additionally, the input dynamic power management (V_{IN-DPM}) prevents the charger from crashing incorrectly configured USB sources.

The DIO5907x features dynamic power path management (DPPM) that powers the system while simultaneously and independently charging the battery. The DPPM circuit reduces the charge current when the input current limit causes the system output to fall to the DPPM threshold; thus, supplying the system load at all times while monitoring the charge current separately. This feature reduces the number of charge and discharge cycles on the battery, allows for proper charge termination and enables the system to run with a defective or absent battery pack.

Applications

- Smart phones
- Portable media players
- Portable navigation devices
- Low-power handheld device

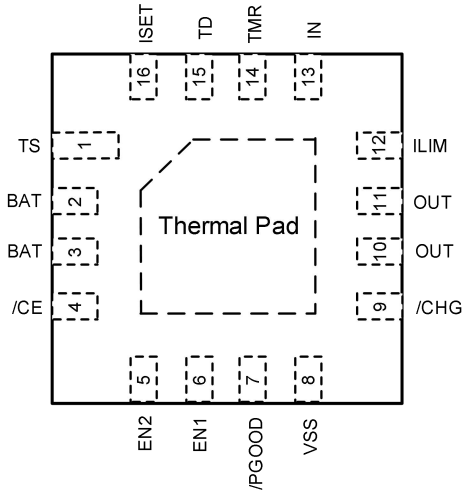
Ordering Information

Ordering Part No.	Top Marking	MSL	RoHS	T_A	Package	
DIO59073CL16	DJVG3	3	Green	-40 to 85°C	QFN3*3-16	Tape & Reel, 5000
DIO59073BCL16	DVG3B	3	Green	-40 to 85°C	QFN3*3-16	Tape & Reel, 5000
DIO59075CL16	DJVG5	3	Green	-40 to 85°C	QFN3*3-16	Tape & Reel, 5000
DIO59078CL16	DJVG8	3	Green	-40 to 85°C	QFN3*3-16	Tape & Reel, 5000

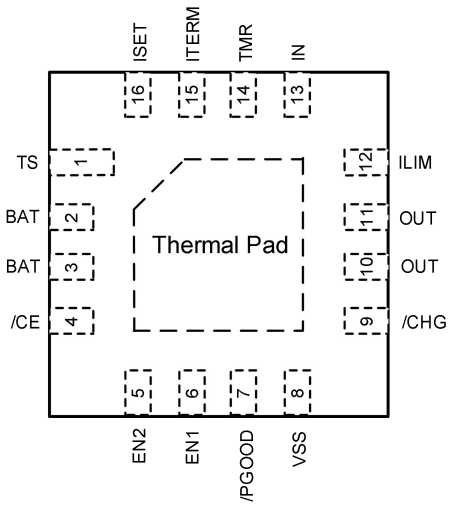
Device Comparison Table

Ordering Part No.	V_{OVP}	$V_{BAT(REG)}$	$V_{OUT(REG)}$	V_{DPPM}	TS Method	Optional Function
DIO59073CL16	6.6 V	4.2 V	4.4 V	$V_{O(REG)}$ – 100 mV	Current based	TD
DIO59073BCL16	6.6 V	4.2 V	4.4 V	$V_{O(REG)}$ – 100 mV		TD
DIO59075CL16	6.6 V	4.2 V	5.5 V	5.3 V		SYSOFF
DIO59078CL16	6.6 V	4.2 V	4.4 V	$V_{O(REG)}$ – 100 mV		ITERM

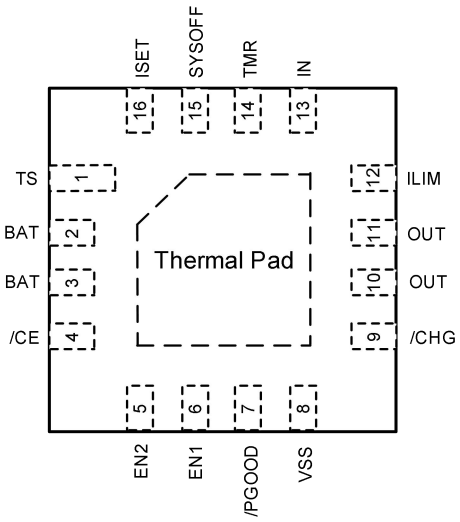
Pin Assignment



DIO59073 / DIO59073B
QFN3*3-16



DIO59078
QFN3*3-16



DIO59075
QFN3*3-16

Pin Descriptions

Name	I/O	Description
TS	I	External NTC Thermistor Input. Connect the TS input to the NTC thermistor in the battery pack. TS monitors a 10 kΩ NTC thermistor. For applications that do not use the TS function, connect a 10 kΩ fixed resistor from TS to VSS to maintain a valid voltage level on TS.
BAT	I/O	Charger Power Stage Output and Battery Voltage Sense Input. Connect BAT to the positive terminal of the battery. Bypass BAT to VSS with a 4.7 µF to 47 µF ceramic capacitor.
/CE	I	Charge Enable Active-Low Input. Connect /CE to a high logic level to disable battery charging. OUT is active and battery supplement mode is still available. Connect /CE to a low logic level to enable the battery charger. /CE is internally pulled down with approximately 285 kΩ. Do not leave /CE unconnected to ensure proper operation.
EN1	I	Input Current Limit Configuration Inputs. Use EN1 and EN2 control the maximum input current and enable USB compliance. See Table 1 for the description of the operation states. EN1 and EN2 are internally pulled down with ≈285 kΩ. Do not leave EN1 or EN2 unconnected to ensure proper operation.
EN2	I	
/PGOOD	O	Open-drain Power Good Status Indication Output. /PGOOD pulls to VSS when a valid input source is detected. /PGOOD is high-impedance when the input power is not within specified limits. Connect /PGOOD to the desired logic voltage rail using a 1 kΩ to 100 kΩ resistor, or use with an LED for visual indication.
VSS	–	Ground. Connect to the thermal pad and to the ground rail of the circuit.
/CHG	O	Open-Drain Charging Status Indication Output. /CHG pulls to VSS when the battery is charging. /CHG is high impedance when charging is complete and when charger is disabled. Connect /CHG to the desired logic voltage rail using a 1 kΩ to 100 kΩ resistor, or use with an LED for visual indication.
OUT	O	System Supply Output. OUT provides a regulated output when the input is below the OVP threshold and above the regulation voltage. When the input is out of the operation range, OUT is connected to VBAT except when SYSOFF is high (DIO59075 only). Connect OUT to the system load. Bypass OUT to VSS with a 4.7 µF to 47 µF ceramic capacitor.
ILIM	I	Adjustable Current Limit Programming Input. Connect a 1100 Ω to 8 kΩ resistor from ILIM to VSS to program the maximum input current (EN2 = 1, EN1 = 0). The input current includes the system load and the battery charge current. Leaving ILIM unconnected disables all charging.
IN	I	Input Power Connection. Connect IN to the external DC supply (AC adapter or USB port). The input operating range is 4.35 V to 6.4 V (DIO59073/ 73B/ 75 /78). The input can accept voltages up to 28 V without damage but operation is suspended. Connect bypass capacitor 4.7 µF to 10 µF to VSS.

TMR	I	Timer Programming Input. TMR controls the pre-charge and fast-charge safety timers. Connect TMR to VSS to disable all safety timers. Connect a 18 kΩ to 72 kΩ resistor between TMR and VSS to program the timers a desired length. Leave TMR unconnected to set the timers to the default values.
TD	I	Termination Disable Input. Connect TD high to disable charger termination. Connect TD to VSS to enable charger termination. See the TD section in this datasheet for a description of the behavior when termination is disabled. TD is internally pulled down to VSS with approximately 285 kΩ. Do not leave TD unconnected to ensure proper operation. (DIO59073/73B).
ITERM	I	Termination Current Programming Input. Connect a 0 Ω to 15 kΩ resistor from ITERM to VSS to program the termination current. Leave ITERM unconnected to set the termination current to the default 10% termination threshold. (DIO59078 only).
SYSOFF	I	System Enable Input. Connect SYSOFF high to turn off the FET connecting the battery to the system output. When an adapter is connected, charging is also disabled. Connect SYSOFF low for normal operation. SYSOFF is internally pulled up to VBAT through a large resistor (approximately 5 MΩ). Do not leave SYSOFF unconnected to ensure proper operation. (DIO59075 only).
ISET	I/O	Fast Charge Current Programming Input. Connect a 590 Ω to 8.9 kΩ resistor from ISET to VSS to program the fast charge current level. Charging is disabled if ISET is left unconnected. While charging, the voltage at ISET reflects the actual charging current and can be used to monitor charge current.
Thermal Pad	–	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

Table 1. EN1 / EN2 Settings

EN2	EN1	Maximum Input Current Into IN Pin
0	0	100 mA. USB100 mode
0	1	500 mA. USB500 mode
1	0	Set by an external resistor from ILIM to VSS
1	1	Standby (USB suspend mode)

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter		Min	Max	Unit
V_I	Input voltage	IN (with respect to VSS)	-0.3	28	V
		BAT (with respect to VSS)	-0.3	5	V
		OUT, EN1, EN2, /CE, TS, ISET, /PGOOD, /CHG, ILIM, TMR, ITERM, SYSOFF, TD (with respect to VSS)	-0.3	7	V
I_{IN}	Input current	IN		1.2	A
I_O	Output current (Continuous)	OUT		3	A
		BAT (Discharge mode)		3	A
		BAT (Charging mode)		1.1(1)	A
	Output sink current	/CHG, /PGOOD		15	mA
T_J	Junction temperature		-40	150	°C
T_{STG}	Storage temperature		-65	150	°C
ESD	HBM		-2000	2000	V

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min	Max	Unit
V_I	IN voltage range	4.35	28	V
	IN operating voltage range	4.35	6.4	V
I_{IN}	Input current, IN pin		1.1	A
I_{OUT}	Current, OUT pin		3	A
I_{BAT}	Current, BAT pin (Discharging)		3	A
I_{CHG}	Current, BAT pin (Charging)		1.1(1)	A
T_J	Junction Temperature	-40	125	°C
R_{ILIM}	Maximum input current programming resistor	500	10k	Ω
R_{ISET}	Fast-charge current programming resistor (2)	500	10k	Ω
R_{ITERM}	Termination current programming resistor	0	15	kΩ
R_{TMR}	Timer programming resistor	18	72	kΩ
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.5		°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.2		
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.8		

Note:

(1) The IC operational charging life is reduced to 20,000 hours, when charging at 1.1 A and 125°C. The thermal regulation feature reduces charge current if the IC’s junction temperature reaches 125°C; thus without a good thermal design the maximum programmed charge current may not be reached.

(2) Use a 1% tolerance resistor for R_{ISET} to avoid issues with the R_{ISET} short test when using the maximum charge current setting.

Electrical Characteristics

Over junction temperature range (0° ≤ T_J ≤ 125°C) and the recommended supply voltage range (unless otherwise noted).

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
Input							
UVLO	Under-voltage lockout	V_{IN}: 0 V → 4 V		3.2	3.0	3.2	V
$V_{IN(DT)}$	Input power detection threshold	Input power detected when V_{IN} > V_{BAT} + $V_{IN(DT)}$, V_{BAT} = 3.6 V, V_{IN}: 3.5 V → 4 V		55	120	130	mV
$t_{DGL(PGOOD)}$	Deglitch time, input power detected status	Time measured from V_{IN}: 0 V → 5 V 1 µs rise-time to /PGOOD = LO			1.2		ms
V_{OVP}	Input overvoltage protection threshold	V_{IN}: 5 V → 7 V		6.4	6.6	6.8	V
V_{hys}	Hysteresis on OVP	V_{IN}: 7 V → 5 V			200		mV
$t_{DGL(OVP)}$	Input overvoltage blanking time (OVP fault deglitch)				10		µs
t_{REC}	Input overvoltage recovery time	Time measured from V_{IN}: 11 V → 5 V with 1 µs fall-time to /PGOOD = LO			1.0		ms
Quiescent current							
$I_{BAT(PDWN)}$	Sleep current into BAT pin	/CE = LO or HI, input power not detected, No load on OUT pin, T_J = 85°C				1.3	µA
I_{IN}	Standby current into IN pin	EN1 = HI, EN2 = HI, V_{IN} = 5 V, T_J= 85°C				60	µA
I_{CC}	Active supply current, IN pin	/CE = LO, V_{IN} = 6 V, no load on OUT pin, V_{BAT} > $V_{BAT(REG)}$, (EN1, EN2) ≠ (HI, HI)				1.5	mA
Power path							
$V_{DO(IN-OUT)}$	V_{IN} – V_{OUT}	V_{IN} = 4.3 V, I_{IN} = 500 mA, V_{BAT} = 4.2 V			200		mV
$V_{DO(BAT-OUT)}$	V_{BAT} – V_{OUT}	I_{OUT} = 500 mA, V_{IN} = 0 V, V_{BAT} = 4 V			165		mV
$V_{O(REG)}$	OUT pin voltage regulation	V_{IN} > V_{OUT} + $V_{DO(IN-OUT)}$	DIO59073/ 73B/ 78	4.3	4.4	4.5	V
			DIO59075	5.4	5.5	5.6	V
I_{IN}max	Maximum input current	EN1 = LO, EN2 = LO			95		mA
		EN1 = HI, EN2 = LO			475		
		EN2 = HI, EN1 = LO		K_{ILIM} / R_{ILIM}			A
K_{ILIM}	Maximum input current factor	I_{LIM} = 500 mA to 1.1 A			750		AΩ
		I_{LIM} = 200 mA to 500 mA			850		
I_{IN}max	Programmable input current limit range	EN2 = HI, EN1 = LO, R_{ILIM} = 8 kΩ to 1.1 kΩ				1100	mA

V_{IN-DPM}	Input voltage threshold when input current is reduced	EN2 = LO, EN1 = X	4.35	4.5	4.63	V
V_{DPPM}	Output voltage threshold when charging current is reduced	DIO59073/ 73B/ 78		$V_{O(REG)}$ - 100 mV		V
		DIO59075		5.3		
$V_{O(SC1)}$	Output short-circuit detection threshold, power-on	V_{IN} > V_{UVLO} and V_{IN} > V_{BAT} + $V_{IN(DT)}$	0.8	0.9	1	V
$V_{O(SC2)}$	Output short-circuit detection threshold, supplement mode V_{BAT} – V_{OUT} > $V_{O(SC2)}$ indicates short-circuit	V_{IN} > V_{UVLO} and V_{IN} > V_{BAT} + $V_{IN(DT)}$		1.2		V
$t_{DGL(SC2)}$	Deglitch time, supplement mode short circuit			250		µs
$t_{REC(SC2)}$	Recovery time, supplement mode short circuit			60		ms
Battery charger						
I_{BAT}	Source current for BAT pin short-circuit detection	V_{BAT} = 1.5 V		7.5		mA
$V_{BAT(SC)}$	BAT pin short-circuit detection threshold	V_{BAT} rising	1.6	1.8	2	V
$V_{BAT(REG)}$	Battery charge voltage	DIO59073/ 73B/ 75/ 78	4.16	4.20	4.23	V
V_{LOWV}	Pre-charge to fast-charge transition threshold	V_{IN} > V_{UVLO} and V_{IN} > V_{BAT} + $V_{IN(DT)}$; DIO59073/ 75/ 78		3.1		V
		V_{IN} > V_{UVLO} and V_{IN} > V_{BAT} + $V_{IN(DT)}$; DIO59073B		2.5		
$t_{DGL1(LOWV)}$	Deglitch time on pre-charge to fast-charge transition			125		µs
$t_{DGL2(LOWV)}$	Deglitch time on fast-charge to pre-charge transition			25		ms
I_{CHG}	Battery fast charge current	/CE = LO, EN1= LO, EN2 = HI, V_{BAT} > V_{LOWV}, V_{IN} = 5 V, I_{IN}max > I_{CHG}, no load on OUT pin, thermal loop and DPPM loop not active	K_{ISET} / R_{ISET}			A
K_{ISET}	Fast charge current factor		800	900	1000	AΩ
I_{PRECHG}	Pre-charge current		K_{PRECHG} / R_{ISET}			A
K_{PRECHG}	Pre-charge current factor			90	110	AΩ
V_{RCH}	Recharge detection threshold	V_{IN} > V_{UVLO} and V_{IN} > V_{BAT} + $V_{IN(DT)}$	$V_{BAT(RE)}$ –140 mV	$V_{BAT(RE)}$ –100 mV	$V_{BAT(RE)}$ –60 mV	V

$t_{DGL(RCH)}$	Deglitch time, recharge threshold detected			62.5		ms
$t_{DGL(NO-IN)}$	Delay time, input power loss to OUT LDO turn-off	V_{BAT} = 3.6 V. Time measured from V_{IN}: 5 V → 3 V 1 μs fall-time		20		ms
Term						
I_{TERM}	Termination comparator detection threshold (internally set)	V_{BAT} > V_{RCH}, t < t_{MAXCH}, V_{IN} = 5 V, DPPM loop and thermal loop not active	0.09× I_{CHG}	0.1× I_{CHG}	0.11× I_{CHG}	A
$I_{BIAS\ (ITERM)}$	Current for external termination-setting resistor (DIO59078 only)	V_{IN} > V_{UVLO} and V_{IN} > V_{BAT} + $V_{IN(DT)}$		30		μA
I_{TERM}	Termination current threshold (externally set) (DIO59078 only)		K_{ITERM} × R_{ITERM} / R_{ISET}			A
K_{ITERM}	K Factor for termination detection threshold (externally set) (DIO59078 only)	USB500 or ISET mode, /CE = LO, V_{BAT} > V_{RCH}, t < t_{MAXCH}, V_{IN} = 5 V, DPPM loop and thermal loop not active	0.02		0.04	A
$t_{DGL(TERM)}$	Deglitch time, termination detected			25		ms
Battery charging timers						
t_{PRECHG}	Pre-charge safety timer value	TMR = floating	1440	1800	2160	s
t_{MAXCHG}	Charge safety timer value	TMR = floating	14400	18000	21600	s
t_{PRECHG}	Pre-charge safety timer value	18 kΩ < R_{TMR} < 72 kΩ	R_{TMR} × K_{TMR}			s
t_{MAXCHG}	Charge safety timer value	18 kΩ < R_{TMR} < 72 kΩ	10 × R_{TMR} × K_{TMR}			s
K_{TMR}	Timer factor		36	48	60	s/kΩ
Battery-pack NTC monitor (1)						
I_{NTC}	NTC bias current	V_{IN} > UVLO and V_{IN} > V_{BAT} + $V_{IN(DT)}$	70		80	μA
V_{HOT}	High temperature trip point	Battery charging, V_{TS} falling	270	300	330	mV
$V_{HYS(HOT)}$	Hysteresis on high trip point	Battery charging, V_{TS} rising from V_{HOT}		30		mV
V_{COLD}	Low temperature trip point	Battery charging, V_{TS} rising	2000	2100	2200	mV
$V_{HYS(COLD)}$	Hysteresis on low trip point	Battery charging, V_{TS} falling from V_{COLD}		300		mV
$t_{DGL(TS)}$	Deglitch time, pack temperature fault detection	TS fault detected to charger disable		50		ms
$V_{DIS(TS)}$	TS function disable threshold	TS unconnected		V_{IN} - 200 mV		mV

Thermal regulation						
$T_{J(REG)}$	Temperature regulation limit			125		°C
$T_{J(OFF)}$	Thermal shutdown temperature	T_J rising		155		°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		°C
Logic levels on EN1, EN2, /CE, SYSOFF, TD						
V_{IL}	Logic LOW input voltage		0		0.4	V
V_{IH}	Logic HIGH input voltage		1.4		6	V
I_{IL}	Input sink current	V_{IL} = 0 V			1	μA
I_{IH}	Input source current	V_{IH} = 1.4 V			10	μA
Logic levels on /PGOOD, /CHG						
V_{OL}	Output LOW voltage	I_{SINK} = 5 mA			0.4	V

Note:

(1) These numbers set trip points of 0°C and 50°C while charging, with 3°C hysteresis on the trip points, with a Vishay Type 2 curve NTC with an R25 of 10 kΩ.

(2) Specifications subject to change without notice.

Typical Application Circuit

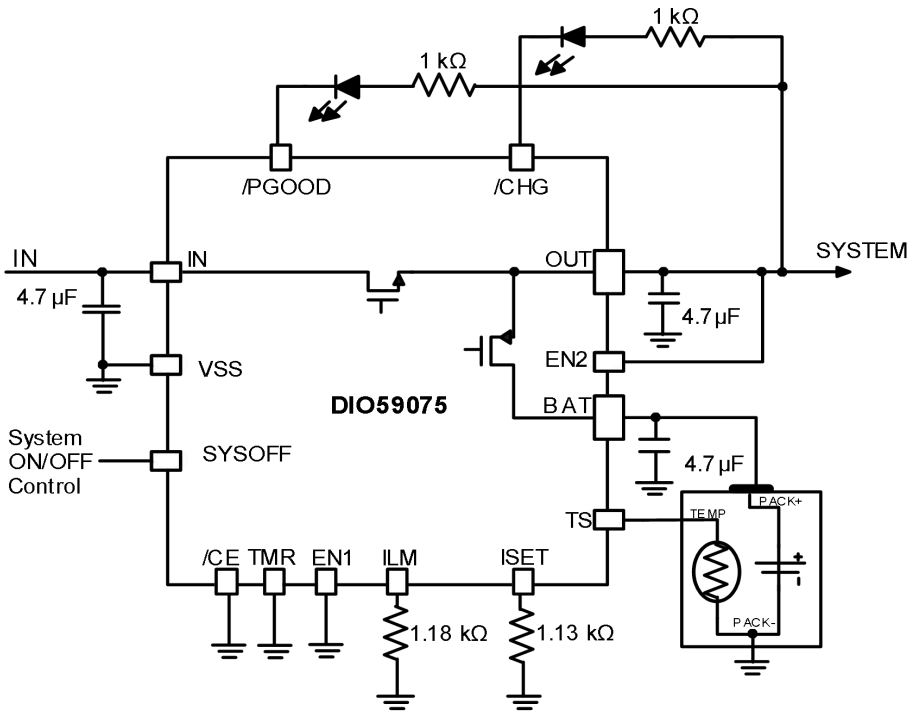


Figure 2. When BAT supply mode $I_{BAT} \leq 1$ A

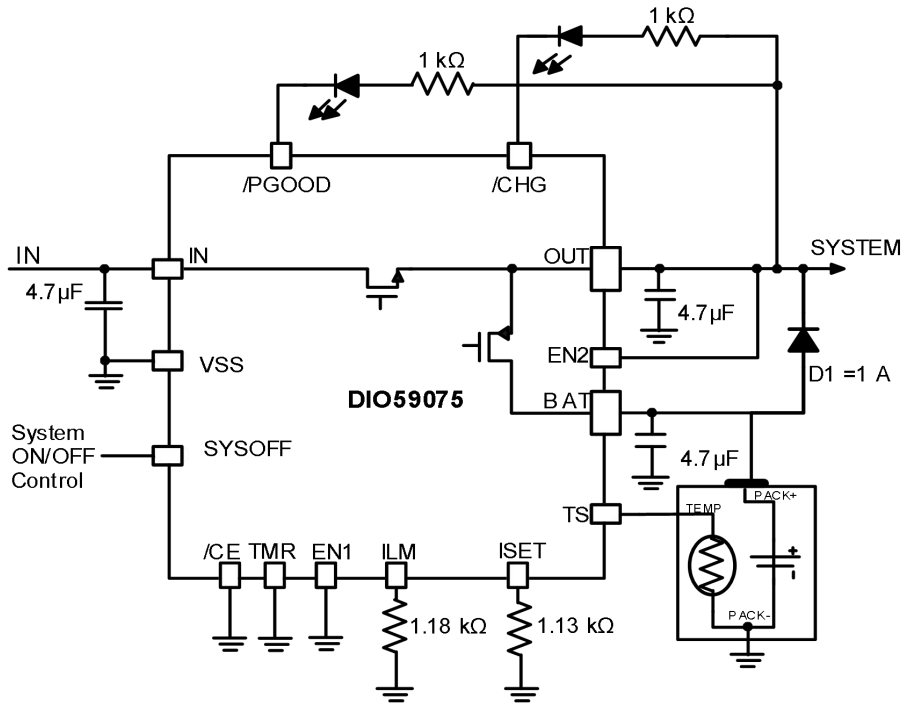


Figure 3. When BAT supply mode 1 A < $I_{BAT} \leq 2$ A

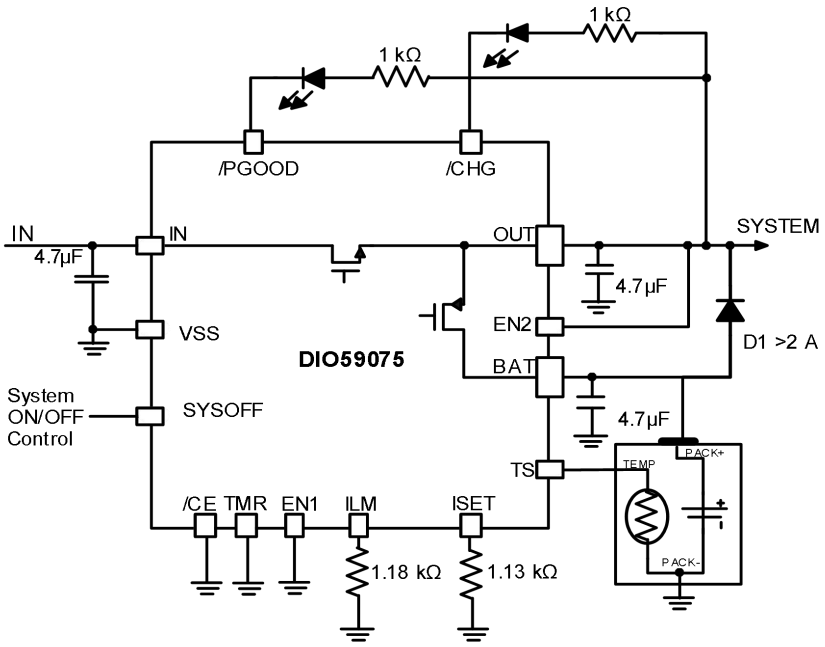


Figure 4. When BAT supply mode 2 A < I_{BAT} ≤ 3 A

Table 2. Diode Selection

I_{BAT}	Forward Current	Reverse Voltage	Forward Pressure Drop	Comment
I_{BAT} ≤ 1 A	NA	NA	NA	NA
1 A < I_{BAT} ≤ 2 A	1 A	>6 V	<0.4 V	D1
2 A < I_{BAT} ≤ 3 A	>2 A	>6 V	<0.4 V	D1

Detailed Description

Overview

The DIO5907x devices are integrated Li-Ion linear chargers and system power path management devices targeted at space-limited portable applications. The device powers the system while simultaneously and independently charging the battery. This feature reduces the number of charge and discharge cycles on the battery, allows for proper charge termination and enables the system to run with a defective or absent battery pack. This feature also allows instant system turn-on even with a totally discharged battery. The input power source for charging the battery and running the system can be an AC adapter or a USB port. The devices feature Dynamic Power Path Management (DPPM), which shares the source current between the system and battery charging, and automatically reduces the charging current if the system load increases. When charging from a USB port, the input dynamic power management (V_{IN-DPM}) circuit reduces the input current if the input voltage falls below a threshold, thus preventing the USB port from crashing. The power-path architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents.

Under voltage lockout (UVLO)

The DIO5907x family remains in power down mode when the input voltage at the IN pin is below the under voltage threshold (UVLO).

During the power down mode the host commands at the control inputs (/CE, EN1 and EN2) are ignored. The Q1 FET connected between IN and OUT pins is off, and the status outputs /CHG and /PGOOD are high impedance. The Q2 FET that connects BAT to OUT is ON. (If SYSOFF is high, Q2 is off). During power down mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on OUT.

Power on

When V_{IN} exceeds the UVLO threshold, the DIO5907x powers up. While V_{IN} is below V_{BAT} + $V_{IN(DT)}$, the host commands at the control inputs (/CE, EN1 and EN2) are ignored. The Q1 FET connected between IN and OUT pins is off, and the status outputs /CHG and /PGOOD are high impedance. The Q2 FET that connects BAT to OUT is ON. (If SYSOFF is high, Q2 is off). During this mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on OUT.

Once V_{IN} rises above V_{BAT} + $V_{IN(DT)}$, /PGOOD is driven low to indicate the valid power status and the /CE, EN1, and EN2 inputs are read. The device enters standby mode if (EN1 = EN2 = HI) or if an input overvoltage condition occurs. In standby mode, Q1 is OFF and Q2 is ON so OUT is connected to the battery input. (If SYSOFF is high, FET Q2 is off). During this mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on OUT.

When the input voltage at IN is within the valid range: V_{IN} > UVLO and V_{IN} > V_{BAT} + $V_{IN(DT)}$ and V_{IN} < V_{OVP}, and the EN1 and EN2 pins indicate that the USB suspend mode is not enabled [(EN1, EN2) ≠ (HI, HI)] all internal timers and other circuit blocks are activated. If no short conditions exists, the device switches on the input FET Q1 with a 100 mA current limit to checks for a short circuit at OUT. When V_{OUT} is above $V_{O(SC1)}$, the FET Q1 switches to the current limit threshold set by EN1, EN2 and R_{ILIM} and the device enters into the normal operation. During normal operation, the system is powered by the input source (Q1 is regulating), and the device continuously monitors the status of /CE, EN1 and EN2 as well as the input voltage conditions.

Overvoltage protection (OVP)

The DIO5907x accepts inputs up to 28 V without damage. Additionally, an overvoltage protection (OVP) circuit is implemented that shuts off the internal LDO and discontinues charging when V_{IN} > V_{OVP} for a period long than $t_{DGL(OVP)}$. When in OVP, the system output (OUT) is connected to the battery and /PGOOD is high impedance. Once the OVP condition is removed, a new power on sequence starts. The safety timers are reset and a new charge cycle will be indicated by the CHG output.

Dynamic power-path management

The DIO5907x features an OUT output that powers the external load connected to the battery. This output is active whenever a source is connected to IN or BAT. The following sections discuss the behavior of OUT with a source connected to IN to charge the battery and a battery source only.

DPPM mode

When the sum of the charging and system load currents exceeds the maximum input current (programmed with EN1, EN2, and ILIM pins), the voltage at OUT decreases. Once the voltage on the OUT pin falls to V_{DPPM}, the DIO5907x enters DPPM mode. In this mode, the charging current is reduced as the OUT current increases in order to maintain the system output. Battery termination is disabled while in DPPM mode.

Battery charging

Set /CE low to initiate battery charging. First, the device checks for a short-circuit on the BAT pin by sourcing $I_{BAT(SC)}$ to the battery and monitoring the voltage. When the BAT voltage exceeds $V_{BAT(SC)}$, the battery charging continues. The battery is charged in three phases: conditioning pre-charge, constant current fast charge (current regulation) and a constant voltage tapering (voltage regulation). In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.

In the pre-charge phase, the battery is charged at with the pre-charge current (I_{PRECHG}). Once the battery voltage crosses the V_{LOWV} threshold, the battery is charged with the fast-charge current (I_{CHG}). As the battery voltage reaches $V_{BAT(REG)}$, the battery is held at a constant voltage of $V_{BAT(REG)}$ and the charge current tapers off as the battery approaches full charge. When the battery current reaches I_{TERM}, the /CHG pin indicates charging done by going high-impedance.

Note that termination detection is disabled whenever the charge rate is reduced because of the actions of the thermal loop, the DPPM loop or the V_{IN-DPM} loop.

The value of the fast-charge current is set by the resistor connected from the ISET pin to VSS, and is given by the equation (1):

$$I_{CHG} = K_{ISET}/R_{ISET} \quad (1)$$

The charge current limit is adjustable up to 1.1 A. The valid resistor range is 590 Ω to 8.9 kΩ. If I_{CHG} is programmed as greater than the input current limit, the battery will not charge at the rate of I_{CHG}, but at the slower rate of $I_{IN(MAX)}$ (minus the load current on the OUT pin, if any). In this case, the charger timers will be proportionately slowed down.

Termination disable (TD input, DIO59073/ 73B)

The DIO59073 contain a TD input that allows termination to be enabled/disabled. Connect TD to a logic high to disable charge termination. When termination is disabled, the device goes through the pre charge, fast-charge and CV phases, then remains in the CV phase. During the CV phase, the charger maintains the output voltage

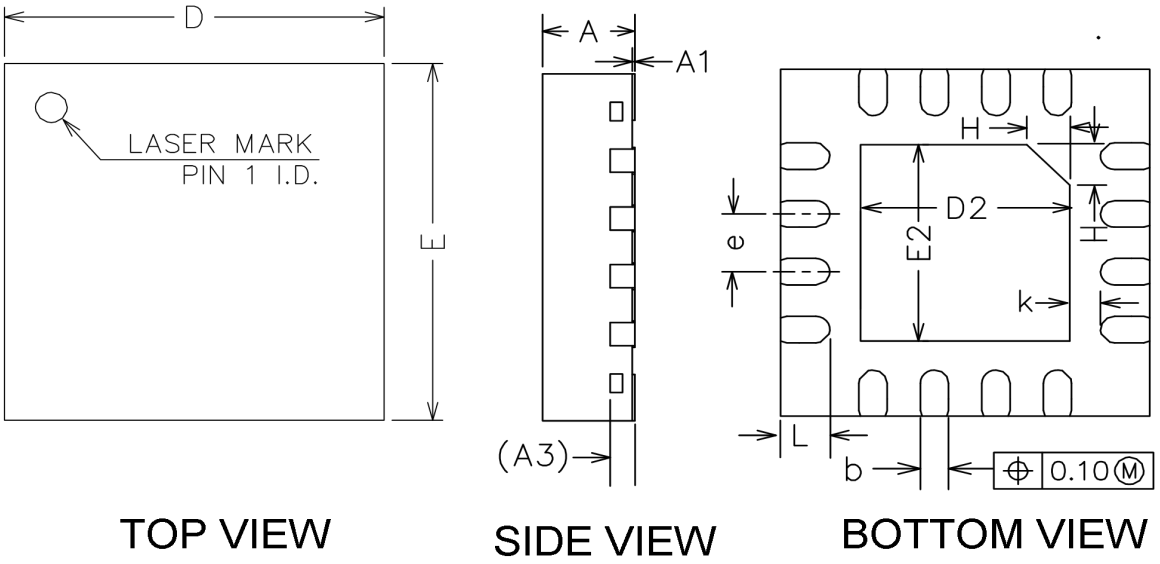
at BAT equal to $V_{BAT(REG)}$, and charging current does not terminate. The charge current is set by I_{CHG} or I_{INmax}, whichever is less. Battery detection is not performed. The /CHG output is high impedance once the current falls below I_{TERM} and does not go low until the input power or /CE are toggled. When termination is disabled, the pre-charge and fast-charge safety timers are also disabled. Battery pack temperature sensing (TS pin functionality) is disabled if the TD pin is high and the TS pin is unconnected or pulled up to V_{IN}.

Battery pack temperature monitoring

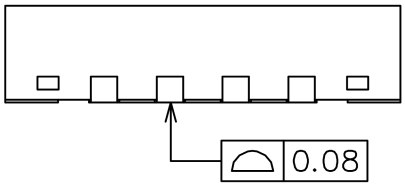
The DIO5907x features an external battery pack temperature monitoring input. The TS input connects to the NTC thermistor in the battery pack to monitor battery temperature and prevent dangerous over-temperature conditions. During charging, I_{NTC} is sourced to TS and the voltage at TS is continuously monitored. If, at any time, the voltage at TS is outside of the operating range (V_{COLD} to V_{HOT}), charging is suspended. The timers maintain their values but suspend counting. When the voltage measured at TS returns to within the operation window, charging is resumed and the timers continue counting. When charging is suspended due to a battery pack temperature fault, the /CHG pin remains low and continues to indicate charging.

For applications that do not require the TS monitoring function, connect a 10 kΩ resistor from TS to VSS to set the TS voltage at a valid level and maintain charging.

Physical Dimensions: QFN3*3-16



TOP VIEW SIDE VIEW BOTTOM VIEW



SIDE VIEW

Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20 REF	
b	0.20	0.25	0.30
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D2	1.60	1.70	1.75
E2	1.60	1.70	1.75
e	0.40	0.50	0.60
H		0.30 REF	
K	0.15	-	-
L	0.35	0.40	0.45

CONTACT US

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