DIO5060A/B

Standalone 1-Cell 600 mA Linear Battery Charger with Power Path, 1 mA Termination, and Battery Leakage below 1 uA

Features

- Input overvoltage protection with 6.5 V
- Charge status indicator
- Charge current accuracy: 10%
- Charge voltage accuracy: 0.7%
- Battery supplement mode
- Supports from 10 mA up to 600 mA charge current with current monitoring output (ISET)
- Programmable pre-charge current by resistor
- Programmable ITERM charge current by resistor
- Pre-charge for 30 minutes safety timing
- Fast-charge for 6 hours safety timing
- Under 1 uA leakage off the battery, when no input power attached
- SEL1 and SEL2 pins control 0.5C, 1C, 2C of fast-charge (DIO5060A)
- 50 μA standby current into IN pin after full charge

Applications

- Smart phones
- Portable media players
- Portable navigation devices
- Low-power handheld device

Descriptions

The DIO5060A/B series are integrated Li-Ion linear chargers and system power path management devices that are targeted at space-limited portable applications. The charger accepts an input voltage of up to 25 V but is disabled when the input voltage exceeds the OVP threshold, typically 6.5 V, to prevent excessive power dissipation. The 25 V rating eliminates the overvoltage protection circuit required in a low input-voltage charger. The input voltage range with input overvoltage protection supports unregulated adapters.

The DIO5060A/B features dynamic power path management (DPPM) that powers the system while simultaneously and independently charging the battery. The DPPM circuit reduces the charge current when the input current limit causes the system output to fall to the DPPM threshold; thus, supplying the system load at all times when monitoring the charge current separately. This feature reduces the number of charge and discharge cycles on the battery, allows for proper charge termination, and enables the system to run with a defective or absent battery pack.

Ordering Information

Order Part Number	Top Marking	RoHS	T_A	Package	
DIO5060A420CN10	FVAA	Green	-40 to 85°C	DFN2*2-10	Tape & Reel, 3000
DIO5060A435CN10	FVAB	Green	-40 to 85°C	DFN2*2-10	Tape & Reel, 3000
DIO5060A440CN10	FVAC	Green	-40 to 85°C	DFN2*2-10	Tape & Reel, 3000
DIO5060A445CN10	FVAD	Green	-40 to 85°C	DFN2*2-10	Tape & Reel, 3000
DIO5060A447CN10	FVAE	Green	-40 to 85°C	DFN2*2-10	Tape & Reel, 3000
DIO5060B420CN10	FVBA	Green	-40 to 85°C	DFN2*2-10	Tape & Reel, 3000
DIO5060B435CN10	FVBB	Green	-40 to 85°C	DFN2*2-10	Tape & Reel, 3000
DIO5060B440CN10	FVBC	Green	-40 to 85°C	DFN2*2-10	Tape & Reel, 3000
DIO5060B445CN10	FVBD	Green	-40 to 85°C	DFN2*2-10	Tape & Reel, 3000
DIO5060B447CN10	FVBE	Green	-40 to 85°C	DFN2*2-10	Tape & Reel, 3000

Pin Assignment

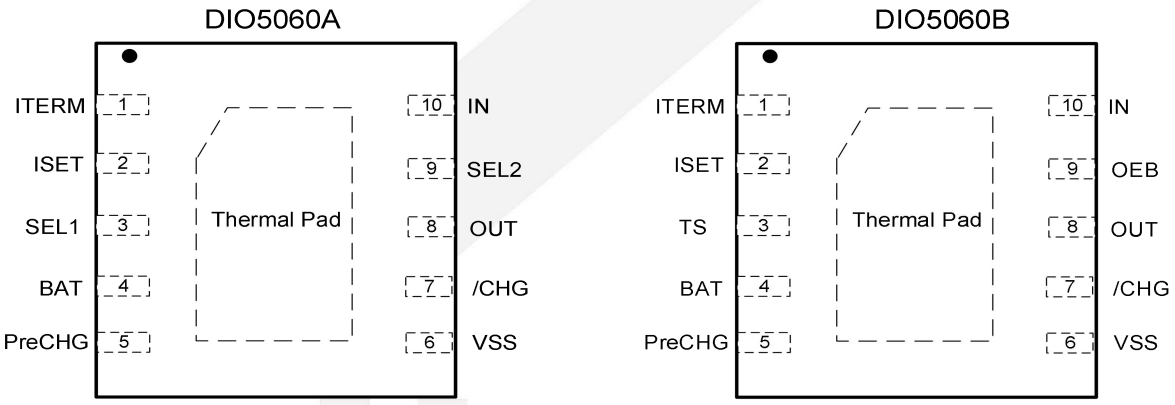


Figure 1. Top View

Pin Descriptions

Name	I/O	Description
TS	I	External NTC thermistor input. Connect the TS input to the NTC thermistor in the battery pack. TS monitors a 10 kΩ NTC thermistor. For applications that do not use the TS function, connect a 10 kΩ fixed resistor from TS to VSS to maintain a valid voltage level on TS. (DIO5060B)
BAT	I/O	Charger power stage output and battery voltage sense input. Connect BAT to the positive terminal of the battery. Bypass BAT to VSS with a 4.7 µF to 47 µF ceramic capacitor.
VSS	–	Ground. Connect to the thermal pad and to the ground rail of the circuit. VSS pin must be connected to ground at all times.
/CHG	O	Open-drain charging status indication output. /CHG pulls to VSS when the battery is charging. /CHG is high impedance when charging is complete and when charger is disabled. Connect

		/CHG to the desired logic voltage rail using a 1 kΩ to 100 kΩ resistor, or use with an LED for visual indication.
OUT	O	System supply output. OUT provides a regulated output when the input is below the OVP threshold and above the regulation voltage. Connect OUT to the system load. Bypass OUT to VSS with a 4.7 μF to 47 μF ceramic capacitor.
PreCHG	O	Pre-charge current programming input. Connect a 0.5 kΩ to 51 kΩ resistor from PreCHG to VSS to program the pre-charge current level.
OEB	I	OEB works normally at low level. When VBUS is powered on, it turns off charger function at high level. (DIO5060B)
IN	I	Input power connection. Connect IN to the external DC supply (AC adapter or USB port). The input operating range is 4.35 V to 6.5 V. The input can accept voltages up to 25 V without damage but operation is suspended. Connect bypass capacitor 10 μF to VSS.
ITERM	I	Termination current programming input. Connect a 0.5 kΩ to 51 kΩ resistor from ITERM to VSS to program the termination current.
ISET	I/O	Fast charge current programming input. Connect a 0.1 kΩ to 6.8 kΩ resistor from ISET to VSS to program the fast charge current level. Charging is disabled if ISET is left unconnected. When charging, the voltage at ISET reflects the actual charging current and can be used to monitor charge current.
SEL1	I	Choose charging current. (DIO5060A)
SEL2	I	Choose charging current. (DIO5060A)
Thermal Pad	–	An internal electrical connection exists between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device.

Truth Table

The truth table is for charging current selection of DIO5060A.

SEL1	SEL2	I_{charge}
0	0	1*C
0	1	2*C
1	0	0.5*C
1	1	0

Typical Application Circuit

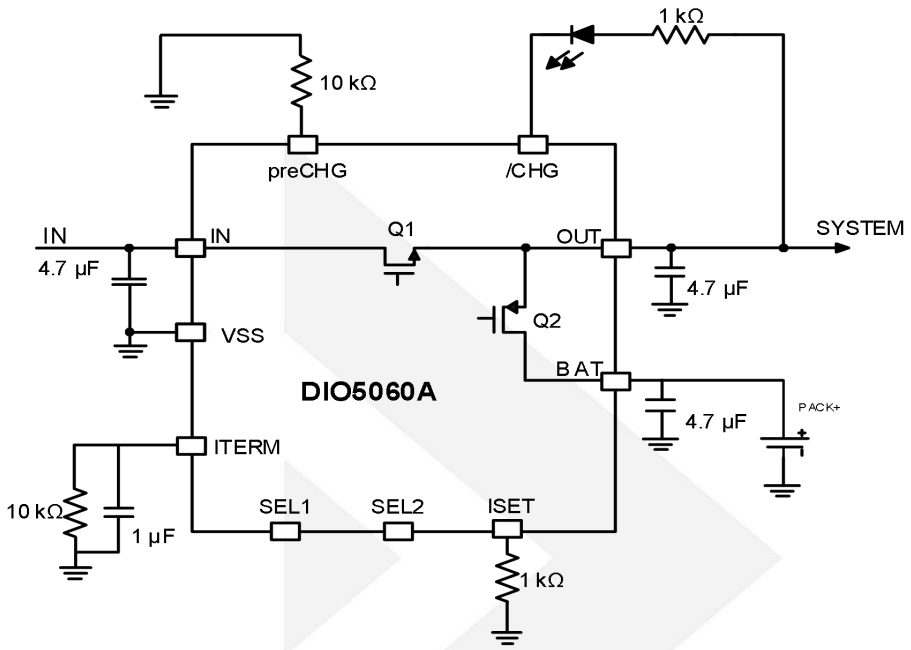


Figure 2. Application for DIO5060A

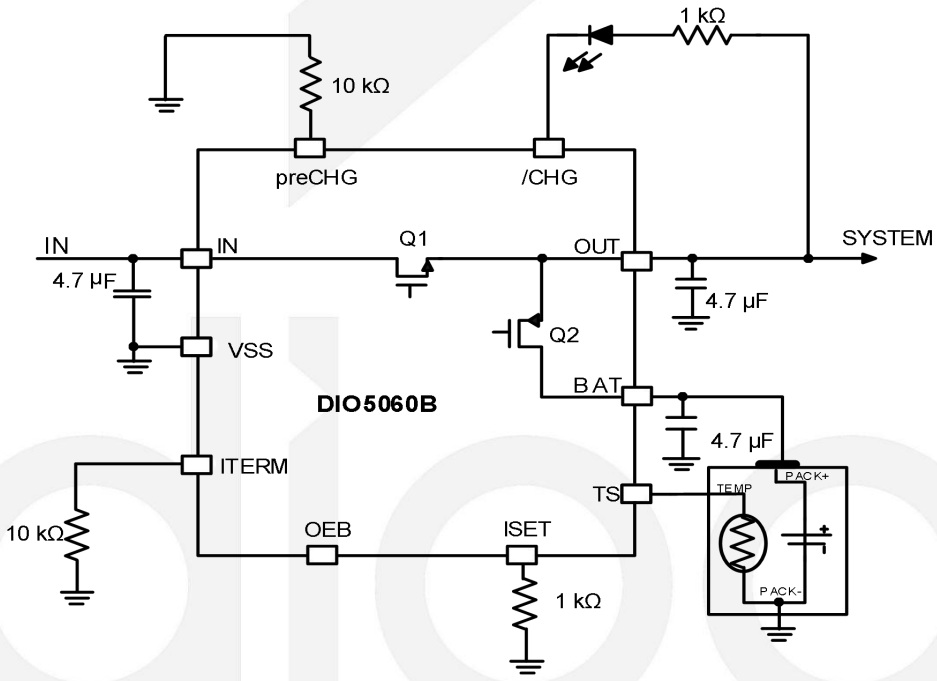


Figure 3. Application for DIO5060B

Absolute Maximum Ratings

Stresses beyond those listed under the Absolute Maximum Rating table may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter			Min	Max	Unit
V_I	Input voltage	IN (with respect to VSS)	-0.3	28	V
		BAT (with respect to VSS)	-0.3	5	V
		OUT, ISET, /CHG, ITERM (with respect to VSS)	-0.3	7	V
I_I	Input current	IN		600	mA
I_O	Output current (continuous)	OUT		1	A
		BAT (discharge mode)		1	A
		BAT (charging mode)		600	mA
	Output sink current	/CHG		15	mA
T_J	Junction temperature		-40	150	°C
T_{STG}	Storage temperature		-65	150	°C
ESD	HBM		-4000	4000	V

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not recommend exceeding them or designing to absolute maximum ratings.

Parameter		Min	Max	Unit
V_I	IN voltage range	4.35	25	V
	IN operating voltage range	4.35	6.5	V
I_{IN}	Input current, IN pin		600	mA
I_{OUT}	Current, OUT pin		1	A
I_{BAT}	Current, BAT pin (discharging)		1	A
I_{CHG}	Current, BAT pin (charging)		600	mA
T_J	Junction temperature	-40	125	°C
R_{preCHG}	Pre-charge current programming resistor	0.5	51	kΩ
R_{TERM}	Maximum input current programming resistor	0.5	51	kΩ
R_{ISET}	Fast-charge current programming resistor (1)	0.1	6.8	kΩ
θ_{JA}	Package thermal resistance	63.5		°C/W

Note:

(1) Use a 1% tolerance resistor for R_{ISET} to avoid issues with the R_{ISET} short test when using the maximum charge current setting.

Electrical Characteristics

Over junction temperature range (0° ≤ T_J ≤ 125°C) and the recommended supply voltage range (unless otherwise noted).

Parameter		Test Conditions	Min	Typ	Max	Unit
Input						
UVLO	Undervoltage lock-out	V_{IN}: 0 V → 4 V		3.0	3.2	V
V_{OVP}	Input overvoltage protection threshold	V_{IN}: 5 V → 7 V	6.4	6.5	6.8	V
V_{hys}(1)	Hysteresis on OVP	V_{IN}: 7 V → 5 V		200		mV
$t_{DGL(OVP)}$(1)	Input overvoltage blanking time (OVP fault deglitch)			10		μs
Quiescent current						
$I_{BATSTBY}$	Standby current into BAT pin	Input power not detected, No load on OUT pin, T_J = 25°C			1.0	μA
I_{IN}	Standby current into IN pin	V_{IN} = 5.5V, T_J = 85°C charge done， No load on OUT pin		50	120	μA
I_{CC}(1)	Active supply current, IN pin	V_{IN} = 6 V, no load on OUT pin, V_{BAT} > $V_{BAT(REG)}$			300	μA
Power path						
$V_{DO(IN-OUT)}$(1)	V_{IN} – V_{OUT}	V_{IN} = 5 V, I_{IN} = 100 mA, V_{BAT} = 4.4 V		40		mV
$V_{DO(BAT-OUT)}$(1)	V_{BAT} – V_{OUT}	I_{OUT} = 100 mA, V_{IN} = 0 V, V_{BAT} > 3 V		30		mV
$V_{O(REG)}$	OUT pin voltage regulation	V_{IN} > V_{OUT} + $V_{DO(IN-OUT)}$	4.4	4.6	4.8	V
I_{IN}max(1)	Input current limit range		700			mA
V_{IN-DPM}(1)	Input voltage threshold when input current is reduced			4.5		V
V_{DPPM}(1)	Output voltage threshold when charging current is reduced	V_{OUT} = 4.6 V		4.5		V
V_{BSUP1}(1)	Enter battery supplement mode	V_{BAT} = 3.6 V, R_{LOAD} = 10 Ω → 2 Ω	V_{OUT} ≤ V_{BAT} – 60 mV			V
V_{BSUP2}(1)	Exit battery supplement mode	V_{BAT} = 3.6 V, R_{LOAD} = 2 Ω → 10 Ω	V_{OUT} ≥ V_{BAT} – 50 mV			V
$V_{O(SC1)}$(1)	Output short-circuit detection threshold, power-on	V_{IN} > V_{UVLO} and V_{IN} > V_{BAT} + $V_{IN(DT)}$	0.8	0.9	1	V
$V_{O(SC2)}$(1)	Output short-circuit detection threshold,	V_{IN} > V_{UVLO} and V_{IN} > V_{BAT} + $V_{IN(DT)}$		260		mV

	supplement mode $V_{BAT} – V_{OUT} > V_{O(SC2)}$ indicates short-circuit						
$t_{DGL(SC2)}$(1)	Deglitch time, supplement mode short circuit				80		µs
$t_{REC(SC2)}$(1)	Recovery time, supplement mode short circuit				28		ms
Battery charger							
I_{BAT}(1)	Source current for BAT pin short-circuit detection	V_{BAT} = 0.5 V			1.2		mA
$V_{BAT(REG)}$	Battery regulation voltage	V_{IN} = 5 V	DIO5060_420	4.17	4.20	4.23	V
			DIO5060_435	4.30	4.35	4.39	V
			DIO5060_440	4.37	4.4	4.43	V
			DIO5060_445	4.42	4.45	4.48	V
$V_{BAT(SC)}$	BAT pin short-circuit detection threshold	V_{BAT} rising		0.7	0.8	0.9	V
V_{LOWV}	Pre-charge to fast-charge transition threshold	$V_{IN} > V_{UVLO}$ and $V_{IN} > V_{BAT} + V_{IN(DT)}$		2.4	2.5	2.6	V
$t_{DGL1(LOWV)}$(1)	Deglitch time on pre-charge to fast-charge transition				130		µs
$t_{DGL2(LOWV)}$(1)	Deglitch time on fast-charge to pre-charge transition				25		ms
I_{CHG}(1)	Battery fast charge current range	R_{ISET} = 1 kΩ			70		mA
	Battery fast charge current	$V_{BAT} > V_{LOWV}$, V_{IN} = 5V, $I_{IN}max > I_{CHG}$, no load on OUT pin and thermal loop not active		K_{ISET} / R_{ISET}			A
K_{ISET}	Fast charge current factor	R_{ISET} = 1 kΩ		60		77	AΩ
I_{PRECHG}(1)	Pre-charge current	$V_{BAT(S)} < V_{BAT} < V_{LOW}$, V_{IN} = 5 V, $I_{IN}max > I_{CHG}$, no load on OUT pin and thermal loop not active		K_{IPre}/R_{IPre}			A
K_{PRECHG}(1)	Pre-charge current factor	R_{PreCHG} = 1 kΩ		45		60	AΩ
V_{RCH}(1)	Recharge detection threshold	$V_{IN} > V_{UVLO}$ and $V_{IN} > V_{BAT} + V_{IN(DT)}$		$V_{BAT(RE)}$ –200mV	$V_{BAT(RE)}$ –150mV	$V_{BAT(RE)}$ –100mV	V
$t_{DGL(RCH)}$(1)	Deglitch time, recharge threshold detected				60		ms

$t_{DGL(NO-IN)}$(1)	Delay time, input power loss to OUT LDO turn-off	V_{BAT} = 3.6 V. Time measured from V_{IN}: 5 V → 3 V 1 µs fall-time		20		ms
TERM						
I_{TERM}(1)	Termination comparator detection threshold (internally set)		K_{ITERM} / R_{ITERM}			A
K_{ITERM}(1)		R_{ITERM}= 1 kΩ	45		60	AΩ
Battery-pack NTC monitor, TS terminal						
$I_{NTC-10k}$	NTC bias current	V_{TS} = 0.3 V	48	50	52	µA
$V_{TTDM(TS)}$(1)	Termination and timer disable mode Threshold – Enter	V_{TS}: 1.5 V → 4 V; Timer held in reset	3.6	3.7	3.8	V
$V_{HYS-TTDM(TS)}$(1)	Hysteresis			100		mV
$V_{TS-0°C}$(1)	Low temperature CHG Pending	Low temp charging to pending; V_{TS}: 1 V → 1.5 V	1.38			V
$V_{HYS-0°C}$(1)	Hysteresis at 0°C	Charge pending to low temp charging; V_{TS}: 1.5 V → 1 V		60		mV
$V_{TS-10°C}$(1)	Low temperature, half charge	Normal charging to low temp charging; V_{TS}: 0.5 V → 1 V		920		mV
$V_{HYS-10°C}$(1)	Hysteresis at 10°C	Low temp charging to normal CHG; V_{TS}: 1 V → 0.5 V		20		mV
$V_{TS-45°C}$(1)	High temperature at 4.1 V	Normal charging to high temp CHG; V_{TS}: 0.5 V → 0.2 V			245	mV
$V_{HYS-45°C}$(1)	Hysteresis at 45°C	High temp charging to normal CHG; V_{TS}: 0.2 V → 0.5 V		10		mV
Thermal regulation						
$T_{J(REG)}$(1)	Temperature regulation limit			125		°C
$T_{J(OFF)}$(1)	Thermal shutdown temperature	T_J rising		150		°C
$T_{J(OFF-HYS)}$(1)	Thermal shutdown hysteresis			20		°C
Logic levels on OEB						
V_{IH}	Logic high input voltage		1.4			V
V_{IL}	Logic low input voltage				0.4	V
Logic levels on /CHG						
V_{OL}(1)	Output low voltage	I_{SINK} = 5 mA			0.4	V
$R_{SEL1\_Pull\ Down}$(1)	SEL1 pin internal pull-down resistance			270		kΩ
$R_{SEL2\_Pull\ Down}$(1)	SEL2 pin internal			270		kΩ

	pull-down resistance					
$R_{OEB\_Pull\ Down}$(1)	OEB pin internal pull-down resistance			270		kΩ

Note:

(1) Guaranteed by design.

(2) Specifications subject to change without notice.

Detailed Description

Overview

The DIO5060A/B devices are integrated Li-Ion linear chargers and system power path management devices targeted at space-limited portable applications. The device powers the system and charges the battery simultaneously and independently. This feature reduces the number of charge and discharge cycles on the battery, allows for proper charge termination, and enables the system to run with a defective or absent battery pack. This feature also allows instant system turn-on even with a totally discharged battery. The input power source for charging the battery and running the system can be an AC adapter or a USB port. The devices feature dynamic power path management (DPPM), which shares the source current between the system and battery charging, and automatically reduces the charging current if the system load increases. When charging from a USB port, the input dynamic power management (V_{IN-DPM}) circuit reduces the input current if the input voltage falls below a threshold, thus preventing the USB port from crashing. The power-path architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents.

Undervoltage lockout (UVLO)

The DIO5060A/B family remains in power-down mode when the input voltage at the IN pin is below the undervoltage lockout threshold.
The Q1 FET connected between IN and OUT pins is off and the status outputs /CHG is high impedance. The Q2 FET that connects BAT to OUT is ON. During power-down mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on OUT.

Power on

When the input voltage at IN is within the valid range: V_{IN} > UVLO and V_{IN} < V_{OVP}, all internal timers and other circuit blocks are activated. If OUT no short conditions exists, the device switches on the input FET Q1 with a 100 mA current limit. When V_{OUT} is above $V_{O(SC1)}$, the FET Q1 switches to the current limit threshold set by I_{IN}max. and the device enters into the normal operation. During normal operation, the system is powered by the input source (Q1 is regulating).

Overvoltage protection (OVP)

The DIO5060A/B accepts inputs up to 25 V without damage. Additionally, an overvoltage protection (OVP) circuit is implemented that shuts off the internal LDO and discontinues charging when V_{IN} > V_{OVP} for a period longer than $t_{DGL(OVP)}$. As soon as the OVP condition is removed, a new power-on sequence starts (see Power on). The safety timers are reset and a new charge cycle will be indicated by the CHG output.

Dynamic power-path management

The DIO5060A/B features an OUT output that powers the external load connected to the battery. This output is active whenever a source is connected to IN or BAT. The following sections discuss the behavior of OUT with a source connected to IN to charge the battery and a battery source only.

Input source connected

The OUT output is regulated to a fixed voltage ($V_{O(REG)}$). This allows for proper startup of the system load even with a discharged battery. The current into IN is shared between charging the battery and powering the system load at OUT.

Input DPM mode (V_{IN}-DPM)

The DIO5060A/B utilizes the V_{IN}-DPM mode for operation from current-limited USB ports. When the configuration defaults to USB500 mode, the input voltage is monitored. If V_{IN} falls to V_{IN}-DPM, the input current limit is reduced to prevent the input voltage from falling further. This prevents the DIO5060A/B from crashing poorly designed or incorrectly configured USB sources. Figure 4 shows the V_{IN}-DPM behavior to a current limited source. In this figure, the input source has a 400 mA current limit and the device is in USB500 mode.

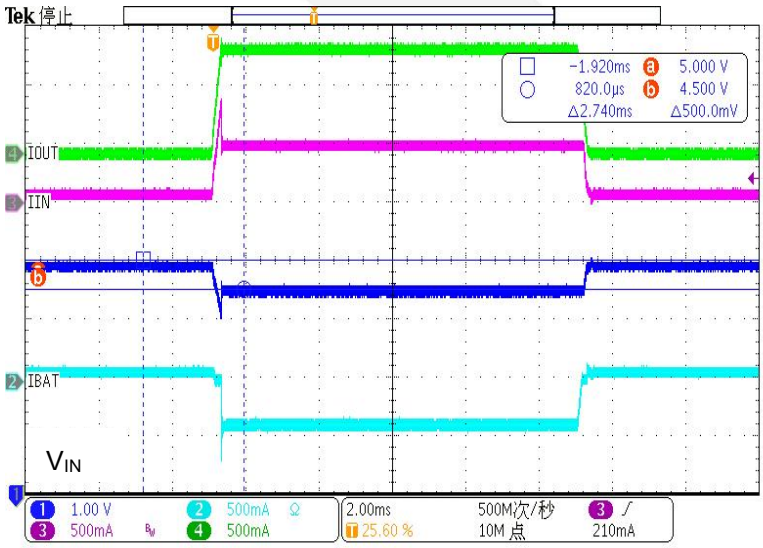


Figure 4. V_{IN}-DPM Waveform

DPPM mode

When the sum of the charging and system load currents exceeds the maximum input current, the voltage at OUT decreases. As soon as the voltage on the OUT pin falls to VDPPM, the DIO5060A/B enters DPPM mode. In this mode, the charging current is reduced as the OUT current increases in order to maintain the system output.

Battery supplement mode

If the charging current falls to zero and the system load current increases beyond the input current limit, the voltage at OUT reduces further. When the OUT voltage drops below the V_{BSUP1} threshold, the battery supplements the system load. The battery stops supplementing the system load when the voltage at OUT rises above the V_{BSUP2} threshold.

During supplement mode, the battery supplement current is not regulated (BAT-FET is fully on). However, there is a short circuit protection circuit built in. If during battery supplement mode, the voltage at OUT drops $V_{O(SC2)}$ below the BAT voltage. The OUT output is turned off if the overload exists after $t_{DGL(SC2)}$. The short circuit recovery timer then starts counting. After $t_{REC(SC2)}$, OUT turns on and attempts to restart. If the short circuit remains, OUT is turned off and the counter restarts. Battery termination is disabled in supplement mode.

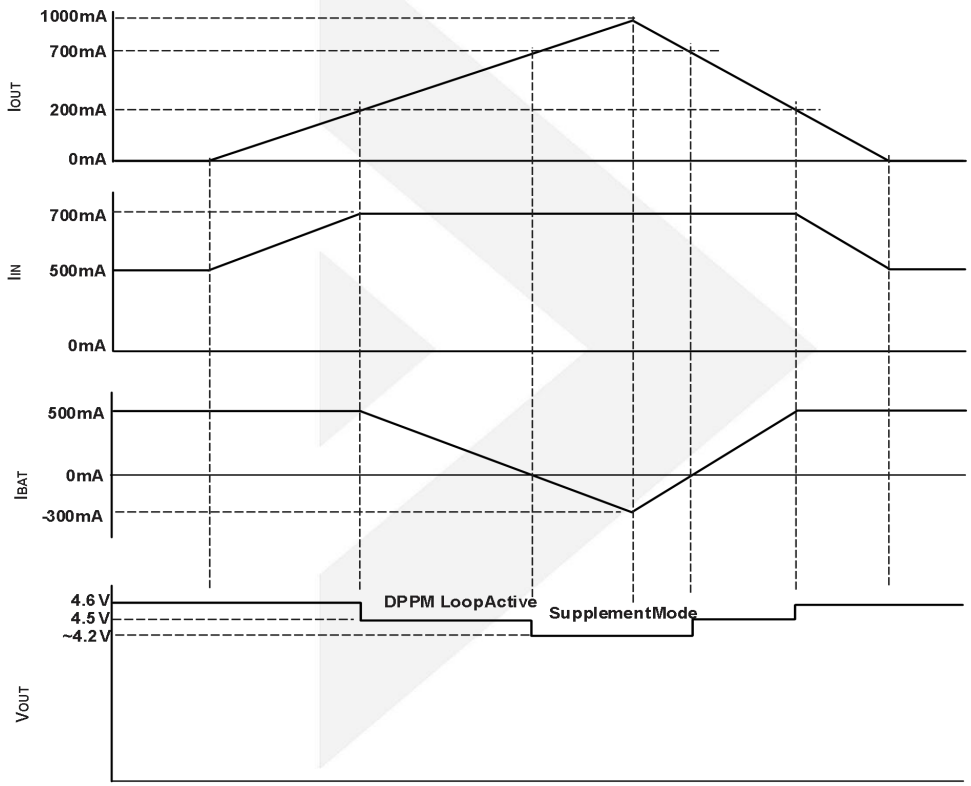


Figure 5. DIO5060A/B DPPM and Battery Supplement Modes (V_{OREG} = V_{BAT} + 225 mV, V_{BAT} = 4.4 V)

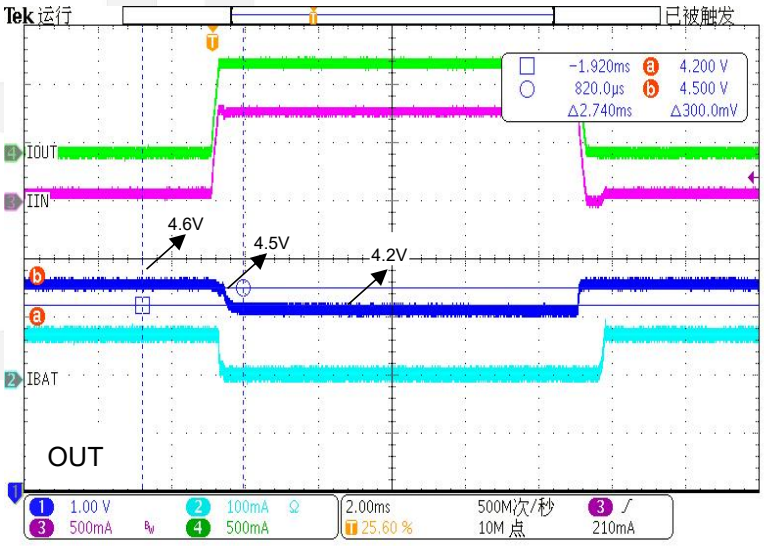


Figure 6. V_{OUT}-DPPM

Input source not connected

When no source is connected to the IN input, OUT is powered strictly from the battery. During this mode the current into OUT is not regulated, similar to Battery Supplement Mode, however the short circuit circuitry is active. If the OUT voltage falls below the BAT voltage by 260 mV for longer than $t_{DGL(SC2)}$, OUT is turned off. The short circuit recovery timer then starts counting. After $t_{REC(SC2)}$, OUT turns on and attempts to restart. If the short circuit remains, OUT is turned off and the counter restarts. This ON/OFF cycle continues until the overload condition is removed.

Battery charging

First, the device checks for a short-circuit on the BAT pin by sourcing $I_{BAT(SC)}$ to the battery and monitoring the voltage. When the BAT voltage exceeds $V_{BAT(SC)}$, the battery charging continues. The battery is charged in three phases: conditioning pre-charge, constant current fast charge (current regulation) and a constant voltage tapering (voltage regulation). In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.

In the pre-charge phase, the battery is charged at with the pre-charge current (I_{PRECHG}). As soon as the battery voltage crosses the V_{LOWV} threshold, the battery is charged with the fast-charge current (I_{CHG}). As the battery voltage reaches $V_{BAT(REG)}$, the battery is held at a constant voltage of $V_{BAT(REG)}$ and the charge current tapers off as the battery approaches full charge. When the battery current reaches I_{TERM}, the /CHG pin indicates charging done by going high-impedance.

The value of the pre-charge current is set by the resistor (0.5 kΩ to 51 kΩ) connected from the PreCHG pin to VSS, and is given by the table:

R_{PreCHG} (kΩ)	I_{PreCHG} (mA)
0.5	101.92
1	51.21
2.5	20.58
5.11	10.11
10	5.21
51	1.01

The minimum termination current is 1 mA, set by a resistor (0.5 kΩ to 51 kΩ), and is given by the table:

R_{TERM} (kΩ)	I_{TERM} (mA)
0.5	100.89
1	51.28
2.5	21.09
5.11	10.45
10	5.46
51	1.10

The valid resistor range is 0.1 kΩ to 6.8 kΩ and is given by the table:

R_{ISET} (kΩ)	I_{CHG} (mA)
0.13	485.11
0.17	385.90
0.25	271.08
0.5	139.32
1	70.94
2	35.59
2.5	28.49

If I_{CHG} is programmed as greater than the input current limit, the battery will not charge at the rate of I_{CHG}, but at the slower rate of $I_{IN(MAX)}$.

Battery detection and recharge

As soon as a charge cycle is completed, the battery voltage is monitored. When the battery voltage falls below V_{RCH}, the battery enters another charge cycle.

Status indicators (/CHG)

The charge cycle after power-up, OEB going low, or exiting OVP is indicated with the CHG pin on (low - LED on), whereas all refresh (subsequent) charges will result in the /CHG pin off (open - LED off). In addition, the /CHG signals timer faults by flashing at approximately 1.2 Hz.

Charge State	CHG Output
Charging	Low (for first charge cycle)
Charging suspended by thermal loop	
Safety timers expired	Flashing at 1.2 Hz
Charging done	High-impedance
Recharging after termination	
IC disabled or no valid input power	

Thermal regulation and thermal shutdown

The DIO5060A/B contains a thermal regulation loop that monitors the die temperature. If the temperature exceeds $T_{J(REG)}$, the device automatically reduces the charging current to prevent the die temperature from increasing further. In some cases, the die temperature continues to rise despite the operation of the thermal loop, particularly under high VIN and heavy OUT system load conditions. Under these conditions, if the die temperature increases to $T_{J(OFF)}$, the input FET Q1 is turned OFF. FET Q2 is turned ON to ensure that the battery still powers the load on OUT. As soon as the device die temperature cools by $T_{J(OFF-HYS)}$, the input FET Q1 is turned on and the device returns to thermal regulation. Continuous over temperature conditions result in a hiccup mode.

Note that this feature monitors the die temperature of the DIO5060A/B. This is not synonymous with ambient temperature. Self heating exists due to the power dissipated in the IC because of the linear nature of the battery charging algorithm and the LDO associated with OUT.

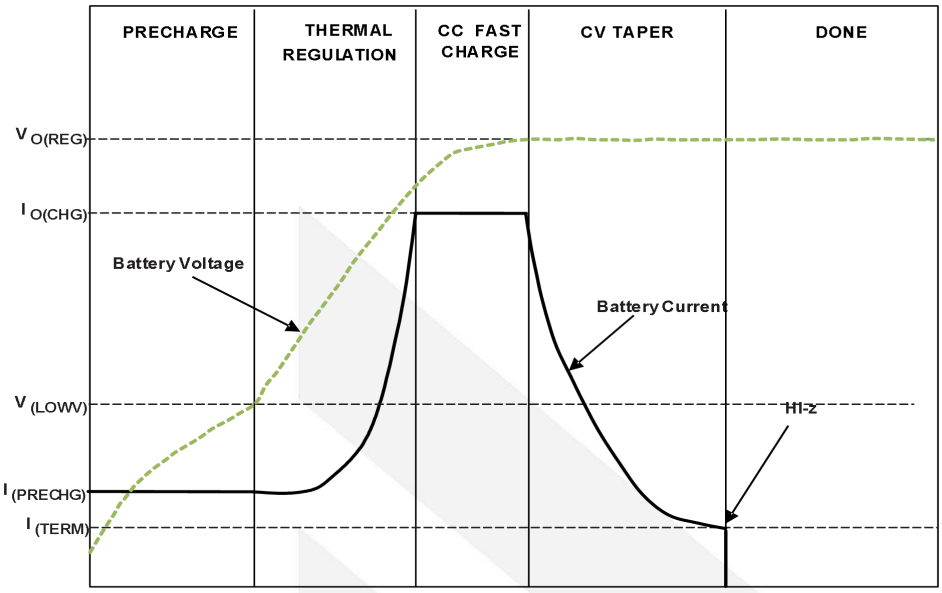


Figure 7. Charge Cycle Modified by Thermal Loop

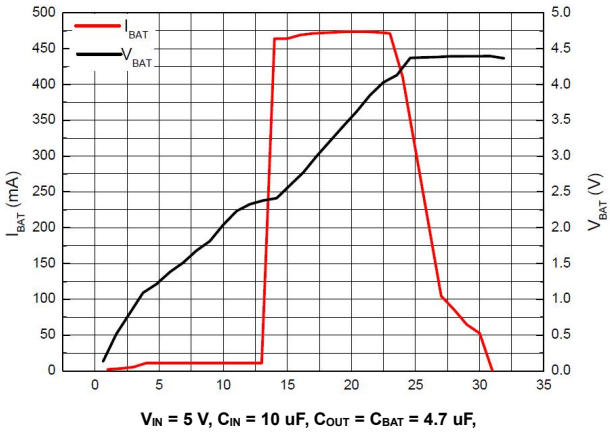
TS

The TS function is designed to follow the new JEITA temperature standard for Li-Ion and Li-Pol batteries. There are now three thresholds 45°C, 10°C, and 0°C for DIO5060B.

Normal operation occurs between 10°C and 45°C. If between 0°C and 10°C the charge current level is 0.2*I_{BAT} and if less than 0°C or more than 45°C, the charging is disabled.

The TS feature is implemented by using an internal 50 µA current source to bias the thermistor (designed for use with a 10 kΩ NTC β = 3435) connected from the TS terminal to VSS. If this feature is not needed, a fixed 10 kΩ can be placed between TS and VSS to allow normal operation. This may be done if the host is monitoring the thermistor and then the host determines when to pull the TS terminal low to disable charge.

Typical Performance Characteristics



V_{IN} = 5 V, C_{IN} = 10 uF, C_{OUT} = C_{BAT} = 4.7 uF,

R_{Iset} = 130 Ω, R_{preCHG} = 5.1 kΩ, R_{Iterm} = 1 kΩ

Figure 8. Charger Current vs. V_{BAT}

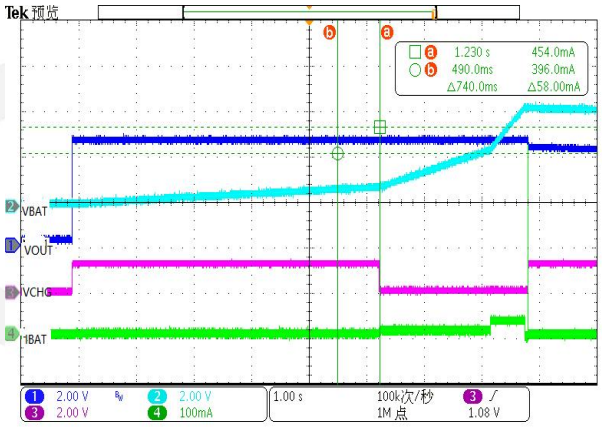


Figure 9. Charging Process

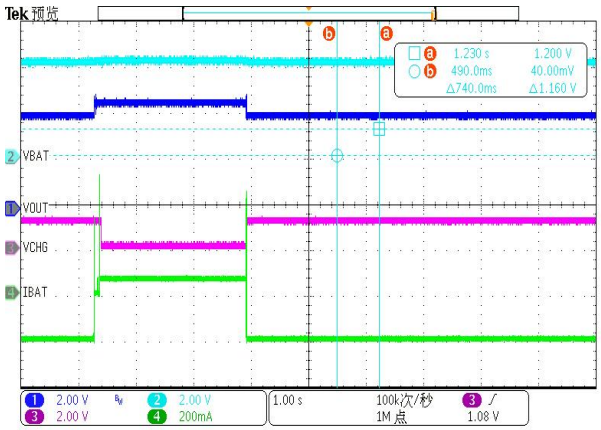


Figure 10. Power Path

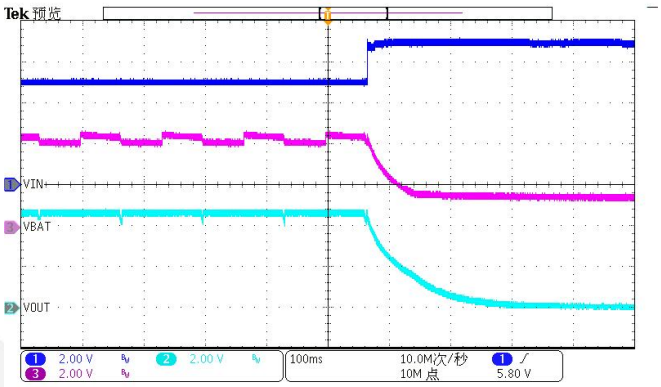
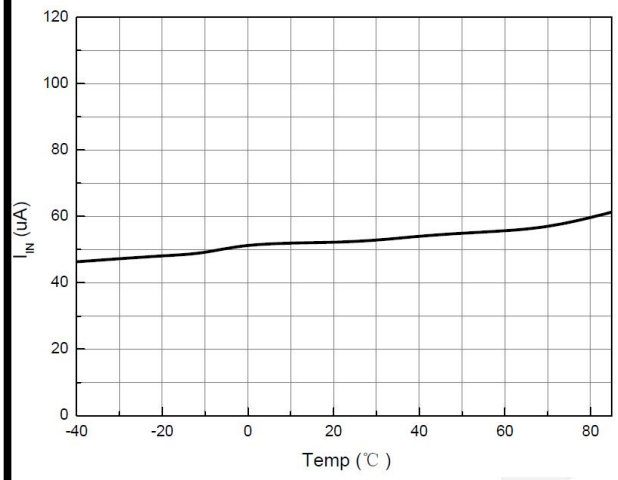
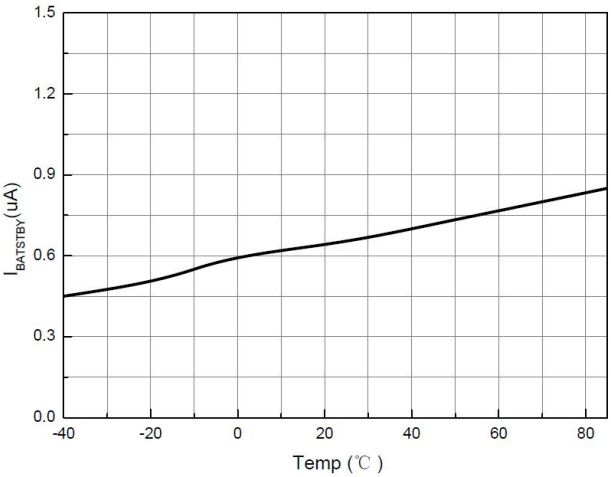


Figure 11. OVP Fault



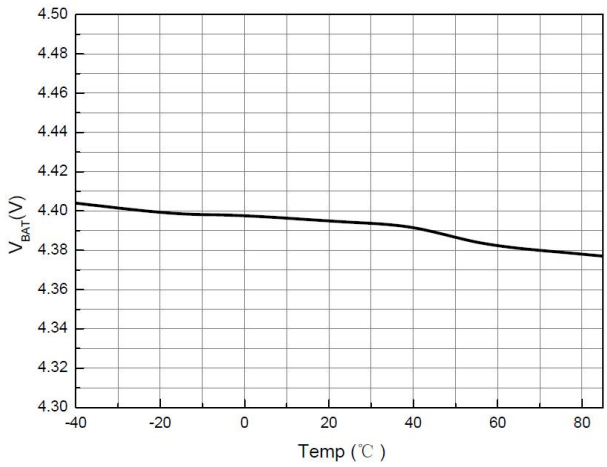
V_{IN} = 5 V, R_{ISET} = 1 kΩ, I_{SET1} = I_{SET2} = L

Figure 12. $I_{IN\ (STDBY)}$ vs. Temp



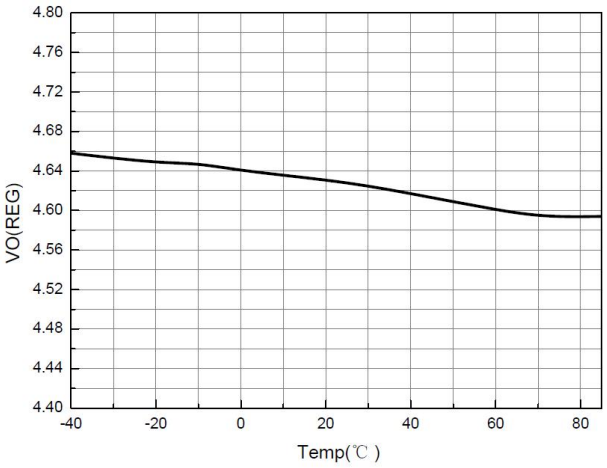
V_{IN} = 0 V, R_{ISET} = 1 kΩ, I_{SET1} = I_{SET2} = L, V_{BAT} = 4.2 V

Figure 13. $I_{BATSTBY}$ vs. Temp



V_{IN} = V_{ISET} = 5.8 V, V_{OUT} = 4.8 V

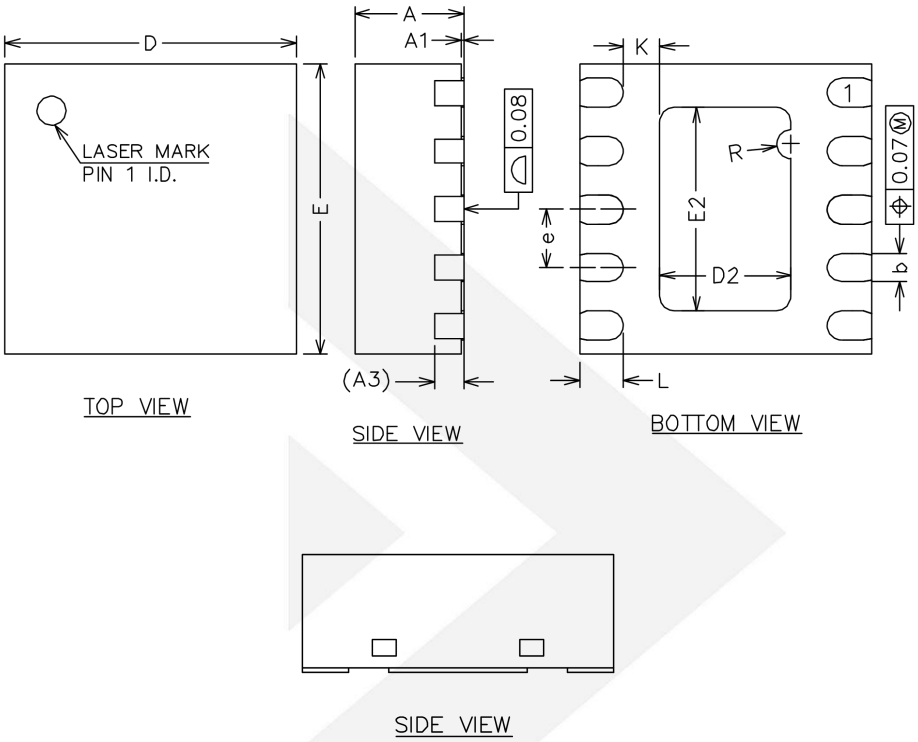
Figure 14. V_{BAT} vs. Temp



V_{IN} = 5 V, C_{IN} = 10 uF, C_{OUT} = 4.7 uF

Figure 15. $V_{O(REG)}$ vs. Temp

Physical Dimensions: DFN2*2-10



Common Dimensions (Units of Measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.80	0.90	1.00
E2	1.30	1.40	1.50
e	0.30	0.40	0.50
K	0.15	0.25	0.35
L	0.25	0.30	0.35
R		0.10 REF	

CONTACT US

Dioo is a professional design and sales corporation for high-quality and performance analog semiconductors. The company focuses on industry markets, such as cell phones, handheld products, laptops, medical equipment, and so on. Dioo's product families include analog signal processing and amplifying, LED drivers, and charger ICs. Go to http://www.dioo.com for a complete list of Dioo product families.

For additional product information or full datasheet, please contact our sales department or representatives.