DIO4482X
USB Type-C Analog Audio Switch with Protection Function

Features

- Power supply voltage range: 2.7 V to 5.5 V
- Version information:
  - DIO4482/DIO4482L: Default: DP_R~DP; DN_L~DN; turn-on
  - DIO4482B/DIO4482LB: Default: DP_R~DP; DN_L~DN; SBU1~SBU1_H; SBU2~SBU2_H turn-on
- USB 2.0 high speed switch:
  - −3 dB bandwidth: 970 MHz
  - R_{ON} = 4.3 Ω (Typ)
- Audio switch
  - Negative rail capability: −3.6 V to 3.6 V
  - THD + N = -110 dB, 1 V_{RMS}, f = 20 Hz to 20 kHz, 32 Ω load
  - −3 dB bandwidth: 830 MHz
  - R_{ON} = 1.0 Ω (Typ)
- High voltage protection
  - +20 V DC tolerance on USB type-C pins
  - +25 V surge capable on USB type-C pins
  - -20 V surge capable on USB type-C pins
  - ±8 kV HBM ESD
- Over voltage protection:
  - DP_R, DN_L V_{TH} = 4.8 V (Typ)
  - SBU1/SUB2/GSBU1/GSBU2 V_{TH} = 4.5 V (Typ)
- Support OMTP, CTIA, and 3-pole audio jack pinouts
- Support moisture detection
- 25-ball WLCSP package (2.24 mm × 2.28 mm)

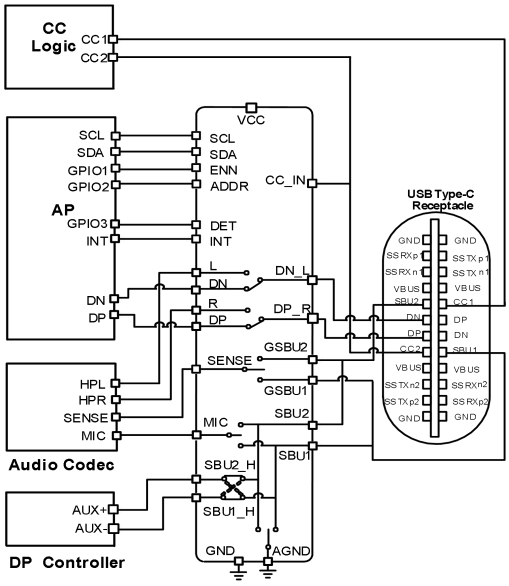
Applications

- Mobile phones
- Tablets
- Notebook PCs
- Media players

Descriptions

The DIO4482/DIO4482B/DIO4482L/DIO4482LB are high-performance USB Type−C analog switches that support analog audio headsets and can be used in portable multimedia devices. They can detect OMTP, CTIA, or 3-pole headsets and configure pinouts automatically. The DIO4482/B/L/LB shares common Type−C pins to pass USB 2.0 signal, analog audio signal, sidebands use wires and analog microphone signals. The DIO4482/B/L/LB also supports high voltages and surge on SBUx pins and USB pins on the USB Type−C receptacle side.

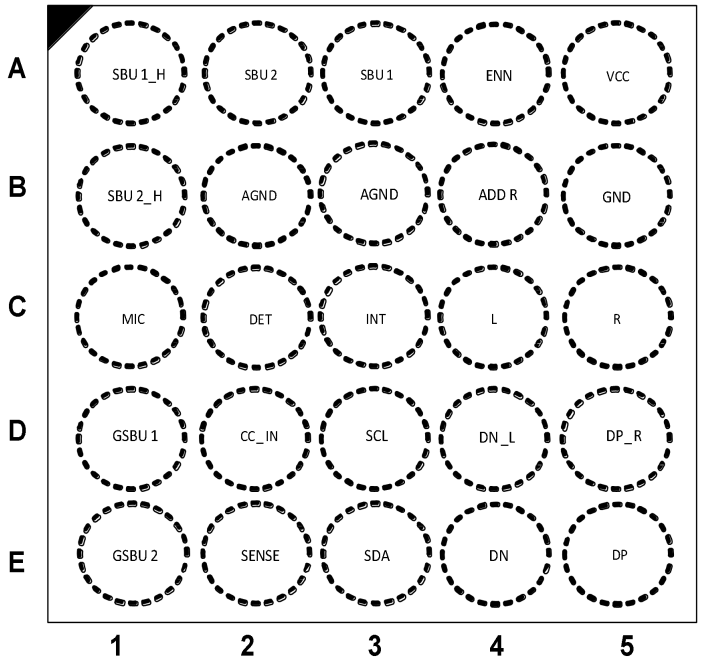
Block Diagram



Ordering Information

Ordering Part No.	Top Marking	MSL	RoHS	T_A	Package	
DIO4482WL25	D4HB	1	Green	-40 to 85°C	WLCSP-25	Tape & Reel, 3000
DIO4482LWL25	DH2L	1	Green	-40 to 85°C	WLCSP-25	Tape & Reel, 3000
DIO4482BWL25	DH2B	1	Green	-40 to 85°C	WLCSP-25	Tape & Reel, 3000
DIO4482LBWL25	D2LB	1	Green	-40 to 85°C	WLCSP-25	Tape & Reel, 3000

Pin Assignment



WLCSP-25

Figure 1. Top view

Pin Descriptions

Pin	Name	Description
A5	VCC	Power supply (2.7 V to 5.5 V)
B5	GND	Chip ground
D5	DP_R	USB/Audio common pin
D4	DN_L	USB/Audio common pin
E5	DP	USB data (differential +)
E4	DN	USB data (differential –)
C5	R	Audio – right channel
C4	L	Audio – left channel
A3	SBU1	Sideband use wire 1
A2	SBU2	Sideband use wire 2
C1	MIC	Microphone signal
B2	AGND	Audio signal ground
B3	AGND	Audio signal ground
E2	SENSE	Audio ground reference output
C3	INT	I^2C Interrupt output, active low (open drain)
D2	CC_IN	Audio accessory attachment detection input
D1	GSBU1	Audio sense path 1 to headset jack GND
E1	GSBU2	Audio sense path 2 to headset jack GND
C2	DET	Push−pull output. When CC_IN > 1.5 V, DET is low and CC_IN < 1.2 V, DET is high
D3	SCL	I^2C clock
E3	SDA	I^2C data
B1	SBU2_H	Host side sideband use wire 2
A1	SBU1_H	Host side sideband use wire 1
A4	ENN	Chip enable, active low, internal pull−down by 470 kΩ
B4	ADDR	I^2C slave address pin

Absolute Maximum Ratings

Stresses beyond those listed under the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol		Parameter		Rating	Unit
V_{CC}		Supply voltage from VCC		−0.5 to 6.5	V
V_{CC_IN}		V_{CC_IN} to GND		−0.5 to 20	V
V_{SW_C}		V_{DP_R} to GND, V_{DN_L} to GND		−3.5 to 20	V
V_{SW_USB}		V_{DP} to GND, V_{DN} to GND		−0.5 to 6.5	V
V_{SW_Audio}		V_L to GND, V_R to GND		−3.6 to 6.5	V
$V_{V\_SBUx/GSBUx}$		V_{SBU1} to GND, V_{SBU2} to GND, V_{GSBU1} to GND, V_{GSBU1} to GND		−0.5 to 20	V
V_{VSBUx_H}		V_{SBU1_H} to GND, V_{SBU2_H} to GND		−0.5 to 6.5	V
$V_{I/O}$		SENSE, MIC, DET, INT to GND		−0.5 to 6.5	V
V_{CNTRL}		Control input voltage	SDA, SCL, ENN, ADDR	−0.5 to 6.5	V
I_{SW_Audio}		Switch I/O current, audio path		−250 to 250	mA
I_{SW_USB}		Switch I/O current, USB path		100	mA
I_{SW_MIC}		Switch I/O current, MIC to SBU1 or SBU2		50	mA
I_{SW_SBUx}		Switch I/O current, SBUx to SBUx_H		50	mA
I_{SW_SENSE}		Switch I/O current, SENSE to GSBU1 or GSBU2		100	mA
I_{SW_AGND}		Switch I/O current, AGND to SBU1 or SBU2		500	mA
I_{IK}		DC input diode current		−50	mA
ESD	HBM	Human body model, ANSI/ESDA/JEDEC JS−001	Connector side and power pins: VCC, SBU1, SBU2, DP_R, DN_L, GSBU1, GSBU2, CC_IN	±8	kV
			Host side pins: the rest pins	±5	kV
	CDM	Charged device model, ANSI/ESDA/JEDEC JS−002		±2	kV
T_{STG}		Storage temperature		−65 to 150	°C

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter		Min	Typ	Max	Unit
Power						
V_{CC}	Supply voltage		2.7		5.5	V
USB switch						
V_{SW_USB}	V_{DP} to GND, V_{DN} to GND, V_{DP_R} to GND, V_{DN_L} to GND		0		3.6	V
AUDIO switch						
V_{SW_Audio}	V_{DP_R} to GND, V_{DN_L} to GND, V_L to GND, V_R to GND		−3.6		3.6	V
MIC switch						
V_{VSBU_MIC}	V_{SBU1} to GND, V_{SBU2} to GND, V_{MIC} to GND		0		3.6	V
SENSE switch						
V_{VGSBU_SEN}	V_{GSBU1} to GND, V_{GSBU2} to GND, V_{SENSE} to GND		0		3.6	V
SBU TO SBUX_H switch						
V_{VGSBU}	V_{SBU1} to GND, V_{SBU2} to GND, V_{SBU1_H} to GND, V_{SBU2_H} to GND		0		3.6	V
CC_IN pin						
V_{CC_IN}	V_{CC_IN} to GND		0		5.5	V
Control voltage (ADDR/ENN/SDA/SCL)						
V_{IH}	DIO4482WL25 DIO4482BWL25	Input voltage high	1.3		V_{CC}	V
V_{IL}		Input voltage low			0.5	V
V_{IH}	DIO4482LWL25 DIO4482LBWL25	Input voltage high	0.825		V_{CC}	V
V_{IL}		Input voltage low			0.35	V
Operating temperature						
T_A	Ambient operating temperature		−40	25	85	°C

DC Electrical Characteristics

V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = -40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Power	Min	Typ	Max	Unit
I_{CC}	Supply current	USB switches ON, SBUx to SBUx_H switches ON	V_{CC} = 4.2 V		70		μA
		Audio switches ON, MIC switch ON and Audio GND switch ON			70		μA
I_{CCZ}	Quiescent current	ENN = L, 04H'b7 = 0			2		μA
USB/AUDIO common pins: DP_R, DN_L							
I_{OZ}	Off leakage current of DP_R and DN_L	DN_L, DP_R = −3 V to 3.6 V	V_{CC} = 2.7 V to 5.5 V	-3		3	μA
I_{OFF}	Power−off leakage current of DP_R and DN_L	DN_L, DP_R = 0 V to 3.6 V	Power off	-3		3	μA
V_{OV_TRIP}	Input OVP lockout	Rising edge	V_{CC} = 2.7 V to 5.5 V	4.6	4.8	5	V
V_{OV_HYS}	Input OVP hysteresis				0.3		V
AUDIO switch							
I_{ON}	On leakage current of audio switch	DN_L, DP_R = −3 V to 3 V, DP, DN, R, L = float	V_{CC} = 2.7 V to 5.5 V	-3		3	μA
I_{OFF}	Power−off leakage current of L and R	L, R = 0 V to 3 V; DP_R, DN_L = float	Power off	-1		1	μA
R_{ON}	Switch on resistance	I_{SW} = 100 mA, V_{SW} = −3 V to 3 V	V_{CC} = 2.7 V to 5.5 V		1		Ω
R_{SHUNT}	Pull down resistor on R/L pin when audio switch is off	L = R = 3 V		6	10	14	kΩ
USB switch							
I_{ON}	On leakage current of USB switch	DN_L, DP_R = 0 V to 3.6 V, DP, DN, R, L = float	V_{CC} = 2.7 V to 5.5 V	-3		3	μA
I_{OZ}	Off leakage current of DP and DN	DN, DP = 0 V to 3.6 V	V_{CC} = 2.7 V to 5.5 V	-3		3	μA
I_{OFF}	Power−off leakage current of DP and DN	DN, DP = 0 V to 3.6 V	Power off	-3		3	μA
R_{ON_USB}	USB switch on resistance	I_{SW} = 8 mA, V_{SW} = 0.4 V	V_{CC} = 2.7 V to 5.5 V		4.3		Ω
SENSE switch							
I_{ON}	Sense path leakage current	GSBUx = 0 V to 1 V, SENSE is floating	V_{CC} = 2.7 V to 5.5 V	-2		2	μA
R_{ON}	Sense switch ON resistance	I_{OUT} = 100 mA, V_{SW} = 1.0 V	V_{CC} = 2.7 V to 5.5 V		270		mΩ

I_{OZ}	Off leakage current of SENSE	SENSE = 0 V to 1.0 V	V_{CC} = 2.7 V to 5.5 V	-2		2	µA
	Off leakage current of GSBUx	GSBUx = 1 V to 3.6 V		-3		3	
I_{OFF}	Power−off leakage current of SENSE	SENSE = 0 V to 1.0 V	V_{CC} = 2.7 V to 5.5 V	-2		2	µA
	Power−off leakage current of GSBUx	GSBUx = 0 V to 3.6 V		-3		3	
V_{OV_TRIP}	Input OVP lockout on GSBUx	Rising edge	V_{CC} = 2.7 V to 5.5 V	4.3	4.5	4.7	V
V_{OV_HYS}	Input OVP hysteresis of GSBUx				0.3		V
SBUX pins							
I_{OZ}	Off leakage current of SBUx	SBUx = 0 V to 3.6 V	V_{CC} = 2.7 V to 5.5 V	-3		3	µA
I_{OFF}	Power−off leakage Current port SBUx	SBUx = 0 V to 3.6 V	Power off	-2		10	µA
V_{OV_TRIP}	Input OVP lockout	Rising edge	V_{CC} = 2.7 V to 5.5 V	4.3	4.5	4.7	V
V_{OV_HYS}	Input OVP hysteresis				0.3		V
MIC switch							
I_{ON}	On leakage current of MIC switch	SBUx = 0 V to 3.6 V, MIC is floating	V_{CC} = 2.7 V to 5.5 V	-3		3	µA
I_{OZ}	Off leakage current of MIC	MIC = 0 V to 3.6 V		-1		1	µA
I_{OFF}	Power off leakage current of MIC	MIC = 0 V to 3.6 V	Power off	-1		1	µA
R_{ON}	MIC switch on resistance	V_{SW} = 3.6 V, Isw = 30 mA	V_{CC} = 2.7 V to 5.5 V		3.3		Ω
SBUX_H switch							
I_{ON}	On leakage current of SBUx_H switch	SBUx = 0 V to 3.6 V, SBUx_H is floating	V_{CC} = 2.7 V to 5.5 V	-3		3	µA
I_{OZ}	Off leakage of SBUx_H	SBUx_H = 0 V to 3.6 V		-1		1	µA
I_{OFF}	Power off leakage current of SBUx_H	SBUx_H = 0 V to 3.6 V	Power off	-1		1	µA
R_{ON}	SBUx_H switch on resistance	V_{SW} = 0 V to 3.6 V, Isw = 30 mA	V_{CC} = 2.7 V to 5.5 V		2.8		Ω
AUDIO ground switch: pin: AGND TO SBUX							
R_{ON}	AGND switch on resistance	I_{SOURCE} = 100 mA on SBUx	V_{CC} = 2.7 V to 5.5 V		66		mΩ
CC_IN pin							
V_{TH_L}	Input low threshold		V_{CC} = 2.7 V to 5.5 V		1.2		V
V_{TH_H}	Input high threshold				1.5		V
I_{IN}	Input leakage of CC_IN	CC_IN = 0 V to 5.5 V				1	µA

INT, DET pins							
V_{OH}	Output high for DET	Io = −2 mA	V_{CC} = 2.7 V to 5.5 V	1.5	1.8	2	V
V_{OL}	Output low for DET and INT	Io = 2 mA				0.4	V
ADDR pin							
V_{IH}	DIO4482WL25 DIO4482BWL25	Input voltage high	V_{CC} = 2.7 V to 5.5 V	1.3			V
V_{IL}		Input voltage low				0.5	V
V_{IH}	DIO4482LWL25 DIO4482LBWL25	Input voltage high		0.825			
V_{IL}		Input voltage low				0.35	
I_{IN}	Control input leakage	ADDR = 0 V to V_{CC}		-1		1	μA
ENN pin							
V_{IH}	DIO4482WL25 DIO4482BWL25	Input voltage high	V_{CC} = 2.7 V to 5.5 V	1.3			V
V_{IL}		Input voltage low				0.5	V
V_{IH}	DIO4482LWL25 DIO4482LBWL25	Input voltage high		0.825			V
V_{IL}		Input voltage low				0.35	V
R_{PD}	Internal pull down resistor				470		kΩ
SDS, SCL pins							
V_{ILI2C}	DIO4482WL25 DIO4482BWL25	Low−level input voltage	V_{CC} = 2.7 V to 5.5 V			0.5	V
V_{IHI2C}		High−level input voltage		1.3			V
V_{ILI2C}	DIO4482LWL25 DIO4482LBWL25	Low−level input voltage				0.35	V
V_{IHI2C}		High−level input voltage		0.825			V
I_{I2C}	Input current of SDA and SCL pins	SCL/SDA = 0 V to 3.6 V		-2		2	μA
V_{OLSDA}	Low−level output voltage	I_{OLSDA} = 2 mA				0.3	V
I_{OLSDA}	Low−level output current	V_{OLSDA} = 0.2 V		10			mA

Note:

(1) Specifications subject to change without notice.

AC Electrical Characteristics

V_{CC}=2.7 V to 5.5V, V_{CC} (Typ.) =3.3 V, T_A = -40°C to 85°C, and T_A(Typ.) =25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Power	Min	Typ	Max	Unit
AUDIO switch							
t_{delay}	Audio switch turn on delay time	DP_R = DN_L = 1 V, R_L = 32 Ω	V_{CC} = 3.3 V		40		μs
t_{rise}	Audio switch turn on rising time(1)	DP_R = DN_L = 1 V, R_L = 32 Ω			75		μs
t_{OFF}	Audio switch turn-off time	DP_R = DN_L = 1 V, R_L = 32 Ω			7		μs
X_{TALK}	Cross talk (adjacent)	f = 1 kHz, R_L = 50 Ω, V_{SW} = 1 V_{RMS}			-90		dB
BW	−3 dB bandwidth	R_L = 50 Ω			830		MHz
OIRR	Off isolation	f = 1 kHz, R_L = 50 Ω, C_L = 0 pF, V_{SW} = 1 V_{RMS}			-95		dB
THD+N	Total harmonic distortion + noise performance with A−weighting filter	R_L = 600 Ω, f = 20 Hz ~ 20 kHz, V_{SW} = 2V_{RMS}			-110		dB
		R_L = 32 Ω, f = 20 Hz ~ 20 kHz, V_{SW} = 1 V_{RMS}			-110		dB
		R_L = 16 Ω, f = 20 Hz ~ 20 kHz, V_{SW} = 0.5 V_{RMS}			-108		dB
USB switch							
t_{ON}	USB switch turn−on time	DP_R = DN_L =1.5 V, R_L = 50 Ω	V_{CC} = 3.3 V		40		μs
t_{OFF}	USB switch turn−off time	DP_R = DN_L =1.5 V, R_L = 50 Ω			6		μs
BW	−3 dB bandwidth	R_L = 50 Ω			970		MHz
OIRR	Off Isolation between DP, DN and Common Node Pins	f = 1 kHz, R_L = 50 Ω, C_L = 0 pF, V_{SW} = 1 V_{RMS}			-100		dB
t_{OVP}	DP_R and DN_L pins OVP response time	Vsw = 3.5 V to 5.5 V			0.4		μs
MIC/AUDIO ground switch							
t_{delay_MIC}	MIC switch turn-on delay time	SBUx = 1 V, R_L = 50 Ω	V_{CC} = 3.3 V		75		μs
t_{rise_MIC}	MIC switch turn-on rising time(1)				120		
t_{delay_AGND}	AGND switch turn-on time	SBUx pulled up to 0.5 V by 16 Ω, AGND connect to GND			1		ms
t_{rise_AGND}	AGND switch turn-on rising time(1)				1.5		
t_{OFF_MIC}	MIC switch turn-off time	SBUx = 2.5 V, R_L = 50 Ω			6		μs

$t_{OFF\_Audio\ GND}$	AGND switch turn-off time	SBUx: Isource = 10 mA, clamp to 2.5 V			65		μs
BW	-3dB bandwidth	R_L = 50 Ω			60		MHz
SBUx_H switch							
t_{ON}	SBUx_H switch turn-on time	SBUx = 2.5 V, R_L= 50 Ω	V_{CC} = 3.3 V		65		μs
t_{OFF}	SBUx_H switch turn-off time				150		ns
BW	-3dB Bandwidth	R_L = 50 Ω			60		MHz
t_{OVP}	SBUx pins OVP response time	Vsw = 3.5 V to 5.5 V			0.4		μs
SENSE switch							
t_{delay}	Sense switch turn-on delay time	GSBUx = 1 V, R_L= 50 Ω	V_{CC} = 3.3 V		280		μs
t_{rise}	Sense switch turn-on rising time(1)				500		μs
t_{OFF}	Sense switch turn-off time				6.5		μs
t_{OVP}	GSBUx pins OVP response time	V_{SW} = 3.5 V to 5.5 V			0.4		μs
BW	-3dB Bandwidth	R_L = 50 Ω			150		MHz
DET delay							
t_{DELAY_DET}	DET response delay	Transition from 0 to 1.8 V	V_{CC} = 3.3 V		0.9		μs
		Transition from 1.8 to 0 V			2		

Note:

(1) Turn-on timing can be controlled by I^2C register.

(2) Specifications subject to change without notice.

I²C Specification

V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = -40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	I²C_SCL clock frequency			400	kHz
$t_{HD;\ STA}$	Hold time (repeated) START condition	0.6			μs
t_{LOW}	Low period of I²C_SCL clock	1.3			μs
t_{HIGH}	High period of I²C_SCL clock	0.6			μs
$t_{SU;\ STA}$	Set−up time for repeated START condition	0.6			μs
$t_{HD;\ DAT}$	Data hold time (1)	0		0.9	μs
$t_{SU;\ DAT}$	Data set−up time (2)	100			ns
t_r	Rise time of I²C_SDA and I²C_SCL signals (2)	20 + 0.1 Cb		300	ns
t_f	Fall time of I²C_SDA and I²C_SCL signals (2)	20 + 0.1 Cb		300	ns
$t_{SU;\ STO}$	Set−up time for STOP condition	0.6			μs
t_{BUF}	Bus−free time between STOP and START conditions	1.3			μs
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	0		50	ns

Note:

(1) Guaranteed by characterization. Not production tested.

(2) A fast−mode I²C−bus device can be used in a standard−mode I²C−bus system, but the requirement $t_{SU;DAT} \geq$ ±250 ns must be met. This is automatically the case if the device does not stretch the LOW period of the I²C_SCL signal. If such a device does stretch the LOW period of the I²C_SCL signal, it must output the next data bit to the I²C_SDA line t_{r_max} + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard−mode I²C bus specification) before the I²C_SCL line is released.

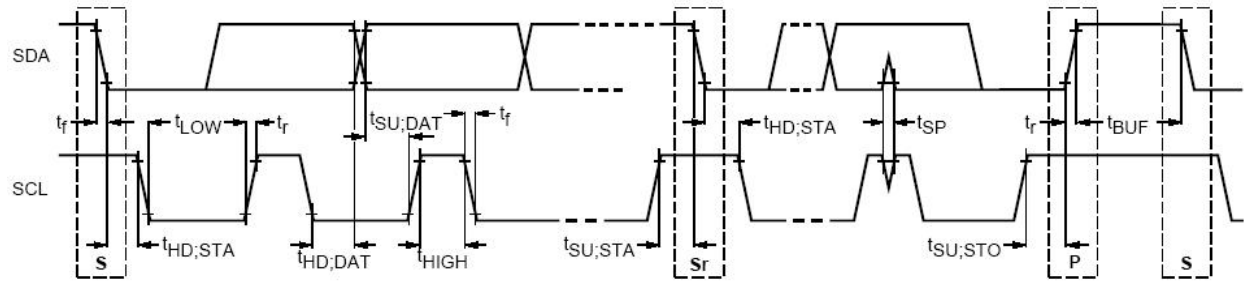


Figure 2. Definition of timing for full−speed mode devices on the I²C bus

Capacitance

V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = -40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions		Power	Min	Typ	Max	Unit
$C_{ON\_USB/Audio}$	On capacitance (common port)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias		V_{CC} = 3.3 V		8		pF
$C_{OFF\_USB/Audio}$	Off capacitance (common port)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias				6.5		pF
C_{OFF_USB}	Off capacitance (non−common ports)	f = 1 MHz,100 mV_{PK-PK}, 100 mV DC bias				2.6		pF
$C_{ON\_SENSE\_SW}$	On capacitance (common ports)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias				55		pF
$C_{OFF\_SENSE\_SW}$	Off capacitance (common ports)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias				88		pF
$C_{ON\_MIC\_SW}$	On capacitance (common ports)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias				170		pF
$C_{OFF\_MIC\_SW}$	Off capacitance (common ports)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias				10		pF
$C_{ON\_AGND\_SW}$	On capacitance (common port)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias				125		pF
$C_{ON\_SBUx\_H\_SW}$	On capacitance (common port)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias				160		pF
C_{CNTRL}	Control input pin capacitance	f = 1 MHz, 100 mV_{PP}, 100 mV DC bias	ENN			3		pF

Register Maps

ADDR	Register Name	Type	Reset Value	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00H	Device ID	R	0XF3	1	1	1	1	0	0	0	1
01H	OVP interrupt mask	R/W	0x00	Reserved	Mask OVP interrupt	Mask OVP /DP_R	Mask OVP /DN_L	Mask OVP /SBU1	Mask OVP /SBU2	Mask OVP /GSBU1	Mask OVP /GSBU2
02H	OVP interrupt flag	R	0x00	Reserved	Reserved	OVP/ DP_R	OVP/ DN_L	OVP/ SBU1,SBU2		OVP/ GSBU1	OVP/ GSBU2
03H	OVP status	R	0x00	Reserved	Reserved	OVP/ DP_R	OVP/ DN_L	OVP/ SBU1,SBU2		OVP/ GSBU1	OVP/ GSBU2
04H	Switch settings enable	R/W	4482/L: 0x98 4482B/L B:0xF8	Device control	SBU1_H to SBUx	SBU2_H to SBUx	DN_L to DN or L	DP_R to DP or R	Sense to GSBUx	MIC to SBUx	Audio ground to SBUx
05H	Switch select	R/W	0x18	Reserved	SBU1_H to SBUx	SBU2_H to SBUx	DN_L to DN or L	DP_R to DP or R	Sense to GSBUx	MIC to SBUx	Audio ground to SBUx
06H	Switch status0	R	0x05	Reserved		Sense switch status		DP_R switch status		DN_L switch status	
07H	Switch status1	R	4482/L: 0x00 4482B/L B:0x23	Reserved		SBU2 switch status			SBU1 switch status		
08H	Audio switch left channel turn-on control	R/W	0x01	Audio switch left channel slow control [7:0]							
09H	Audio switch right channel turn-on control	R/W	0x01	Audio switch right channel slow control [7:0]							
0AH	MIC switch turn-on control	R/W	0x01	MIC switch slow control [7:0]							
0BH	Sense switch turn-on control	R/W	0x01	Sense switch slow control [7:0]							
0CH	Audio ground switch turn-on control	R/W	0x01	Audio ground switch slow control [7:0]							

0DH	Timing delay between R switch enable and switch on order	R/W	0x00	Timing delay between R switch enable and switch on order control [7:0]								
0EH	Timing delay between MIC switch enable and switch on order	R/W	0x00	Timing delay between MIC switch enable and switch on order control [7:0]								
0FH	Timing delay between sense switch enable and switch on order	R/W	0x00	Timing delay between sense switch enable and switch on order control [7:0]								
10H	Timing delay between Audio ground switch enable and switch on order	R/W	0x00	Timing delay between audio ground switch enable and switch on order control [7:0]								
11H	Audio accessory status	R	0x02	Reserved							CC_IN	DET
12H	Function enable	R/W	0x00	Reserved	DET I/O control	RES detection r ange setting	GPIO control enable	Slow turn-on control enable	MIC auto break out control enable	RES detection: auto clear	Audio jack detection and configurati on enable	
13H	RES detection pin setting	R/W	0x00	Reserved					Resistance detection pin select [2:0]			
14H	RES detection value	R	0x00	RES detection value [7:0]								
15H	RES detection interrupt threshold	R/W	0x02	Resistance detection threshold [7:0]								
16H	RES detection	R/W	0X04	Reserved				Res detection time [3:2]		Res detection interval [1:0]		

	interval							
17H	Audio jack status	R	0x01	Reserved	4 pole, SBU2 to MIC	4 pole, SBU1 to MIC	3 pole	No audio
18H	RES detection/audio jack detection interrupt flag	R	0x00	Reserved		Audio jack detection done	Low resistance occurred	Low resistance detection
19H	RES/audio jack detection interrupt mask	R/W	0x00	Reserved		Audio detection done mask	Low resistance occurred	Low resistance detection
1CH	MIC detection threshold DATA0	R/W	0x20	MIC threshold value DATA0 [7:0]				
1DH	MIC detection threshold DATA1	R/W	0xFF	MIC threshold value DATA1 [7:0]				
1EH	I²C reset	W/C	0x00	Reserved				I²C reset
1FH	Current source setting	R/W	0x07	Reserved	Current source setting [3:0]			
20H	Timing delay between L switch enable and switch on order	R/W	0x00	Delay timing setting [7:0]				

I²C Slave Address

ADDR	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ADDR = L	1	0	0	0	0	1	0	R/W
ADDR = H	1	0	0	0	0	1	1	R/W

Device ID

Address: 00h

Reset Value: 8'b 1111_0011

Type: Read

Bits	Name	Size	Description
[7:6]	Vendor ID	2	Vendor ID
[5:3]	Version ID	3	Device version ID
[2:0]	Revision ID	3	Revision history ID

OVP Interrupt Mask

Address: 01h

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
7	Reserved	1	Do not use
6	OVP interrupt mask control	1	OVP interrupt function enable/disable 0: Controlled by [5:0] bit 1: Mask all connector side pins OVP interrupt
5	DP_R OVP interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt
4	DN_L OVP interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt
3	SBU1 OVP interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt
2	SBU2 OVP interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt
1	GSBU1 OVP interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt
0	GSBU2 OVP Interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt

OVP INTERRUPT Flag

Address: 02h

Reset Value: 8'b 0000_0000

Type: Read Clear

Bits	Name	Size	Description
[7:6]	Reserved	2	Do not use
5	DP_R OVP	1	0: OVP event has not occurred 1: OVP event has occurred
4	DN_L OVP	1	0: OVP event has not occurred 1: OVP event has occurred
[3:2]	SBU1 || SBU2 OVP	2	0: OVP event has not occurred 1: At least one of SBU1 or SBU2 OVP event has occurred

1	GSBU1 OVP	1	0: OVP event has not occurred 1: OVP event has occurred
0	GSBU2 OVP	1	0: OVP event has not occurred 1: OVP event has occurred

OVP Status

Address: 03h

Reset Value: 8'b 0000_0000

Type: Read

Bits	Name	Size	Description
[7:6]	Reserved	2	Do not use
5	OVP on DP_R PIN	1	0: OVP event has not occurred 1: OVP event has occurred
4	OVP on DN_L PIN	1	0: OVP event has not occurred 1: OVP event has occurred
[3:2]	SBU1 || SBU2 OVP	2	0: OVP event has not occurred 1: At least one of SBU1 or SBU2 OVP event has occurred
1	OVP on GSBU1 PIN	1	0: OVP event has not occurred 1: OVP event has occurred
0	OVP on GSBU2 PIN	1	0: OVP event has not occurred 1: OVP event has occurred

Switching Setting Enable

Address: 04h

Reset Value: DIO4482/L: 8'b 1001_1000

DIO4482B/LB: 8'b 1111_1000

Type: Read/Write

Bits	Name	Size	Description
7	Device enable	1	0: Device disable; L, R pull down by 10 kΩ and other switch nodes will be high−Z for positive input. 1: Device enable. Device enable = 1 / Device enable = 0 ENN = 1 device disable / Device disable ENN = 0 device enable / Device disable
6	SBU1_H to SBUx switches	1	0: Switch disable; SBU1_H will be high−Z for positive input 1: Switch enable
5	SBU2_H to SBUx switches	1	0: Switch disable; SBU2_H will be high−Z for positive input 1: Switch enable
4	DN_L to DN or L switches	1	0: Switch disable; DN_L, DN will be high−Z for positive input. L pull down by 10 kΩ 1: Switch enable
3	DP_R to DP or R switches	1	0: Switch disable; DP_R, DP will be high−Z for positive input. R pull down by 10 kΩ 1: Switch enable

2	Sense to GSBUx switches	1	0: Switch disable; Sense, GSBU1 and GSBU2 will be high−Z for positive input 1: Switch enable
1	MIC to SBUx switches	1	0: Switch disable: MIC will be high−Z for positive input. 1: Switch enable
0	AGND to SBUx switches	1	0: Switch disable: AGND will be high−Z for positive input. 1: Switch enable

Switch Select

Address: 05h

Reset Value: 8'b 0001_1000

Type: Read/Write

Bits	Name	Size	Description
7	Reserved	1	Do not use
6	SBU1_H switches	1	0: SBU1_H to SBU1 switch ON 1: SBU1_H to SBU2 switch ON
5	SBU2_H switches	1	0: SBU2_H to SBU2 switch ON 1: SBU2_H to SBU1 switch ON
4	DN_L to DN or L switches	1	0: DN_L to L switch ON 1: DN_L to DN switch ON
3	DP_R to DP or R switches	1	0: DP_R to R switch ON 1: DP_R to DP switch ON
2	Sense to GSBUx switches	1	0: Sense to GSBU1 switch ON 1: Sense to GSBU2 switch ON
1	MIC to SBUx switches	1	0: MIC to SBU2 switch ON 1: MIC to SBU1 switch ON
0	AGND to SBUx switches	1	0: AGND to SBU1 switch ON 1: AGND to SBU2 switch ON

Switch Status0

Address: 06h

Reset Value: 8'b 0000_0101

Type: Read Only

Bits	Name	Size	Description
[7:6]	Reserved	2	Do not use
[5:4]	Sense switch status	2	00: Sense switch is open/not connected 01: Sense connected to GSBU1 10: Sense connected to GSBU2 11: Not valid
[3:2]	DP_R switch status	2	00: DP_R Switch open/not connected 01: DP_R connected to DP 10: DP_R connected to R 11: Not valid
[1:0]	DN_L switch status	2	00: DN_L switch open/not connected 01: DN_L connected to DN

			10: DN_L connected to L 11: Not valid

Switch Status1

Address: 07h

Reset Value: DIO4482/L: 8'b 0000_0000

DIO4482B/LB: 8'b 0010_0011

Type: Read Only

Bits	Name	Size	Description
[7:6]	Reserved	2	Do not use
[5:3]	SBU2 switch status	3	000: SBU2 switch is open/not connected 001: SBU2 connected to MIC 010: SBU2 connected to AGND 011: SBU2 connected to SBU1_H 100: SBU2 connected to SBU2_H 101: SBU2 connected both SBU1_H and SBU2_H 110…111: Do not use
[2:0]	SBU1 switch status	3	000: SBU1 switch is open/not connected 001: SBU1 connected to MIC 010: SBU1 connected to AGND 011: SBU1 connected to SBU1_H 100: SBU1 connected to SBU2_H 101: SBU1 connected both SBU1_H and SBU2_H 110…111: Do not use

Audio Switch Left Channel Slow Turn-on

Address: 08h

Reset Value: 8'b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn-on rising time setting	8	11111111: 25600 μs
			…
			00000001: 200 μs
			00000000: 100 μs

Audio Switch Right Channel Slow Turn-on

Address: 09h

Reset Value: 8'b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn-on rising time setting	8	11111111: 25600 μs
			…
			00000001: 200 μs
			00000000: 100 μs

MIC Switch Slow Turn-on

Address: 0Ah

Reset Value: 8'b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn-on rising time setting	8	11111111: 25700 μs
			…
			00000010: 350 μs
			00000001: 250 μs
			00000000: Not valid

Sense Switch Slow Turn-on

Address: 0Bh

Reset Value: 8'b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn-on rising time setting	8	11111111: 25600 μs
			…
			00000001: 200 μs
			00000000: 100 μs

Audio Ground Switch Slow Turn-on

Address: 0Ch

Reset Value: 8'b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn-on rising time setting	8	11111111: 179000 μs
			…
			00000001: 1400 μs
			00000000: 700 μs

Timing Delay between R Switch Enable and Switch-on Order

Address: 0Dh

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 102 ms
			11111110: 101.6 ms
			…
			00000001: 400 μs
			00000000: 0 μs

Timing Delay between MIC Switch Enable and Switch-On Order

Address: 0Eh

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 102 ms
			11111110: 101.6 μs
			…
			00000001: 400 μs
			00000000: 0 μs

Timing Delay between Sense Switch Enable and Switch-On Order

Address: 0Fh

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 102 ms
			11111110:101.6 ms
			…
			00000001: 400 μs
			00000000: 0 μs

Timing Delay between Audio Ground Switch Enable and Switch-On Order

Address: 10h

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 102 ms
			11111110: 101.6 ms
			…
			00000001: 400 μs
			00000000: 0 μs

Audio Accessory Status

Address: 11h

Reset Value: 8'b 0000_0010

Type: Read/Write

Bits	Name	Size	Description
[7:2]	Reserved	6	Do not use
1	CC_IN	1	0: CC_IN < 1.2 V 1: CC_IN > 1.5 V
0	DET	1	0: DET output is low 1: DET is output is high

Function Enable

Address: 12h

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
7	Reserved	1	Do not use
6	DET I/O Control	1	1: DET pin is in Open/Drain Configuration 0: DET pin is in Push/Pull Configuration
5	RES detection range setting	1	1: 10 k to 2560 k 0: 1 k to 256 k
4	GPIO control enable	1	Do not use
3	Slow turn-on control enable	1	1: Enable 0: Disable
2	MIC auto break out control enable	1	1: Enable 0: Disable
1	RES detection enable	1	1: Enable; will be changed to '0' after low resistance detection 0: Disable
0	Audio jack detection and configuration enable	1	1: Enable; will be changed to '0' after audio jack detection and configuration 0: Disable

When GPIO control mode (manual switch control) is enabled. '**Switch control**' register is changed to read only.

Res Detection Pin Setting

Address: 13h

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:3]	Reserved	5	Do not use
[2:0]	Resistance detection pin select	3	000: CC_IN 001: DP_R 010: DN_L 011: SBU1 100: SBU2 101: Do not use ... 111: Do not use

Recommend user to select the pin first before setting the RES detection pin enabled.

RES Value

Address: 14h

Reset Value: 8'b 1111_1111

Type: Read Clear

Bits	Name	Size	Description
[7:0]	Detected resistance value	8	Selection by 1 kΩ per step if Reg 12h[5]=0, Selection by 10 kΩ per step if Reg 12h[5]=1 0000_0000 : R < 1 k/10 k … 1111_1111: R > 300 K/3 M

Res Detection Threshold

Address: 15h

Reset Value: 8'b 0001_0110

Type: Read/Write

Bits	Name	Size	Description
[7:0]	RES detection threshold	8	Selection by 1 kΩ per step if Reg 12h[5] = 0, Selection by 10 kΩ per step if Reg 12h[5] = 1 Default value = 22 kΩ 0000_0000:1 kΩ/10 kΩ ... 1111_1111:256 kΩ/2560 kΩ

Res Detection Interval

Address: 16h

Reset Value: 8'b 0000_0100

Type: Read/Write

Bits	Name	Size	Description
[7:4]	Reserved	4	Do not use
[3:2]	RES detection duration time	2	00: Reserved 01:5 ms 10:10 ms 11:20 ms
[1:0]	RES detection interval	2	00: Single 01: 100 ms 10: 1 s 11: 10 s

Audio Jack Status

Address: 17h

Reset Value: 8'b 0000_0001

Type: Read

Bits	Name	Size	Description
[7:4]	Reserved	4	Do not use
3	4 pole	1	1: 4 pole SBU2 to MIC, SBU1 to audio ground 0: others
2	4 pole	1	1: 4 pole SBU1 to MIC, SBU2 to audio ground 0: others
1	3 pole	1	1: 3 pole 0: others
0	No audio accessory	1	1: No audio accessory 0: Reserved

RES Detection/Audio Jack Detection Interrupt Flag

Address: 18h

Reset Value: 8'b 0000_0000

Type: Read Clear

Bits	Name	Size	Description
[7:3]	Reserved	5	Do not use
2	Audio jack detection and configuration	1	0: Audio jack detection and configuration has not occurred 1: Audio jack detection and configuration has occurred
1	Low resistance occurred	1	0: Low resistance has not occurred 1: Low resistance has occurred
0	Low resistance detection	1	0: Low resistance has not occurred 1: Low resistance has occurred

RES/Audio Jack Detection Interrupt Mask

Address: 19h

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:3]	Reserved	5	Do not use
2	Audio jack detection and configuration	1	1: Mask audio jack detection and configuration has occurred interrupt
1	Low resistance occurred	1	1: Low resistance has occurred interrupt
0	Low resistance detection	1	1: Low resistance detection has occurred interrupt

MIC Detection Threshold Data0

Address: 1Ch

Reset Value: 8'b 0010_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	MIC detection threshold DATA0	8	MIC detection threshold DATA0 0010_0000: 300 mV

MIC Detection Threshold Data1

Address: 1Dh

Reset Value: 8'b 1111_1111

Type: Read/Write

Bits	Name	Size	Description
[7:0]	MIC detection threshold DATA1	8	MIC detection threshold DATA1 1111_1111: 2.4 V

I²C Reset

Address: 1Eh

Reset Value: 8'b 0000_0000

Type: W/C

Bits	Name	Size	Description
[7:1]	Reserved	7	Reserved
0	I²C reset	1	0: default 1: I²C reset

Current Source Setting

Address: 1Fh

Reset Value: 8'b 0000_0111

Type: Read/Write

Bits	Name	Size	Description
[7:4]	Reserved	4	Reserved
[3:0]	Current source setting	4	1111: 1500 μA 0111: 700 μA 0001: 100 μA 0000: Invalid

Timing Delay between L Switch Enable and Switch-On Order

Address: 20h

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 102 ms
			11111110: 101.6 ms
			...
			00000001: 400 us
			00000000: 0 us

Application Information

Over-Voltage Protection

DIO4482/B/L/LB feature over−voltage protection (OVP) on the receptacle side pins that turns off the internal signal routing path if the voltage exceeds the OVP threshold. If OVP occurs, pin INT will be pulled down, which is an open-drain output pin. Flag register 0×02h and 0×03h will indicate which pin had an OVP event.

Headset Detection

The DIO4482/B/L/LB integrates the headset unplug detection function by detecting the CC_IN voltage. The function will be active when the device is enabled. Output pin DET will be high when CC_IN is low (CC_IN < 1.2 V), and DET will be low when CC_IN = High (CC_IN > 1.5 V).

	Device Disable	Device Enable
CC_IN < 1.2 V	DET = 0	DET = 1
CC_IN > 1.5 V	DET = 0	DET = 0

MIC Switch Auto−off Function

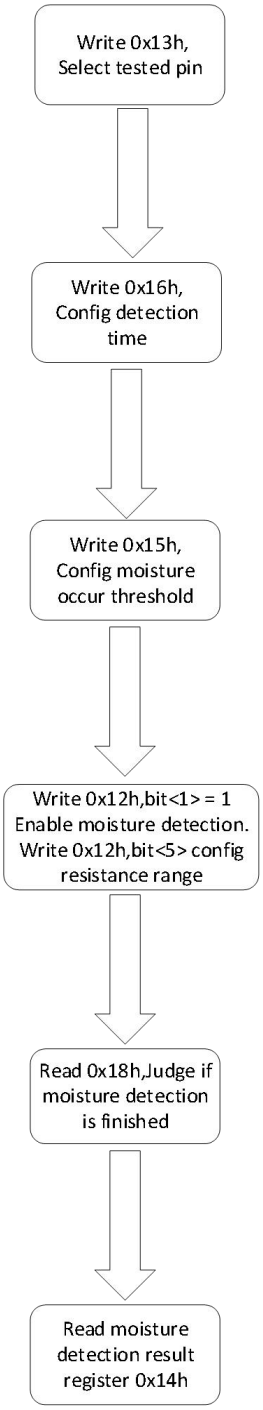
The function is active during control bit 0×12h bit [2] = 1. When CC_IN is changed from low to high and L, R, and AGND switches are under ON status, the MIC switch will be off and the receptacle side pin will be pulled to the ground for 50 μs first. Then it shows that the high−Z status under the MIC switch is set to ON status.

Audio Jack Detection and Configuration

The function is active when control bit 0×12h bit [0] = 1. When the headset is inserted, the DIO4482/B/L/LB can detect OMTP, CTIA, or 3-pole headset and configure pinout automatically. During detection and configuration, the R, L, Sense, MIC, and Audio ground switches will be off. After detection and configuration, R, L, MIC, Sense, and AGND switches will turn on according to detection results and timing control settings.

Moisture Detection

The function is active during control bit 0×12h bit [1] = 1. It will monitor the resistance between receptacle side pins and the ground. The resistance detection pin can be selected by register 0×13h. During moisture detection, the switch, which is monitored, will be off. The detection result will be saved in the resistance flag register 0×14h. The measurement threshold could be from 200 k to 1 MΩ, which is configured by the internal register. The detection interval can be set at single, 100 ms, 1 s, or 10 s by register 0×16h.



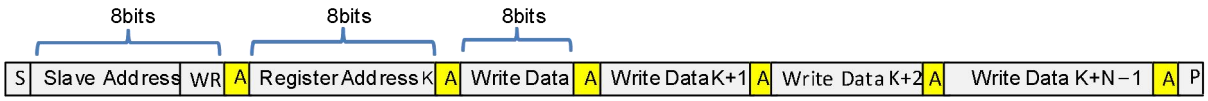
Manual Switch Control

The function is active during control bit 0×12h bit [4] = 1 and 0x04h = FF. It will provide manual control for the device. During this configuration, ADDR and INT pins will be set as a logic control input.

Power	ENN	ADDR	INT	SENSE Switch	Headset Detection	USB Switch	Audio Switch	MIC/Audio GND Switch	SBU by Pass Switch
OFF	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF
ON	H	X	X	OFF	OFF	OFF	OFF	OFF	OFF
ON	L	0	0	OFF	OFF	ON: DP_R to DP DN_L to DN	OFF	OFF	ON: SBU1 to SBU1_H SBU2 to SBU2_H
ON	L	0	1	OFF	OFF	ON: DP_R to DP DN_L to DN	OFF	OFF	ON: SBU1 to SBU2_H SBU2 to SBU1_H
ON	L	1	0	ON GSBU2 to SESNE	ON	OFF	ON: DP_R to R DN_L to L	ON: SBU1 to MIC SBU2 to AGND	OFF
ON	L	1	1	ON GSBU1 to SESNE	ON	OFF	ON: DP_R to R DN_L to L	ON: SBU2 to MIC SBU1 to AGND	OFF

I²C Interface

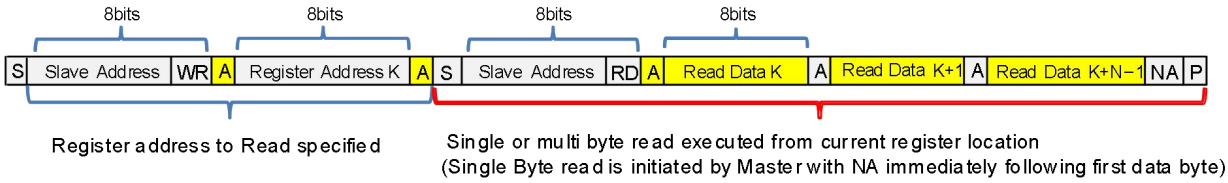
The DIO4482/B/L/LB includes a full I²C slave controller. The I²C slave fully complies with the I²C specification version 2.1 requirements. This block is designed for fast mode, 400 kHz signals. Examples of an I²C write and read sequence are respectively shown in the figures below.



Note:

(1) Single-byte read is initiated by the master with P immediately following the first data byte.

Figure 3. I²C write example



Note:

(1) If the register is not specified, the master will begin reading from current register. In this case, only the sequence showing in the red bracket is needed.

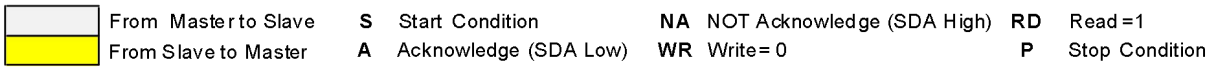
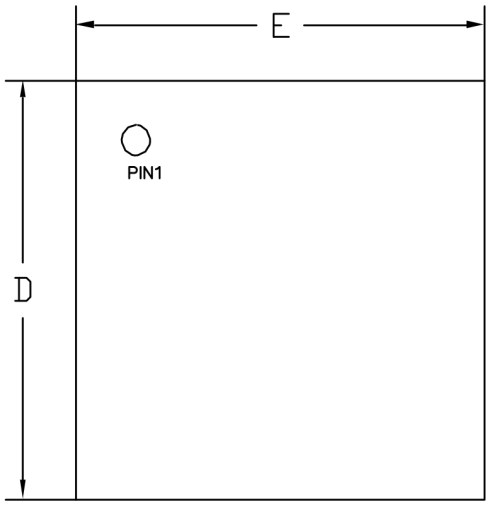
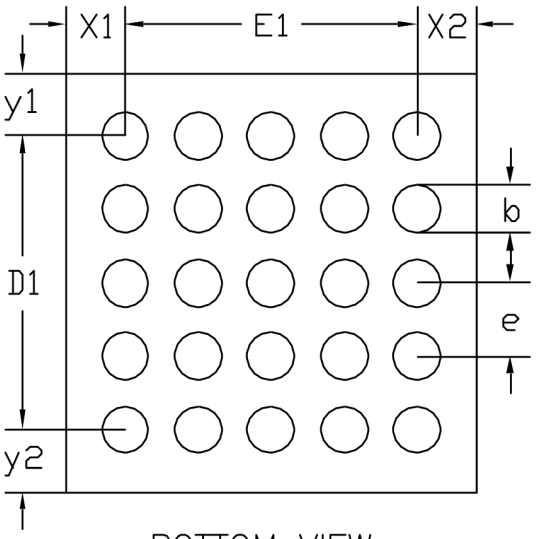


Figure 4. I²C read example

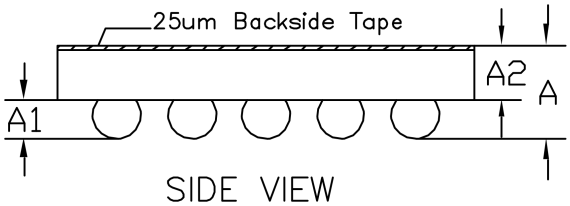
Physical Dimensions: WLCSP-25



TOP VIEW
(MARK SIDE)



BOTTOM VIEW
(BALL SIDE)



SIDE VIEW

Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.547	0.586	0.625
A1	0.190	0.210	0.230
A2	0.351	0.376	0.401
D	2.250	2.280	2.310
D1		1.600 BSC	
E	2.210	2.240	2.270
E1		1.600 BSC	
b	0.238	0.258	0.278
e		0.400 BSC	
x1		0.320 REF	
x2		0.320 REF	
y1		0.340 REF	
y2		0.340 REF	

CONTACT US

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