DIO2673
Three-Channel, 6th-Order 80MHz, 1080p HD Video Filter Driver

Features

- Triple 6th-order 80MHz HD filters
- 6dB Output Driver Gain and Drive Dual Video Load
- Transparent Input Clamping
- Fixed 6dB Gain
- AC or DC Coupled Inputs
- AC or DC Coupled Outputs
- Operates from 3.135V to 5.25V
- Single Power Supply
- RoHS or Green EP-SOIC8 Package
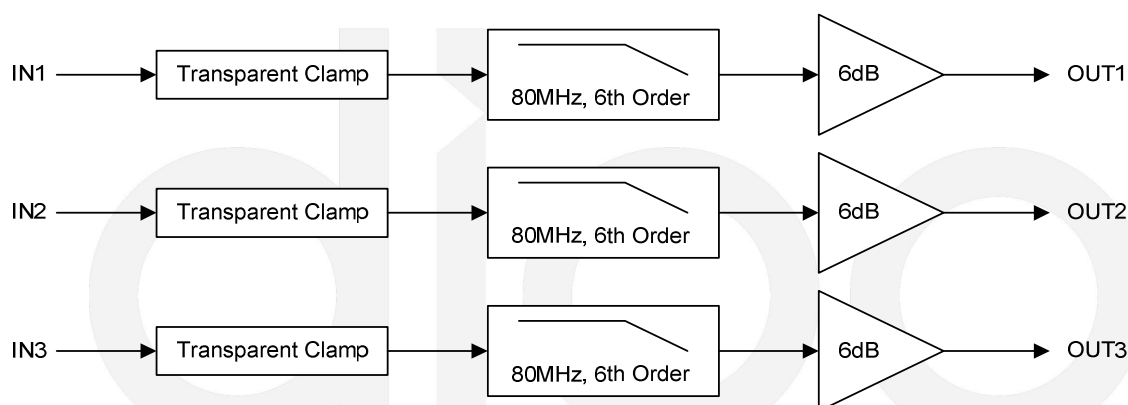- 6500V ESD protection

Applications

- DVD Players
- Video Amplifiers
- Cable set-top boxes
- Personal Video Recorders
- Communications Devices
- Video on Demand

Descriptions

DIO2673 is a low voltage, triple video amplifier with integrated 6dB reconstruction filter and input clamps. All three channels can accept Component and RGB video signals. In fact, DIO2673 is a triple HD video drvier. It can improve image quality compared to the passive LC filters.

All channels can be directly driven by a DC-coupled or an AC-coupled signal. Internal diode-like clamps and bias circuitry may be used if AC-coupled inputs are required. The output in DIO2673 can also drive AC or DC coupled single (150Ω) or dual (75Ω) loads. The DC coupling capacitors can be removed.

Block Diagram

Ordering Information

Order Part Number	Top Marking		T_A	Package	
DIO2673XS8	DIO2673	RoHS or Green	-40 to +85°C	EP-SOIC8	Tape & Reel, 2500

Pin Assignments

EP-SOIC8 (Top View)

Figure 1   Pin Assignment (Top View)

Pin Description

Pin	Name	Description
1	IN1	Channel HD Video Input (Pr)
2	IN2	Channel HD Video Input (Pb)
3	IN3	Channel HD Video Input (Y)
4	V_{CC}	Power supply
5	GND	Ground
6	OUT3	Channel HD Video Output (Y)
7	OUT2	Channel HD Video Output (Pb)
8	OUT1	Channel HD Video Output (Pr)

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Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maxim rating conditions for extended periods may affect device reliability.

Parameter		Rating	Unit
Supply Voltage		-0.3 to 6.0	V
Input Voltage		-0.3 to V_{CC}+0.3	V
Storage Temperature Range		-65 to 150	°C
Junction Temperature		150	°C
Lead Temperature Range		260	°C
SOIC-8 Θ_{JA}		130	°C/W
ESD	HBM, JEDEC: JESD22-A114	6500	V
	CDM, JEDEC: JESD22-C101	2000	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation to ensure optimal performance to the datasheet specifications. DIOO does not recommend exceeding them or designing to Absolute Maximum Ratings.

Parameter	Rating	Unit
Supply Voltage	3.135 to 5.25	V
Operating Temperature Range	-40 to 85	°C

Electrical Characteristics

Typical value: T_A = 25°C, V_{CC}=5V, R_{SOURCE}=37.5Ω, R_L=150Ω loads; referenced to 400kHz, all inputs are AC couple with 0.1μF; all outputs are AC coupled with 220μF; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC ELECTRICAL CHARACTERISTICS						
I_{CC}	Supply Current			78	90	mA
V_{IN}	Video Input Voltage Range		GND		1.4	V_{PP}
PSRR	Power Supply Rejection			-60		dB
DYNAMIC PERFORMANCE						
AV	Channel Gain		5.8	6.0	6.2	dB
BW	Band Width	-1dB, R_{SOURCE}=75Ω		58		MHz
		-3dB, R_{SOURCE}=75Ω		80		
AR	Attenuation	f=148MHz, R_{SOURCE}=75Ω		-27		dB
THD	Output Distortion	V_{OUT}=1.4V_{PP}, f=10MHz		0.6	1.4	%
		V_{OUT}=1.4V_{PP}, f=20MHz		0.8	2.0	
X_{TALK}	Crosstalk	f=1MHz, V_{IN}=1.4V_{PP}		-75		dB
SNR	Signal to Noise Ratio	100kHz to 30MHz, 100% White Signal		65		dB
	Group Delay	100kHz to 30MHz		5		ns
	Propagation Delay	Input to Output		20		ns
SR	Slew Rate	2V Output 80% to 20%		100		V/μs

Notes: SNR=20 • log (714mV / rms noise).

Specifications subject to change without notice.
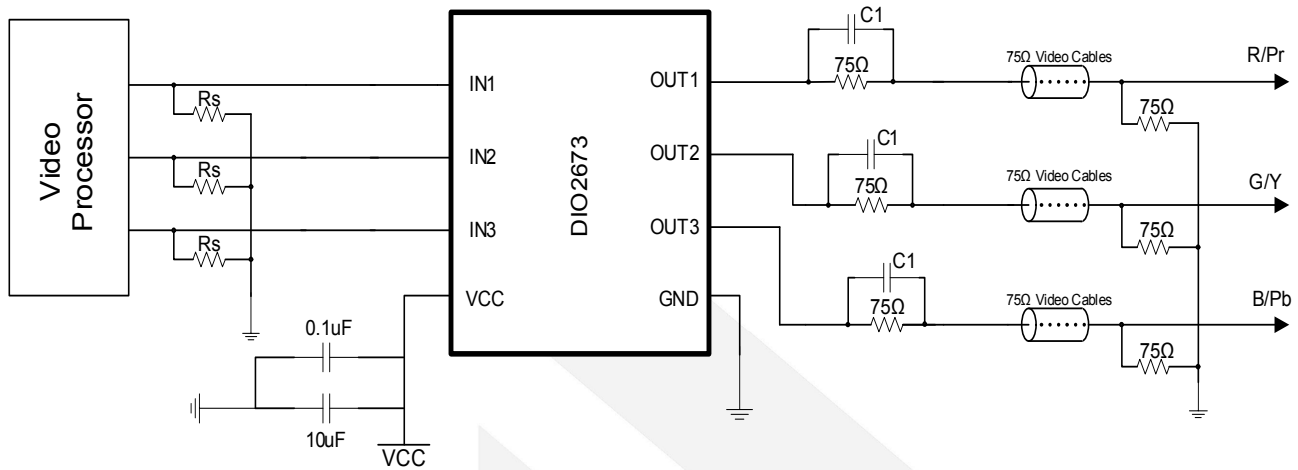
Application Circuit

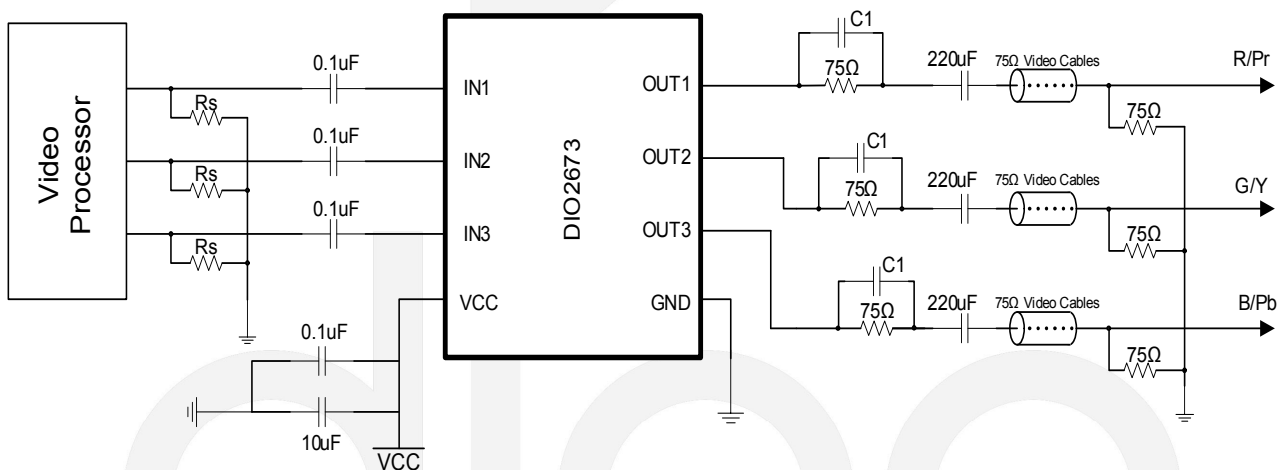**Figure 2   Input and Output DC-Coupling Application**

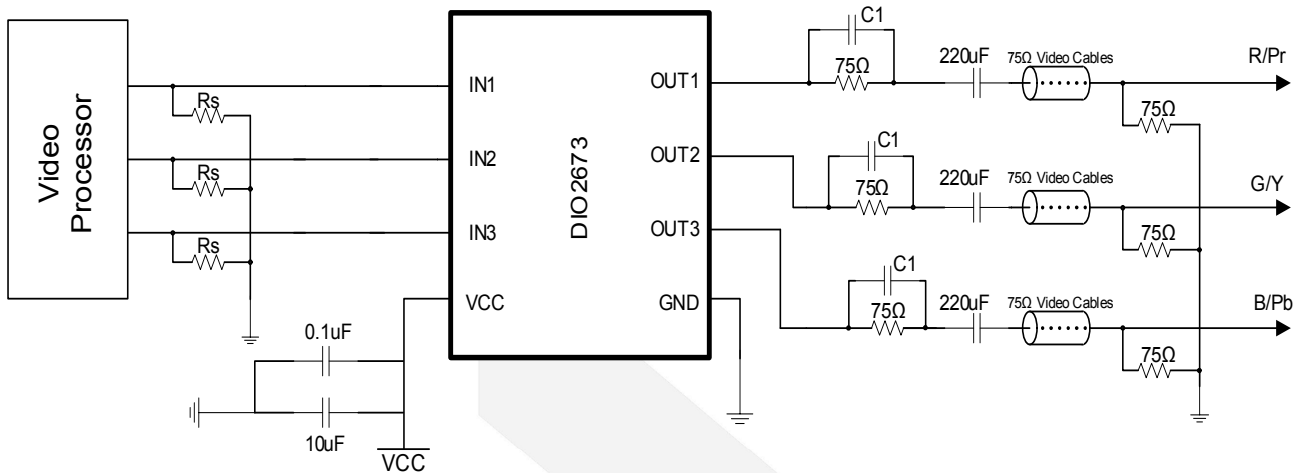**Figure 3   Input and Output AC-Coupling Application**

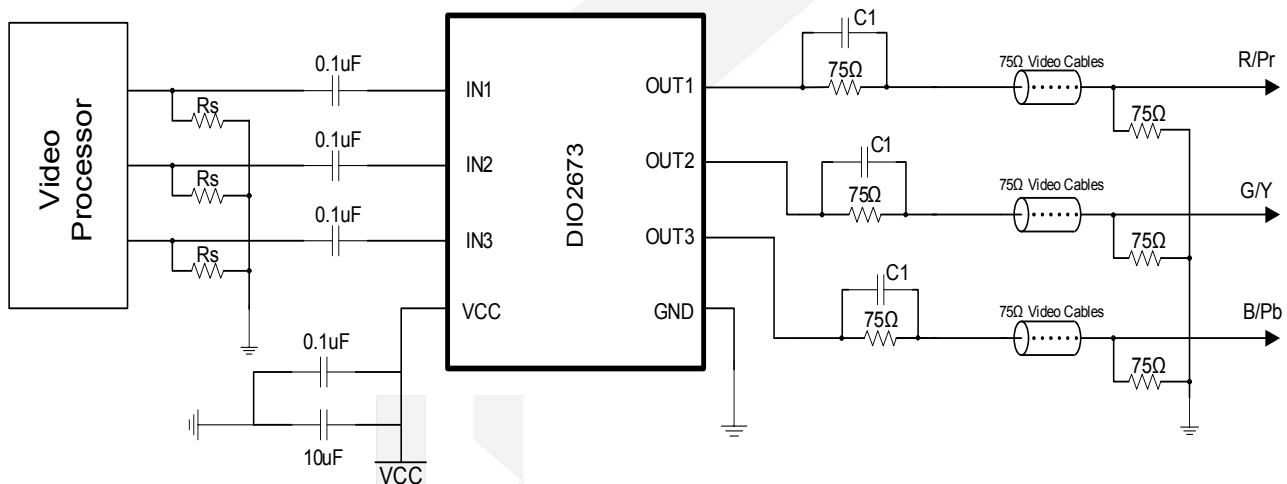**Figure 4   Input DC-Coupling and Output AC-Coupling Application**

Figure 5   Input AC-Coupling and Output DC-Coupling Application

Note: The value of C1 is recommended 2 to 4pf

DIO2673 can also drive double load.

Applications Information

Functional Description

The DIO2673 Low-Cost Video Filter provides 6dB gain from input to output. In addition, the input is slightly offset to optimize the output driver performance. The offset is held to the minimum required value to decrease the standing DC current into the load. Typical voltage levels are shown in Figure 6.
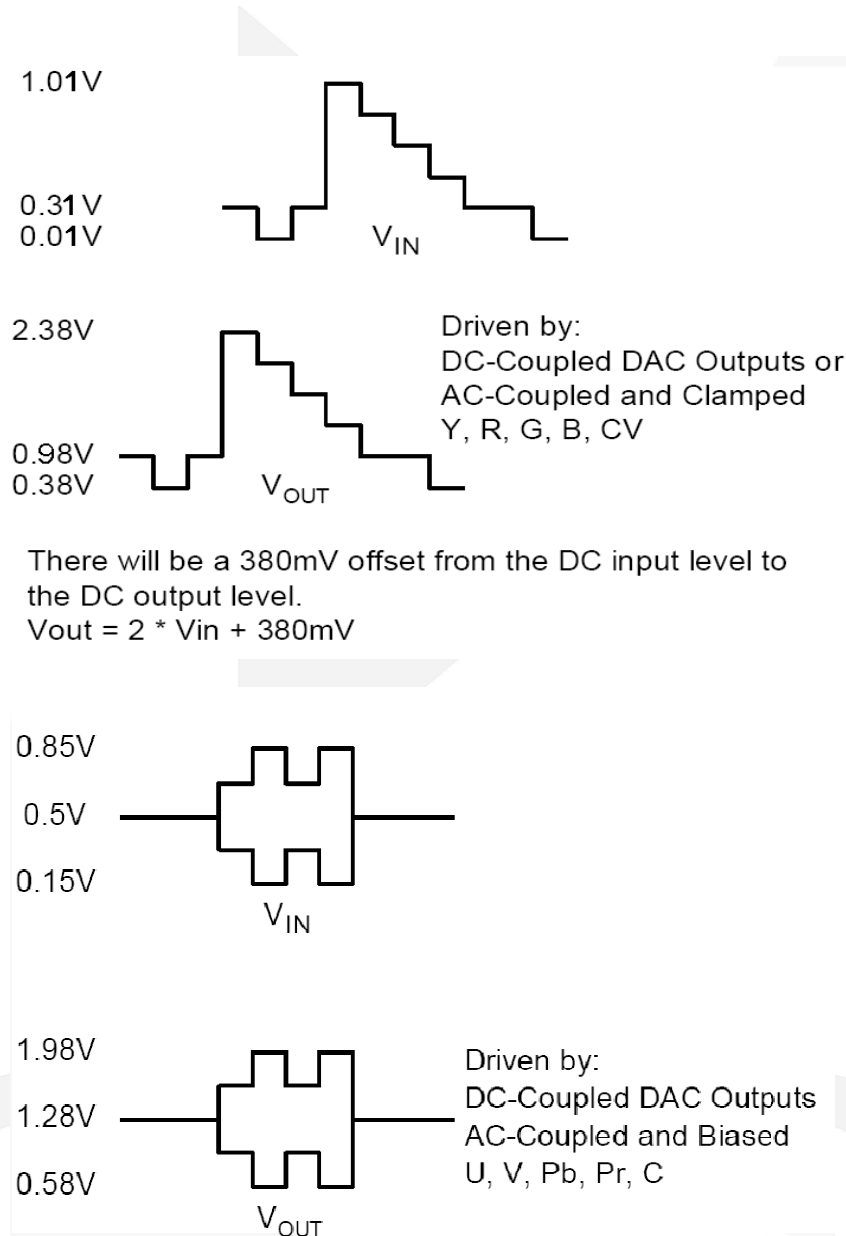

There will be a 380mV offset from the DC input level to the DC output level.

Vout = 2 * Vin + 380mV

Figure 6. Typical Voltage Levels

The DIO2673 provides an internal diode clamp to support AC coupled input signals. If the input signal does not go below ground, the input clamp does not operate. This allows DAC outputs to directly drive the DIO2673 without an AC coupling capacitor. The worst-case sync tip compression due to the clamp does not exceed 7mV. The input level set by the clamp, combined with the internal DC offset, keeps the output within its acceptable range. When the input is AC-coupled, the diode clamp sets the sync tip (or lowest voltage) just below ground.

For symmetric signals like Pb and Pr; the average DC bias is fairly constant and the inputs can be AC-coupled with the addition of a pull-up resistor to set the DC input voltage. DAC outputs can also drive these same signals without the AC coupling capacitor. A conceptual illustration of the input clamp circuit is shown in Figure 7.
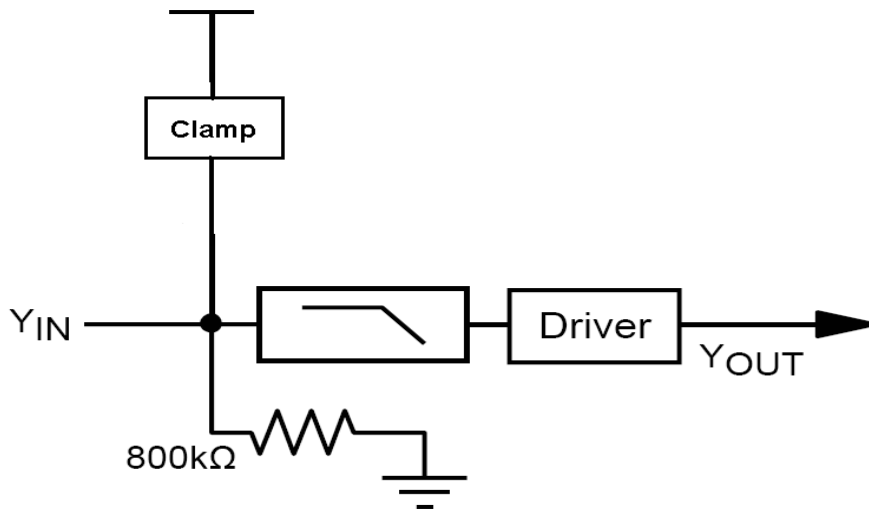

Figure 7. Input Clamp Circuit

I/O Configurations

For DC-coupled DAC drive with DC-coupled outputs, use the configuration in Figure 8.
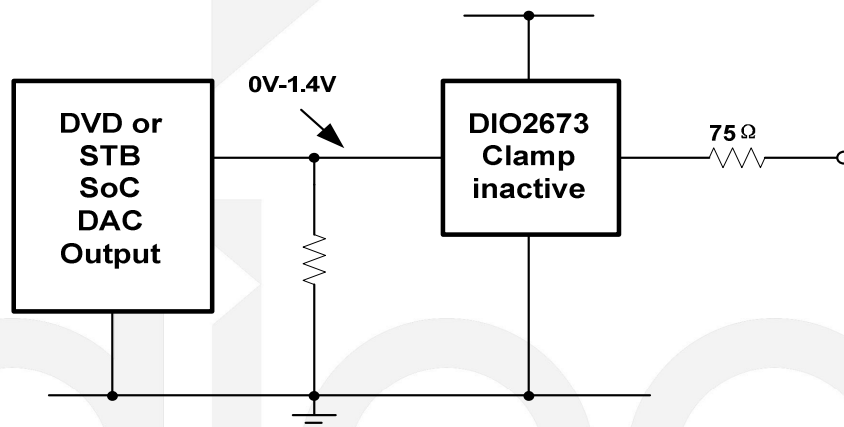

Figure 8. DC-coupled Inputs and Outputs

Alternatively, if the DAC's average DC output level causes the signal to exceed the range of 0V to 1.4V, it can be AC-coupled, as shown in Figure 9.
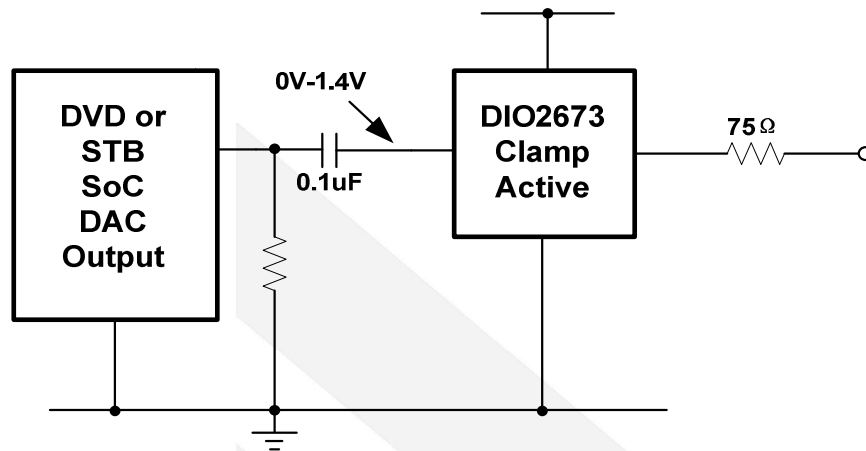

Figure 9. AC-coupled Inputs, DC-coupled Outputs

When the DIO2673 is driven by an unknown external source or a SCART with its own clamping circuitry the inputs should be AC-coupled, shown in Figure 10.
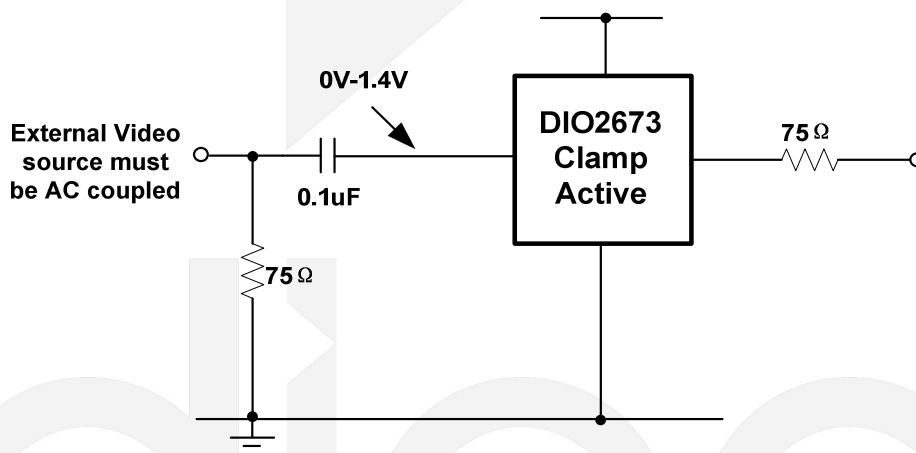

Figure 10. SCART with DC-coupled Outputs

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The same method can be used for biased signals with the addition of a pull-up resistor to make sure the clamp never operates. The internal pull-down resistance is 800kΩ ±20%, so the external resistance should be 7.5MΩ to set the DC level to 500mV. If a pull-up resistance of less than 7.5MΩ desired, add an external pull-down such that the DC input level is set to 500mV.
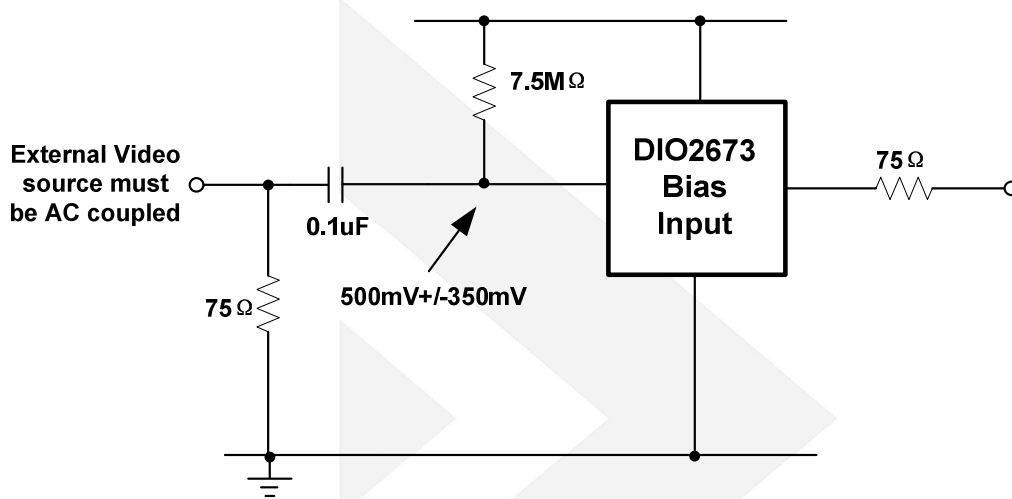

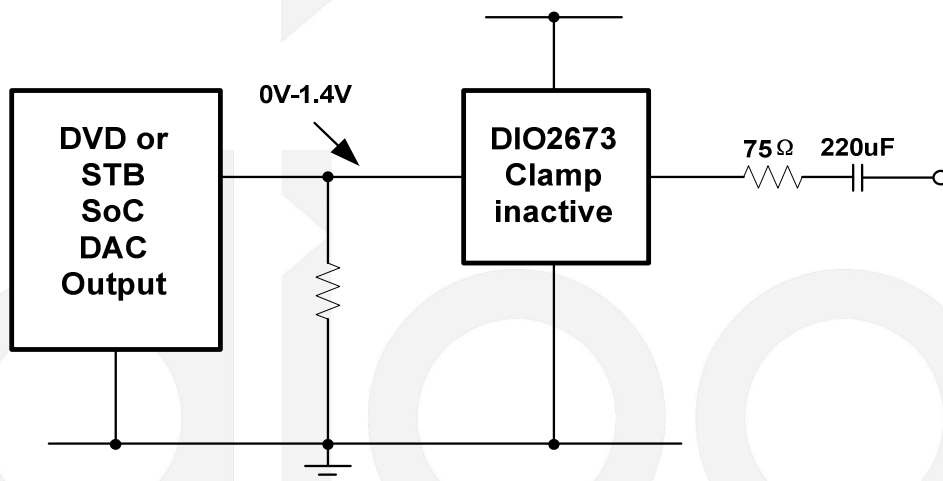**Figure 11. Biased SCART with DC-coupled Outputs**

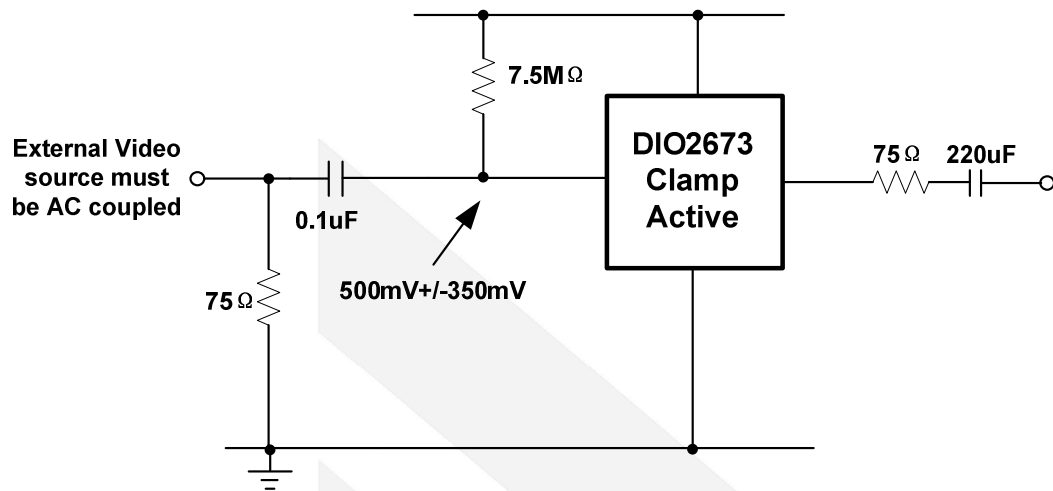**Figure 12. DC-coupled Inputs, AC-coupled Outputs**

Figure 13. Biased SCART with AC-Coupled Outputs

Note: The video tilt or line time distortion is dominated by the AC-coupling capacitor. The value may need to be increased beyond 220μF to obtain satisfactory operation in some applications.

Power Dissipation

The DIO2673 output drive configuration must be considered when calculating overall power dissipation. Care must be taken not to exceed the maximum die junction temperature. The following example can be used to calculate the DIO2673's power dissipation and internal temperature rise.

$T_J = T_A + P_d \cdot \Theta_{JA}$ where $Pd = P_{CH1} + P_{CH2} + P_{CH3}$

and $P_{CHx} = V_S \cdot I_{CH} - (V_{O2}/R_L)$

Where $V_O = 2V_{IN} + 0.380V$

$I_{CH} = (I_{CC}/3) + (V_O/R_L)$

V_{IN} = RMS value of input signal

I_{CC} = 78mA

V_S = 5V

R_L = channel load resistance

Board layout affects thermal characteristics. *Refer to the Layout Considerations section for more information*.

The DIO2673 is specified to operate with output currents typically less than 50mA, more than sufficient for a single (150Ω) video load. Internal amplifiers are current limited to a maximum of 120mA and should withstand brief duration, short-circuit conditions; however, this capability is not guaranteed.
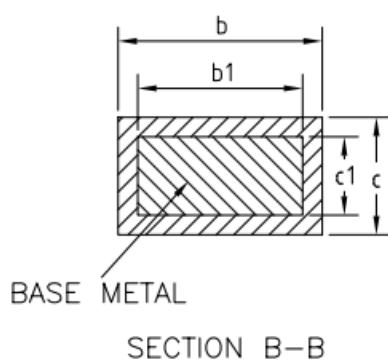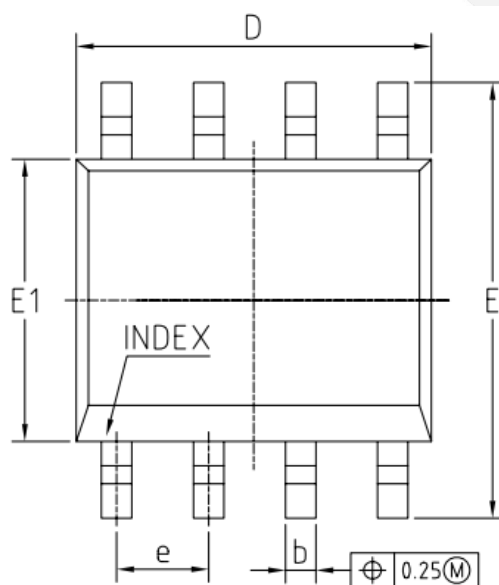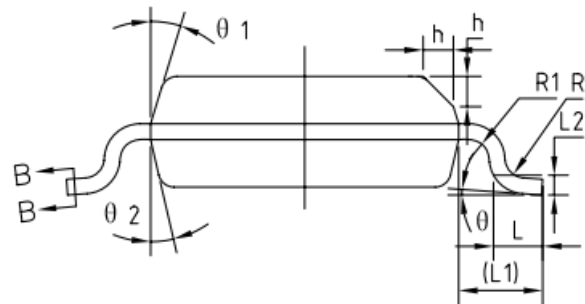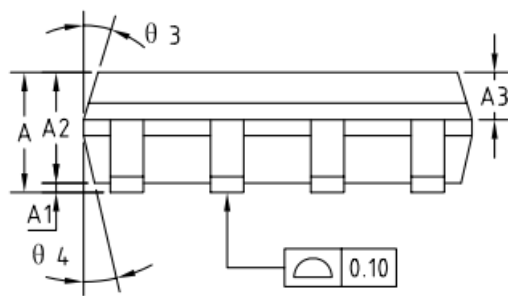
Layout Consideration

Layout and supply bypassing play major roles in high frequency performance and thermal characteristics.

For optimum results, follow the steps below as a basis for high-frequency layout:

■ Include 10μF and 0.1μF ceramic bypass capacitors

■ Place the 10μF capacitor within 0.75 inches of the power pin.

■ Place the 0.1μF capacitor within 0.1 inches of the power pin.

■ Connect all external ground pins as tightly as possible, preferably with a large ground plane under the package.

■ Layout channel connections to reduce mutual trace inductance.

■ Minimize all trace lengths to reduce series inductances. If routing across a board, place device such that longer traces are at the inputs rather than the outputs. If using multiple, low-impedance DC coupled outputs, special layout techniques may be

■ employed to help dissipate heat.

If a multilayer board is used, a large ground plane directly under the device helps reduce package case temperature.

For dual-layer boards, an extended plane can be used. Worst-case additional die power due to DC loading can be estimated at $(I^2*Rload)$ per output channel. $75*(2.8/75)^2*3*50\% = 156.8mW$, total.

Physical Dimensions: EP-SOIC-8

BASE METAL

SECTION B-B

COMMON DIMENSIONS (UNITS OF MEASURE=MILLIMETER)			
Symbol	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.15	0.25
A2	1.25	1.40	1.65
A3	0.50	0.60	0.70
b	0.38	-	0.51
b1	0.37	0.42	0.47
c	0.17	-	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	-	-
R1	0.07	-	-
h	0.30	0.40	0.50
Θ	0°	-	8°
Θ1	15°	17°	19°
Θ2	11°	13°	15°
Θ3	15°	17°	19°
Θ4	11°	13°	15°

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CONTACT US

Dioo is a professional design and sales corporation for high-quality and performance analog semiconductors. The company focuses on industry markets, such as, cell phone, handheld products, laptop, and medical equipments and so on. Dioo's product families include analog signal processing and amplifying, LED drivers and charger IC. Go to http://www.dioo.com for a complete list of Dioo product families.

For additional product information, or full datasheet, please contact with our Sales Department or Representatives.

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