

## DIO2112H

# 2-Vrms Audio Driver with Adjustable Gain

## Features

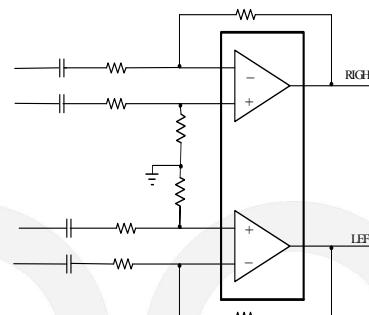
- Voltage Output at 10kΩ Load  
2 Vrms With 3.3V Supply Voltage
- Ultra Low Distortion  
SNR>100dB  
Typical  $V_n < 10\mu V_{rms}$   
 $THD+N < 0.001\%$  at 2Vrms
- No Pop/Clicks Noise when Power ON/OFF
- No Need for Output DC-Blocking Capacitors
- Optimized Frequency Response between 20Hz–20kHz
- Accepting Differential Input
- Featuring external under voltage mute
- Available in TSSOP-14 and DQFN-16 Package

## Descriptions

The DIO2112H is an integrated solution for Set-top box and high definition player, and designed to optimize the audio driver circuit performance while reducing the BOM cost by eliminating the peripheral discrete components for noise reduction. DIO2112H features a 2Vrms stereo audio driver that designed to allow for the removal of output AC-coupling capacitors. Featuring differential input mode, gain range of  $\pm 1$  V/V to  $\pm 10$  V/V can be achieved via external gain resistor setting. The DIO2112H is able to offer 2Vrms output with 10kΩ load and 3.3V supply.

Meanwhile, the DIO2112H offers built-in shut-down control circuitry for optimal pop-free performance. Under the under-voltage condition, DIO2112H is able to detect it and mutes the output.

## Block Diagram



## Applications

- Set-Top Boxes
- High Definition DVD Players
- Car Entertainment System
- Medical

## Ordering Information

Order Part Number	Top Marking		T <sub>A</sub>	Package	
DIO2112HTP14	DIO2112H	Green/RoHS	-40 to +85°C	TSSOP-14	Tape & Reel, 2500
DIO2112HLN16	D21	Green	-40 to +85°C	DQFN-16	Tape & Reel, 3000

## Pin Assignment

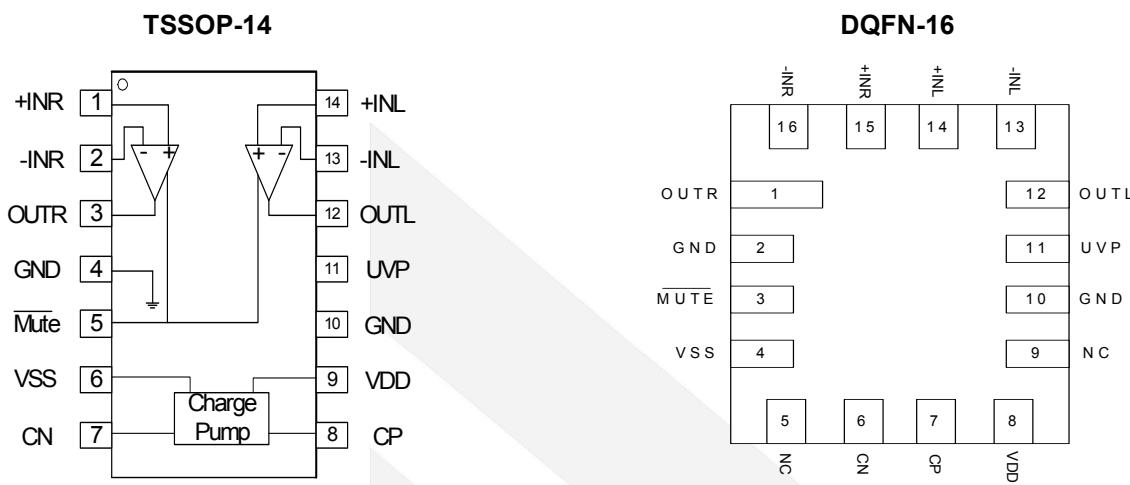


Figure 1 Top View

## Pin Descriptions

PIN Name	I/O	Description
+INR	I	Right-channel positive input
-INR	I	Right-channel negative input
OUTR	O	Right-channel output
GND	P	Ground
Mute	I	Mute input, active-low
VSS	P	Negative Supply
CN	I/O	Charge-pump flying capacitor negative terminal
CP	I/O	Charge-pump flying capacitor positive terminal
VDD	P	Positive supply
UVP	I	Under voltage protection input
OUTL	O	Left-channel output
-INL	I	Left-channel negative input
+INL	I	Left-channel positive input



## DIO2112H

### Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Rating	Unit
Supply Voltage	-0.3 to 4	V
Input Voltage	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Minimum load impedance	>600	$\Omega$
EN to GND	-0.3 to $V_{DD}+0.3$	V
Storage Temperature Range	-65 to 150	$^{\circ}\text{C}$
Junction Temperature	150	$^{\circ}\text{C}$
TSSOP-14, $\Theta_{JA}$	115	$^{\circ}\text{C}/\text{W}$
TSSOP-14, $\Theta_{JC}$	50	$^{\circ}\text{C}/\text{W}$
HBM ESD, JESD22-A114	Output Pins	8
	Others	5
CDM ESD, JESD22-C101E	1	kV

### Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{DD}$	Supply Voltage	3.0	3.3	3.6	V
$V_{IH}$	Mute High level Input Voltage		60		% of $V_{DD}$
$V_{IL}$	Mute Low level Input Voltage		40		% of $V_{DD}$
$T_A$	Operating Temperature Range	-40		85	$^{\circ}\text{C}$

**DIO2112H**

## Electrical Characteristics

Typical value:  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{os}$	Output Offset Voltage	$V_{DD}=3.3\text{V}$ , Input grounded, Unity gain		0.8		$\text{mV}$
PSRR	Power supply rejection ratio	$V_{DD}=3.3\text{V}$		90		$\text{dB}$
$V_{OH}$	High level output voltage	$V_{DD}=3.3\text{V}$ , $R_L=10\text{k}\Omega$	3.1			$\text{V}$
$V_{OL}$	Low level output voltage	$V_{DD}=3.3\text{V}$ , $R_L=10\text{k}\Omega$			-3.05	$\text{V}$
$I_{IH}$	EN High level input current	$V_{DD}=3.3\text{V}$ , $V_I=V_{DD}$			1	$\mu\text{A}$
$I_{IL}$	EN Low level input current	$V_{DD}=3.3\text{V}$ , $V_I=0\text{V}$			1	$\mu\text{A}$
$I_{DD}$	Supply current	$V_{DD}=3.3\text{V}$ , $V_I=V_{DD}$ , No load		16		$\text{mA}$
		Mute mode, $V_{DD}=3.3\text{V}$		0.8		

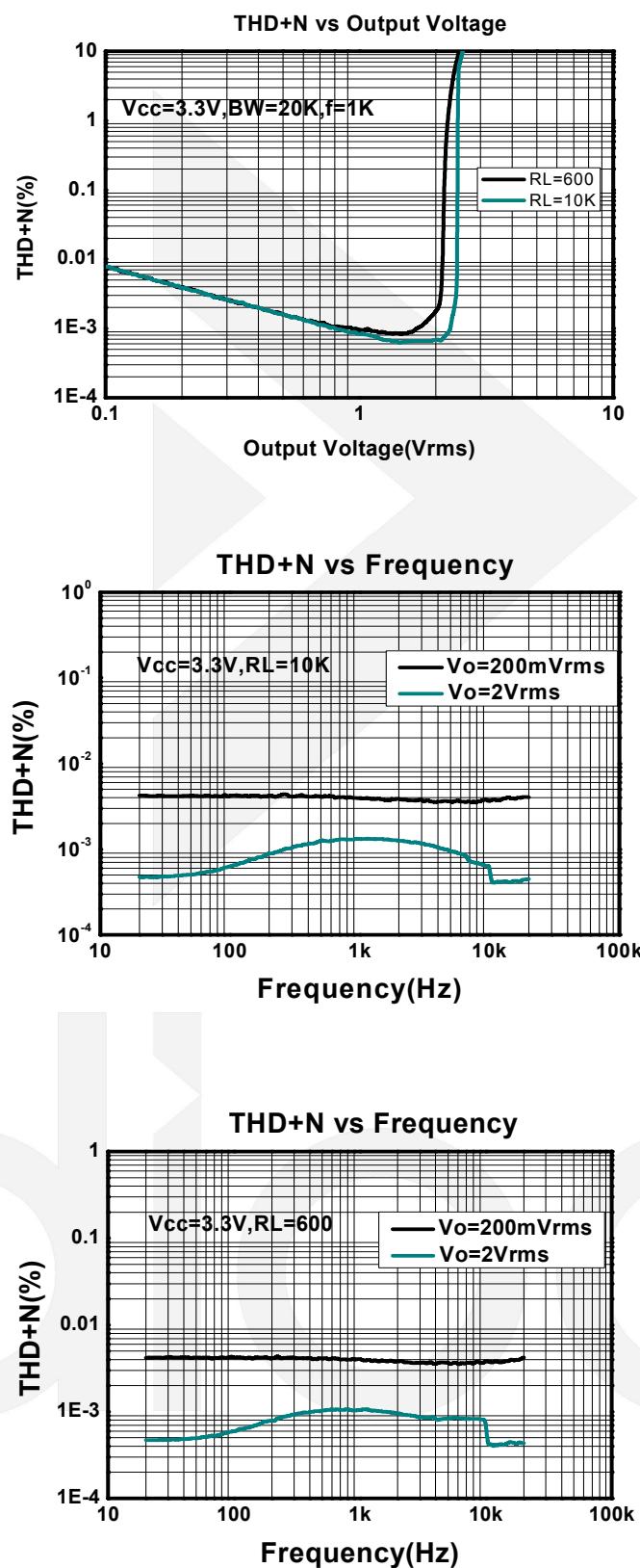
## Operating Characteristics

Typical value:  $V_{DD}=3.3\text{V}$ ,  $R_L=10\text{k}\Omega$ ,  $C_{PUMP}=C_{PVSS}=1\mu\text{F}$ ,  $R_{IN}=15\text{k}\Omega$ ,  $R_{fb}=30\text{k}\Omega$ ,  $T_A=25^\circ\text{C}$ , unless otherwise specified.

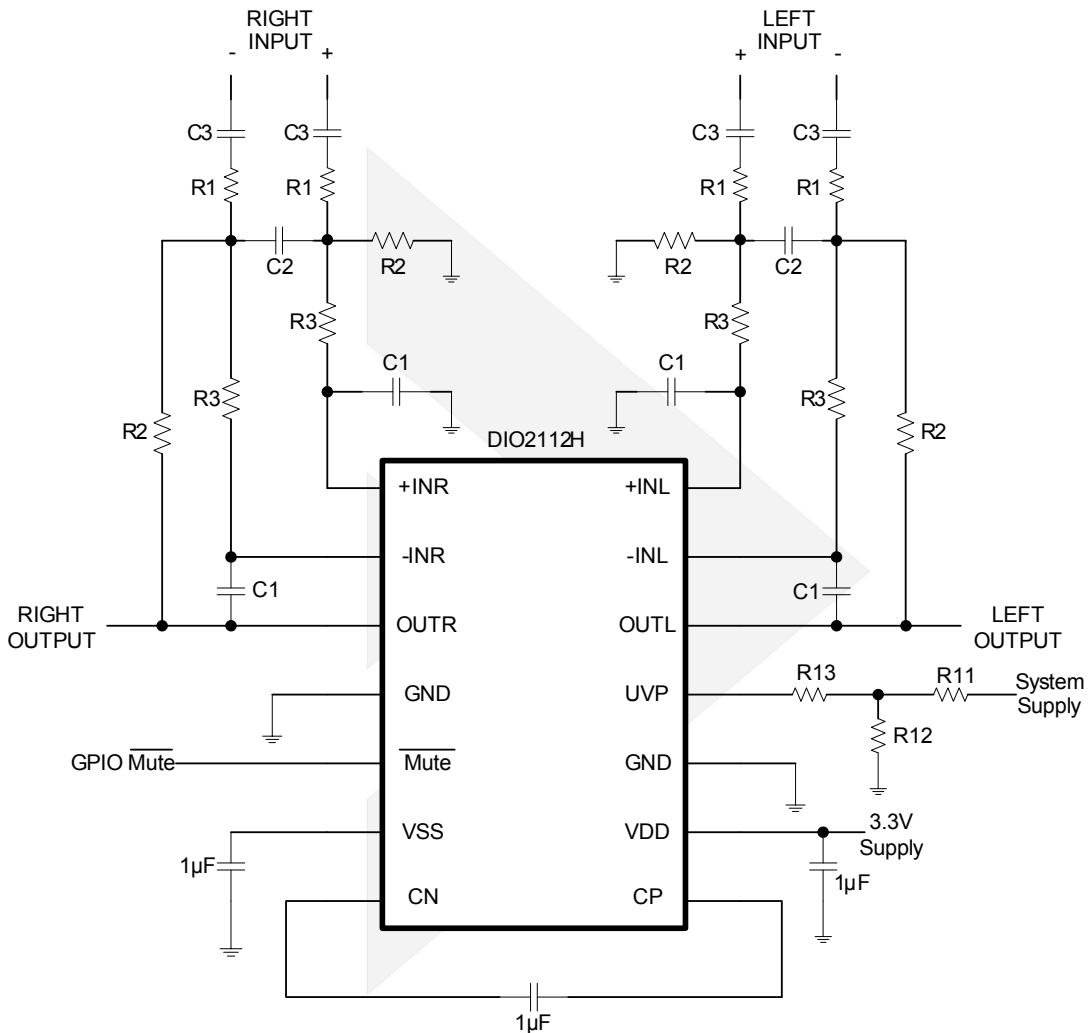
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_o$	Output Voltage	$\text{THD+N}=1\%$ , $V_{DD}=3.3\text{V}$ , $f=1\text{kHz}$	2.0	2.3		$\text{V}_{\text{RMS}}$
$\text{THD+N}$	Total harmonic distortion + noise	$V_o=2\text{V}_{\text{RMS}}$ , $f=1\text{kHz}$		0.0005		%
$X_{\text{TALK}}$	Channel crosstalk	$V_o=2\text{V}_{\text{RMS}}$		-105		$\text{dB}$
SNR	Signal noise ratio	$V_o=2\text{V}_{\text{rms}}$ , $\text{BW}=22\text{kHz}$ , A-weighted,	90	105		$\text{dB}$
DNR	Dynamic range	A-weighted		105		$\text{dB}$
$C_L$	Maximum capacitive load			220		$\text{pF}$
$V_N$	Noise output voltage	A-weighted		10		$\mu\text{V}_{\text{RMS}}$
$G_{\text{BW}}$	Unity gain bandwidth			7.2		$\text{MHz}$
$A_{\text{vo}}$	Open loop voltage gain			165		$\text{dB}$
$V_{\text{UVP}}$	External under-voltage detection			1.25	1.325	$\text{V}$
$I_{\text{Hys}}$	External under-voltage detection hysteresis current			6		$\mu\text{A}$
$f_{\text{CP}}$	Charge pump frequency			300		$\text{kHz}$

## Typical Performance Characteristics

At  $V_{DD}=3.3V$ ,  $R_L=10k\Omega$ ,  $C_{PUMP}=C_{PVSS}=1\mu F$ ,  $R_{IN}=15k\Omega$ ,  $R_{fb}=30k\Omega$ ,  $T_A = +25^\circ C$ , unless otherwise noted.



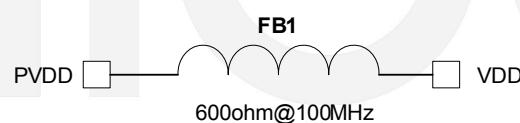
## Application Circuit



Differential-input, single-ended output, second-order filter  
 $R1=15\text{k}\Omega$ ,  $R2=30\text{k}\Omega$ ,  $R3=47\text{k}\Omega$ ,  $C1=33\text{pF}$ ,  $C2=150\text{pF}$ ,  $C3=6.8\mu\text{F}$   
 $R11=2\text{k}\Omega$ ,  $R12=1.69\text{k}\Omega$ ,  $R13=15\text{k}\Omega$

### Important Note:

In some applications, if the power supply noise needs to be filtered, the ferrite bead is recommended in a value of  $600\Omega$ @100MHz, instead of RC network. RC network normally will lower the power supply resulting in the degraded the audio performance. If the resistor is not chosen properly, which can trigger the internal UVP detection circuit and mute the output. As depicted below:



## Application Notes

### Gain-Setting Resistors Ranges and Input-Blocking Capacitors

The gain-setting resistors,  $R_{IN}$  and  $R_{FB}$ , must be chosen so that noise, stability, and input capacitor size of the DIO2112H are kept within acceptable limits. Voltage gain is defined as  $R_{FB}$  divided by  $R_{IN}$ .

Table 1 lists the recommended resistor value for different gain settings. Selecting values that are too low demands a large input ac-coupling capacitor  $C_{IN}$ . Selecting values that are too high increases the noise of the amplifier.

The gain-setting resistor must be placed close to the input pins to minimize capacitive loading on these input pins and to ensure maximum stability.

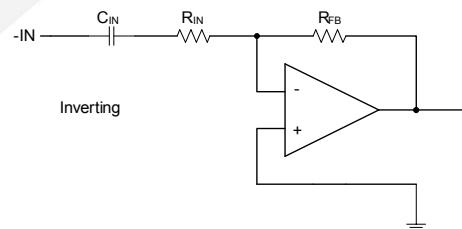
**Table 1 Input Capacitor with 2Hz cutoff and Resistor Values Recommended**

Input Res., $R_{IN}$	Feedback Res., $R_{FB}$	Inverting Gain
22 kΩ	22 kΩ	-1 V/V
15 kΩ	30 kΩ	-2 V/V
10 kΩ	100 kΩ	-10 V/V

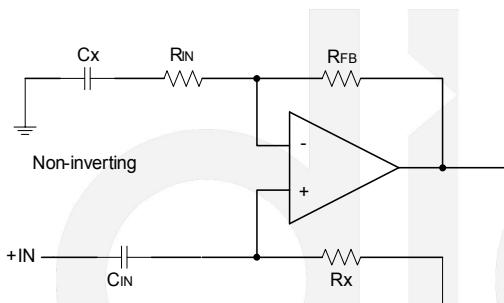
$$f_{CIN} = \frac{1}{2\pi R_{IN} C_{IN}}, \quad \text{or}$$

$$C_{IN} = \frac{1}{2\pi R_{IN} f_{CIN}}$$

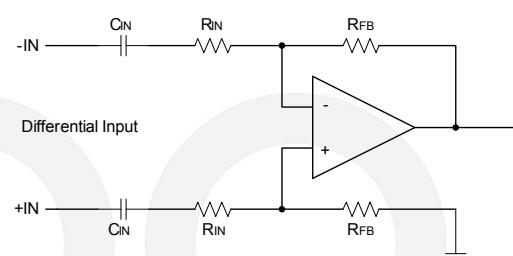
**Equation 1 Cutoff decision Cutoff**



**Figure 2 Inverting Gain Configuration**



**Figure 3 Non-Inverting Gain Configuration**



**Figure 4 Differential Gain Configuration**

## INPUT-BLOCKING CAPACITORS

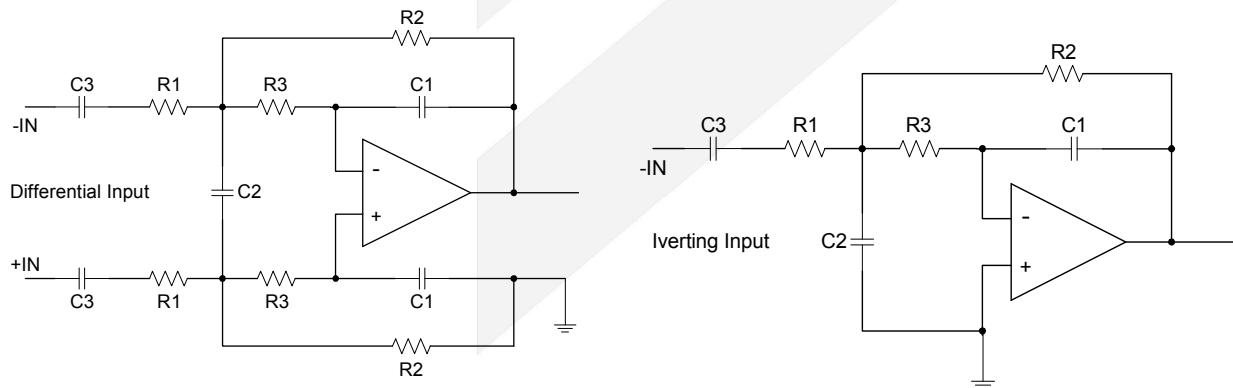
DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the DIO2112H. These capacitors block the dc portion of the audio source and allow the DIO2112H inputs to be properly biased to provide maximum performance.

## 2nd Order Filter Typical Application

Several audio DACs used today require an external low-pass filter to remove out-of-band noise. This is possible with the DIO2112H, as it can be used like a standard OPAMP. Several filter topologies can be implemented, both single-ended and differential. In Figure 5, a multi-feedback (MFB) with differential input and single-ended input is shown.

An ac-coupling capacitor to remove dc content from the source is shown; it serves to block any dc content from the source and lowers the dc-gain to 1, helping reducing the output dc-offset to minimum.

The resistor values should have a low value for obtaining low noise, but should also have a high enough value to get a small size ac-coupling capacitor.



**Figure 5 Second-Order Active Low-Pass Filter**

## Charge Pump Flying Capacitor and VSS Capacitor

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The VSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low-ESR capacitors are an ideal selection, and a value of 1 $\mu$ F is typical. Capacitor values that are smaller than 1 $\mu$ F can be used, but the maximum output voltage may be reduced and the device may not operate to specifications.

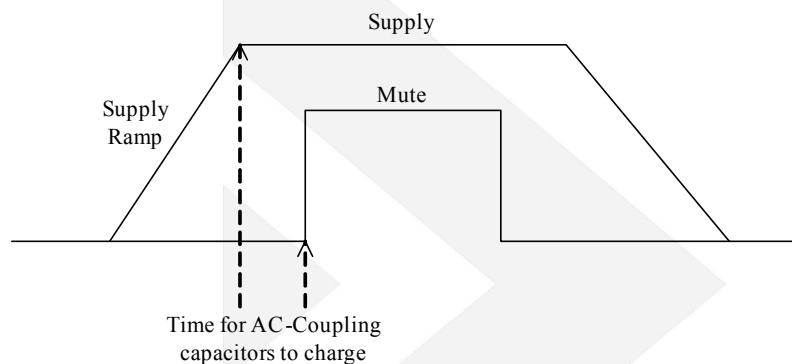
## Decoupling Capacitors

The DIO2112H requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 $\mu$ F, placed as close as possible to the device VDD lead works best. Placing this decoupling capacitor close to the DIO2112H is important for the performance of the amplifier. For filtering lower-frequency noise signals, a 10 $\mu$ F or greater

capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

### Pop-Free Power-Up

Pop-free power up is ensured by keeping the Mute (shutdown pin) low during power-supply ramp up and ramp down. The Mute pin should be kept low until the input ac-coupling capacitors are fully charged before asserting the Mute pin high to achieve pop-less power up. Figure 6 illustrates the preferred sequence.



**Figure 6 Power-Up Sequences**

### External Under-voltage Detection

External under-voltage detection can be used to mute/shut down the DIO2112H before an input device can generate a pop. Although the shutdown voltage is 1.25V typically, customers need to consider the accuracy of system passive components such as resistors and associated temperature variation. In order to guarantee the power-on of the device, usually greater than 1.325V at UVP pin is recommended to cover the possible uncertainty. Users often select a resistor divider to obtain the power-on and shutdown threshold for the specific application. The typical thresholds can be calculated as follows, respectively for VSUP\_MO at 5V and 12V. Usually for best power down noise performance, 12V supply is recommended for UVP circuitry as below. Typically this 12V is the power supply which generates the 5V supply for DIO2112H VDD pins.

Case 1: VSUP\_MO= 12V (**Recommended**)

$$V_{UVP} = (1.25V - 6\mu A \cdot R13) \cdot (R11 + R12) / R12;$$

$$V_{hysteresis} = 5\mu A \cdot R13 \cdot (R11 + R12) / R12;$$

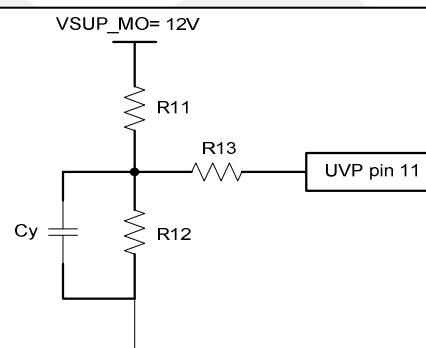
With the condition  $R13 >> R11 // R12$ .

For example, if  $R11 = 11k$ ,  $R12 = 1.4k$  and  $R13 = 47k$ ,

Then  $V_{UVP} = 8.574V$ ;  $V_{hysteresis} = 2.081V$

Here,  $V_{UVP}$  is the shutdown threshold.

In this case, the voltage at UVP pin 11 is greater than 1.325V under worst case of VSUP\_MO ripples.



**Case 2: VSUP\_MO= 5.0V**

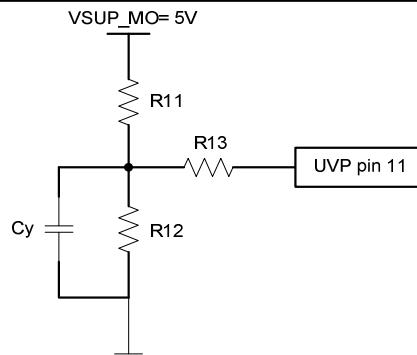
$$V_{UVP} = (1.205V - 6\mu A \cdot R13) \cdot (R11 + R12) / R12;$$

$$V_{hysteresis} = 5\mu A \cdot R13 \cdot (R11 + R12) / R12;$$

With the condition  $R13 >> R11 // R12$ .

For example, if  $R11=5.6k$ ,  $R12=2.2k$  and  $R13=47k$ ,

$$\text{Then } V_{UVP} = 3.83V; V_{hysteresis} = 0.247V$$



Here,  $V_{UVP}$  is the shutdown threshold. In this case, the voltage at UVP pin 11 is greater than 1.325V under worst case of VSUP\_MO ripples.

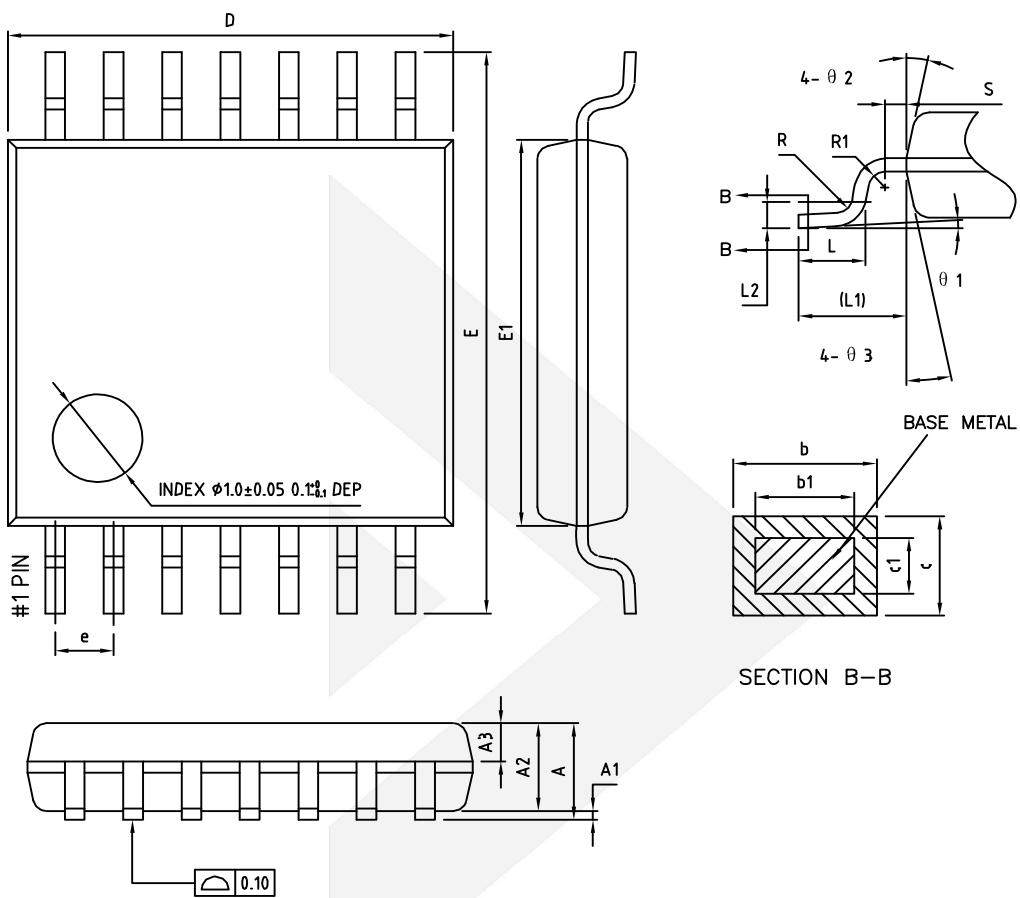
To minimize the system power-up and power-down threshold variations, resistors with less than 1% variations are recommended. Although some resistor value options are offered above for customer's reference or starting points, customers should always verify those resistor options in their actual design. Customer can adjust their own design to achieving the best performance between pop noise and power-on threshold by adjusting the passive resistors R11, R12 and R13.

**Capacitive Load**

The DIO2112H has the ability to drive a high capacitive load up to 220pF directly. Higher capacitive loads can be accepted by adding a series resistor of  $47\Omega$  or larger.

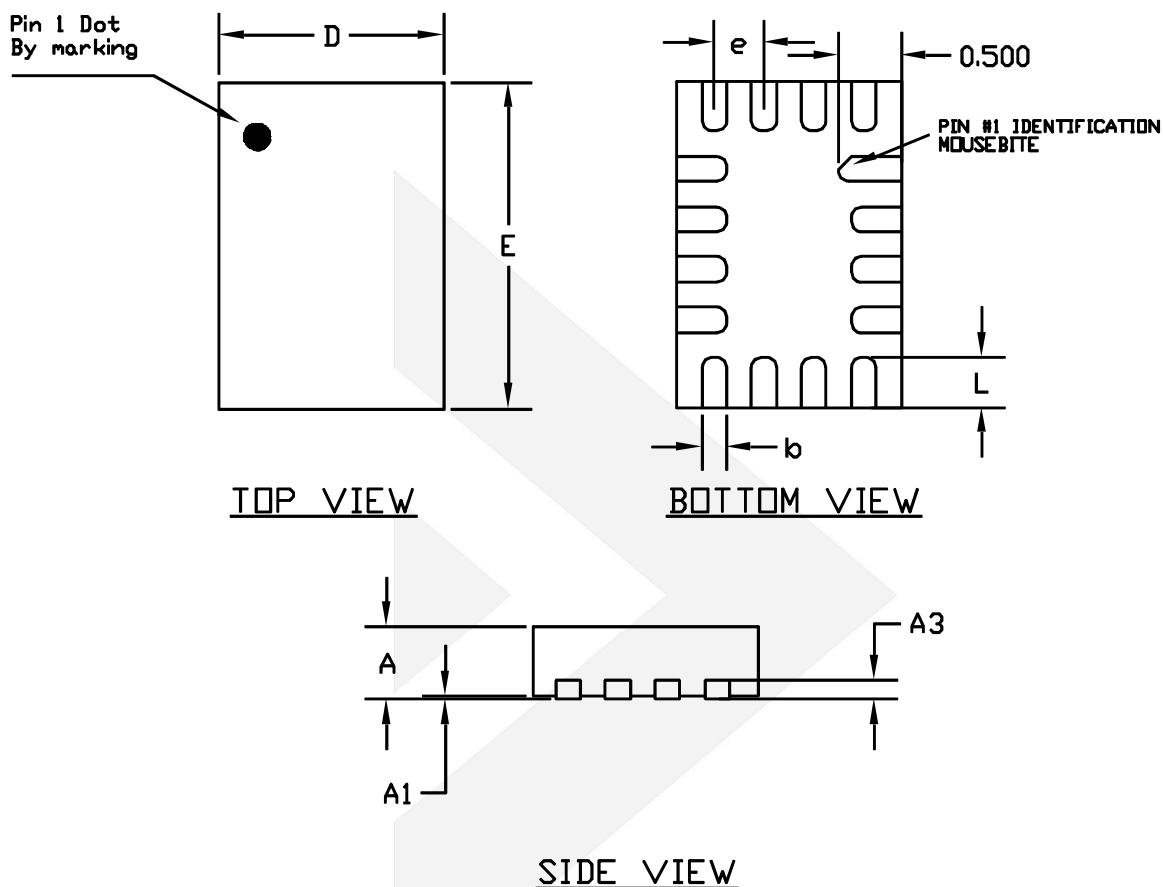
**For further assistance, please contact DIOO worldwide sales office to seek technical support. You can find DIOO sales office information at [www.dioo.com](http://www.dioo.com).**

## Physical Dimensions: TSSOP-14



Symbol	Dimensions In Millimeters		
	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	-	0.28
b1	0.20	0.22	0.24
c	0.10	-	0.19
c1	0.10	0.13	0.15
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e		0.65BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
θ1	0°	-	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

## Physical Dimensions: DQFN-16



Symbol	Dimensions In Millimeters		
	Min	Nom	Max
A	>0.50	0.55	0.60
A1	0.00	-	0.05
A3	0.15 REF		
D	1.75	1.80	1.85
E	2.55	2.60	2.65
L	0.35	0.40	0.45
b	0.15	0.20	0.25
e	0.40 BSC		



### CONTACT US

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