DIO7416

Version 1.0, Oct 2023

Ultra-Low-Voltage I²C Translator with Rise Time Accelerators

Features

- Ultra-low-voltage I²C translator with rise time accelerators
- Operating V_{CC} range: 1.08 V to 3.6 V
- The frequency of SCL: 1 MHz (fast-mode plus)
- Low I_{OFF}: 2.5 μA when either V_{CCA} or V_{CCB} = 0 V
- EN input can be tied directly to V_{CCA} or controlled by GPIO
- 2-bit bidirectional translator for SDA and SCL lines in I²C applications
- Provides bidirectional voltage translation with no direction pin
- Internal 10 kΩ pull-up resistor on all SDA and SCL pins are enabled based on respective V_{CC} voltage
- V_{CC} isolation feature: if either V_{CC} input is at GND, both parts are high impedance
- Either V_{CCA} or V_{CCB} can be ramped first: No power-supply sequencing required
- Operating temperature range: -40°C to 125°C

Applications

- Wearables
- GPIO
- Personal electronics

Package Information

Part Number	Package	Body Size
DIO7416	DFN-8	1.4 mm × 1 mm
	DFN-8	1.35 mm × 0.8 mm
	TSOT23-8	2.9 mm × 1.65 mm

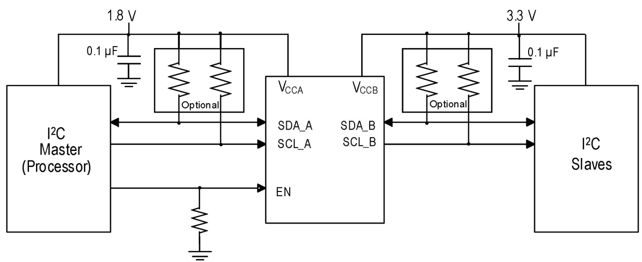
Description

With rising and falling edge accelerators, the DIO7416 is a 2-bit bi-directional I²C voltage translator with enable (EN) pin. Both V_{CCA} and V_{CCB} accept a power supply voltage ranging from 1.08 V to 3.6 V. This allows for low-voltage transmission among 1.2 V, 1.8 V, 2.5 V, and 3.3 V voltage nodes.

Each A port I/O pin of DIO7416 has an internal 10 kΩ pull-up resistor to VCCA and each B port I/O pin has an internal 10 kΩ pull-up resistor to VCCB. The internal pull-up resistors are reverse biased protected, so if the power is turned off, current cannot flow back through the resistors to the power supply.

The enable pin (referenced to V_{CCA}) is 3.6 V tolerant. When the enable pin is high, DIO7416 can achieve level conversion function. When the enable pin is low, the DIO7416 enters shutdown mode. The pull-up resistor is not controlled by the enable (EN) pin. As long as the supply is above V_{UVLO}, the pull-up resistor on one side of it will be enabled.

Simplified Schematic



Ordering Information

Ordering Part No.	Top Marking	MSL	RoHS	T_A	Package	
DIO7416CL8	YWAF	1	Green	-40 to 125°C	DFN1.4*1-8	Tape & Reel, 5000
DIO7416LT8	WA	1	Green	-40 to 125°C	DFN1.35*0.8-8	Tape & Reel, 5000
DIO7416TST8	AFYW	3	Green	-40 to 125°C	TSOT23-8	Tape & Reel, 4000

If you encounter any issue in the process of using the device, please contact our customer service at marketing@dioo.com or phone us at (+86)-21-62116882. If you have any improvement suggestions regarding the datasheet, we encourage you to contact our technical writing team at docs@dioo.com. Your feedback is invaluable for us to provide a better user experience.

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1. Pin Assignment and Functions

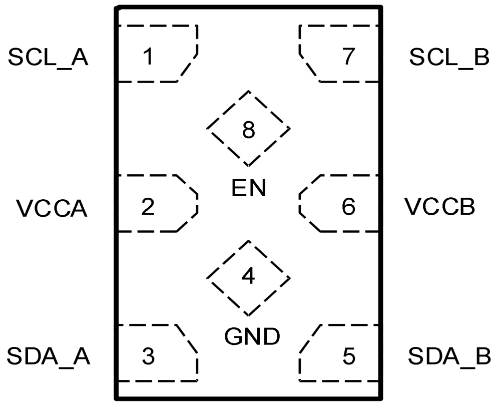


*Figure 1. DFN1.35*0.8-8 (Top view)*

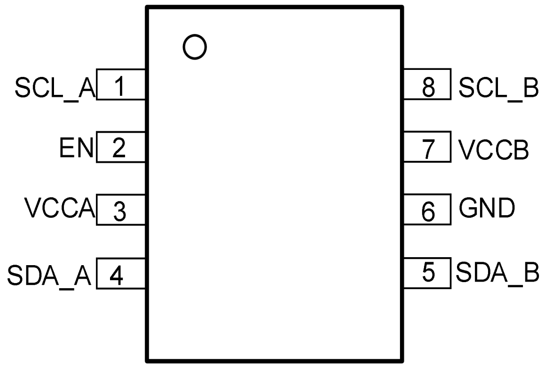


Figure 2. TSOT23-8 (Top view)

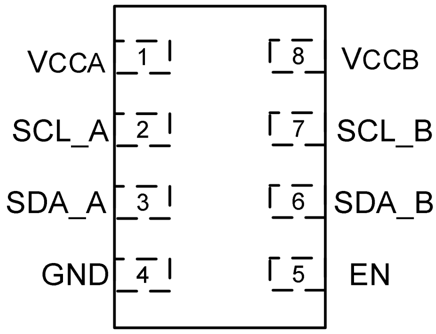


*Figure 3. DFN1.4*1-8 (Top view)*

Name	I/O	Description
SCL_A	I/O	Input/output A. Referenced to V_{CCA}.
VCCA	Power	A-port supply voltage. 1.08 V ≤ V_{CCA} ≤ 3.6 V
SDA_A	I/O	Input/output A. Referenced to V_{CCA}.
GND	GND	Ground
SDA_B	I/O	Input/output B. Referenced to V_{CCB}.
VCCB	Power	B-port supply voltage. 1.08 V ≤ V_{CCB} ≤ 3.6 V
SCL_B	I/O	Input/output B. Referenced to V_{CCB}.
EN	Input	Enable (active high). Pull EN low to enter shutdown mode.

2. Absolute Maximum Ratings

Exceeding the maximum ratings listed under Absolute Maximum Ratings when designing is likely to damage the device permanently. Do not design to the maximum limits because long-time exposure to them might impact the device's reliability. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter		Ratings	Unit
V_{CC}	Supply voltage		-0.5 ~ 4	V
V_I	Input voltage range(1)		-0.5 ~ 4	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(1) (2)	A port	-0.5 ~ 4	V
		B port		
V_O	Voltage range applied to any output in the high or low state(1) (2)	A port	-0.5 ~ 4	V
		B port		
I_{IK}	Input clamp current		-50	mA
I_{OK}	Output clamp current		-50	mA
I_O	Continuous output current		±50	mA
T_{STG}	Storage temperature		-65 ~ 150	°C

Note:

(1) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(2) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

3. Recommended Operating Condition

Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter		V_{CCA}	V_{CCB}	Min	Max	Unit
V_{CCA}	Supply voltage				1.08	3.6	V
V_{CCB}	Supply voltage				1.08	3.6	V
V_I	Input voltage	A-port I/Os, B-port I/Os, EN	0 V to 3.6 V	0 V to 3.6 V	0	3.6	V
V_{IH}	High-level input voltage	EN input	1.08 V to 3.6 V	1.08 V to 3.6 V	V_{CCA} × 0.7	3.6	V
V_{IL}	Low-level input voltage	EN input	1.08 V to 3.6 V	1.08 V to 3.6 V	0	V_{CCA} × 0.3	V
T_A	Operating free-air temperature				-40	125	°C

4. ESD Ratings

When a statically-charged person or object touches an electrostatic discharge sensitive device, the electrostatic charge might be drained through sensitive circuitry in the device. If the electrostatic discharge possesses sufficient energy, damage might occur to the device due to localized overheating.

Model	Metric	Value	Unit
Human-body model	ANSI/ESDA/JEDEC JS-001	±6500	V
Charged-device model	ANSI/ESDA/JEDEC JS-002	±2000	V

5. Thermal Considerations

The thermal resistance determines the heat insulation property of a material. The higher the thermal resistance is, the lower the heat loss. Accumulation of heat energy degrades the performance of semiconductor components.

Symbol	Parameter		Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	DFN1.4*1-8	177.6	°C/W
		DFN1.35*0.8-8	199.3	°C/W
		TSOT23-8	212.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	DFN1.4*1-8	98.7	°C/W
		DFN1.35*0.8-8	26.4	°C/W
		TSOT23-8	105.3	°C/W

6. Electrical Characteristics

6.1. General electrical characteristics

The values are obtained under these conditions unless otherwise specified: T_A = -40°C to 125°C. Typical values are at V_{CC} = 3.6 V, T_A = 25°C.

Symbol	Parameter	Conditions	V_{CCA}	V_{CCB}	Min	Typ	Max	Unit
V_{UVLO_RISE}	UVLO rising threshold	V_{UVLO} for V_{CCA} and V_{CCB} are independent	0 V to 3.6 V	0 V to 3.6 V	0.75	0.9	1	V
V_{UVLO_FALL}	UVLO falling threshold	V_{UVLO} for V_{CCA} and V_{CCB} are independent	0 V to 3.6 V	0 V to 3.6 V	0.73	0.85	0.95	V
V_{RTA}	RTA(2) activation threshold		1.08 V to 3.6 V	1.08 V to 3.6 V		V_{CCI}(1) × 0.5		V
V_{FTA}	FTA(2) activation threshold		1.08 V to 3.6 V	1.08 V to 3.6 V		V_{CCI} × 0.55		V
R_{PU}	Internal pull-up resistor	V_I = 0.15 V	1.08 V to 3.6 V	1.08 V to 3.6 V	7	10	14.5	kΩ
I_I	EN	V_I = V_{CCA} or GND	1.08 V to 3.6 V	1.08 V to 3.6 V	-1	0	+1	μA
I_{OFF}	A port	V_I = 3.6 V, V_O = 0 V (T_A ≤ 85°C)	0 V	0 V to 3.6 V		0.13	2	μA
	B port	V_I = 3.6 V, V_O = 0 V (T_A ≤ 85°C)	0 V to 3.6 V	0 V		0.13	2	μA
	A port	V_I = 3.6 V, V_O = 0 V (T_A ≤ 125°C)	0 V	0 V to 3.6 V		0.13	6.8	μA
	B port	V_I = 3.6 V, V_O = 0 V (T_A ≤ 125°C)	0 V to 3.6 V	0 V		0.13	6.8	μA
I_{CC_off}	V_{CCA}	V_I = V_O = open, I_O = 0, EN = 0 V, (T_A ≤ 85°C)	1.08 V to 3.6 V	1.08 V to 3.6 V		6	13	μA
		V_I = V_O = open, I_O = 0, EN = 0 V, (T_A ≤ 125°C)				6	26	μA
	V_{CCB}	V_I = V_O = open, I_O = 0, EN = 0 V, (T_A ≤ 85°C)				6	13	μA
		V_I = V_O = open, I_O = 0, EN = 0 V, (T_A ≤ 125°C)				6	26	μA
I_{CCA}		V_I = V_O = open,	1.32 V	1.32 V to 3.6 V		1.5	8	μA
		I_O = 0, EN = V_{CCA},	1.98 V	1.32 V to 3.6 V		2	10	μA

		($T_A \le 85°C$)	3.6 V	1.32 V to 3.6 V		5	14	μA
			0 V	1.32 V to 3.6 V	-2	0		μA
			1.32 V to 3.6 V	0 V		3	13	μA
		$V_I = V_O$ = open, $I_O = 0$, EN = V_{CCA}, ($T_A \le 125°C$)	1.32 V	1.32 V to 3.6 V		1.5	20	μA
			1.98 V	1.32 V to 3.6 V		2	22	μA
			3.6 V	1.32 V to 3.6 V		5	27	μA
			0 V	1.32 V to 3.6 V	-5	0		μA
			1.32 V to 3.6 V	0 V		3	26	μA
I_{CCB}		$V_I = V_O$ = open, $I_O = 0$, EN = V_{CCA}, ($T_A \le 85°C$)	1.32 V to 3.6 V	1.32 V		1.5	8	μA
			1.32 V to 3.6 V	1.98 V		2	10	μA
			1.32 V to 3.6 V	3.6 V		5	13	μA
			1.32 V to 3.6 V	0 V	-2	0		μA
			0 V	1.32 V to 3.6 V		1.8	12.5	μA
		$V_I = V_O$ = open, $I_O = 0$, EN = V_{CCA}, ($T_A \le 125°C$)	1.32 V to 3.6 V	1.32 V		1.5	18	μA
			1.32 V to 3.6 V	1.98 V		2	21	μA
			1.32 V to 3.6 V	3.6 V		5	26	μA
			1.32 V to 3.6 V	0 V	-5	0		μA
			0 V	1.32 V to 3.6 V		1.8	25	μA
$I_{CCA} + I_{CCB}$		$V_I = V_O$ = open, $I_O = 0$, EN = V_{CCA}, ($T_A \le 85°C$)	1.32 V	1.32 V		4	17	μA
			1.98 V	1.98 V		6	20	μA
			3.6 V	3.6 V		11	23	μA
		$V_I = V_O$ = open, $I_O = 0$, EN = V_{CCA}, ($T_A \le 125°C$)	1.32 V	1.32 V		4	35	μA
			1.98 V	1.98 V		6	40	μA
			3.6 V	3.6 V		11	44	μA
R_{ON}	On resistance	V_I = 0.2 V, I_O = 2 mA	1.08 V	1.08 V		35	60	Ω
		V_I = 0.2 V, I_O = 2 mA	1.08 V, 1.8 V	1.8 V, 1.08 V		35	60	Ω
		V_I = 0.2 V, I_O = 3 mA	1.65 V	1.65 V		21	30	Ω
		V_I = 0.2 V, I_O = 2 mA	1.08 V, 3.0 V	3.0 V, 1.08 V		35	60	Ω
		V_I = 0.2 V, I_O = 3 mA	1.65 V, 3.0 V	3.0 V, 1.65 V		21	30	Ω
		V_I = 0.2 V, I_O = 6 mA	3.0 V	3.0 V		15	27	Ω
C_I	EN		3.3 V	3.3 V		2.5		pF
C_{IO}	A or B port		0 V, 1.08 V, 3.6 V	0 V, 1.08 V, 3.6 V		9		pF
t_{RTA}	Time from V_{RTA} to RTA disabling	SDA, SCL = Hi-Z; EN = V_{CC}				80	210	ns

Note:

(1) V_{CCI} is the V_{CC} associated with the input port.

(2) RTA is "rise time accelerator" and FTA is "fall time accelerator".

(3) Specifications subject to change without notice.

6.2. Switching characteristics

The values are obtained under these conditions unless otherwise specified: T_A = -40°C to 125°C.

Symbol	Parameter	Conditions V_{CCA}	Conditions V_{CCB}	Min	Typ	Max	Unit
t_{PLH}	Propagation delay time low-to-high output; from port A to port B	V_{CCA} = 1.08 V	V_{CCB} = 1.08 V		4		ns
			V_{CCB} = 1.8 V		15.5		
			V_{CCB} = 2.5 V		16.5		
			V_{CCB} = 3.6 V		18		
		V_{CCA} = 1.8 V	V_{CCB} = 1.08 V		1.5		ns
			V_{CCB} = 1.8 V		2		
			V_{CCB} = 2.5 V		5		
			V_{CCB} = 3.6 V		10		
		V_{CCA} = 2.5 V	V_{CCB} = 1.08 V		1.5		ns
			V_{CCB} = 1.8 V		1		
			V_{CCB} = 2.5 V		2.5		
			V_{CCB} = 3.6 V		6		
		V_{CCA} = 3.6 V	V_{CCB} = 1.08 V		2		ns
			V_{CCB} = 1.8 V		0.5		
			V_{CCB} = 2.5 V		0.5		
			V_{CCB} = 3.6 V		2		
t_{PHL}	Propagation delay time high-to-low output; from port A to port B	V_{CCA} = 1.08 V	V_{CCB} = 1.08 V		12		ns
			V_{CCB} = 1.8 V		19		
			V_{CCB} = 2.5 V		21		
			V_{CCB} = 3.6 V		22		
		V_{CCA} = 1.8 V	V_{CCB} = 1.08 V		13		ns
			V_{CCB} = 1.8 V		9		
			V_{CCB} = 2.5 V		10.5		
			V_{CCB} = 3.6 V		11.5		
		V_{CCA} = 2.5 V	V_{CCB} = 1.08 V		9		ns
			V_{CCB} = 1.8 V		8.5		
			V_{CCB} = 2.5 V		7.5		
			V_{CCB} = 3.6 V		8.5		
		V_{CCA} = 3.6 V	V_{CCB}= 1.08 V		5		ns
			V_{CCB}= 1.8 V		7		
			V_{CCB}= 2.5 V		6.5		
			V_{CCB}= 3.6 V		6		
t_{PLH}	Propagation delay time low-to-high output; from port B to port A	V_{CCA} = 1.08 V	V_{CCB}= 1.08 V		3		ns
		V_{CCA} = 1.8 V			16		
		V_{CCA} = 2.5 V			16.5		
		V_{CCA} = 3.6 V			16.5		

		V_{CCA} = 1.08 V	V_{CCB} = 1.8 V		1		ns
		V_{CCA} = 1.8 V			1.5		
		V_{CCA} = 2.5 V			5		
		V_{CCA} = 3.6 V			9		
		V_{CCA} = 1.08 V	V_{CCB} = 2.5 V		0.5		ns
		V_{CCA} = 1.8 V			1		
		V_{CCA} = 2.5 V			1		
		V_{CCA} = 3.6 V			5		
		V_{CCA} = 1.08 V	V_{CCB} = 3.6 V		-1		ns
		V_{CCA} = 1.8 V			-1.8		
		V_{CCA} = 2.5 V			-1.5		
		V_{CCA} = 3.6 V			1.5		
t_{PHL}	Propagation delay time high-to-low output; from port B to port A	V_{CCA} = 1.08 V	V_{CCB} = 1.08 V		15		ns
		V_{CCA} = 1.8 V			18.5		
		V_{CCA} = 2.5 V			20		
		V_{CCA} = 3.6 V			22		
		V_{CCA} = 1.08 V	V_{CCB} = 1.8 V		15		ns
		V_{CCA} = 1.8 V			8		
		V_{CCA} = 2.5 V			10.5		
		V_{CCA} = 3.6 V			11.5		
		V_{CCA} = 1.08 V	V_{CCB} = 2.5 V		15.5		ns
		V_{CCA} = 1.8 V			10.5		
		V_{CCA} = 2.5 V			7		
		V_{CCA} = 3.6 V			7.5		
		V_{CCA} = 1.08 V	V_{CCB} = 3.6 V		15.5		ns
		V_{CCA} = 1.8 V			7.5		
		V_{CCA} = 2.5 V			6.5		
		V_{CCA} = 3.6 V			6		
$t_{SK(O)-RISE}$	Rising channel-to-channel skew (propagation)				4.8		ns
$t_{SK(O)-FALL}$	Falling channel-to-channel skew (propagation)				4.8		ns
t_{EN}	From EN to port A or B				80		ns
t_{DIS}	From EN to port A or B				180		ns
t_{RA}	From port B to port A	V_{CCA} = 1.08 V	V_{CCB} = 1.08 V		34		ns
		V_{CCA} = 1.8 V			29		
		V_{CCA} = 2.5 V			31		
		V_{CCA} = 3.6 V			25		
		V_{CCA} = 1.08 V	V_{CCB} = 1.8 V		23		ns
		V_{CCA} = 1.8 V			18		

		V_{CCA} = 2.5 V			20		
		V_{CCA} = 3.6 V			22		
		V_{CCA} = 1.08 V	V_{CCB} = 2.5 V		10		ns
		V_{CCA} = 1.8 V			16		
		V_{CCA} = 2.5 V			15		
		V_{CCA} = 3.6 V			20		
		V_{CCA} = 1.08 V	V_{CCB} = 3.6 V		7		ns
		V_{CCA} = 1.8 V			7		
		V_{CCA} = 2.5 V			12		
		V_{CCA} = 3.6 V			12		
t_{RB}	From port A to port B	V_{CCA} = 1.08 V	V_{CCB} = 1.08 V		33		ns
			V_{CCB} = 1.8 V		31		
			V_{CCB} = 2.5 V		28		
			V_{CCB} = 3.6 V		28.5		
		V_{CCA} = 1.8 V	V_{CCB} = 1.08 V		27		ns
			V_{CCB} = 1.8 V		18.5		
			V_{CCB} = 2.5 V		21		
			V_{CCB} = 3.6 V		22		
		V_{CCA} = 2.5 V	V_{CCB} = 1.08 V		27		ns
			V_{CCB} = 1.8 V		11		
			V_{CCB} = 2.5 V		14		
			V_{CCB} = 3.6 V		20		
		V_{CCA} = 3.6 V	V_{CCB} = 1.08 V		28		ns
			V_{CCB} = 1.8 V		14		
			V_{CCB} = 2.5 V		10		
			V_{CCB} = 3.6 V		12		
t_{FA}	From port B to port A	V_{CCA} = 1.08 V	V_{CCB} = 1.08 V		18.5		ns
		V_{CCA} = 1.8 V			24.5		
		V_{CCA} = 2.5 V			28		
		V_{CCA} = 3.6 V			25		
		V_{CCA} = 1.08 V	V_{CCB} = 1.8 V		24		ns
		V_{CCA} = 1.8 V			12		
		V_{CCA} = 2.5 V			14		
		V_{CCA} = 3.6 V			15		
		V_{CCA} = 1.08 V	V_{CCB} = 2.5 V		23		ns
		V_{CCA} = 1.8 V			12		
		V_{CCA} = 2.5 V			9.5		
		V_{CCA} = 3.6 V			10		
		V_{CCA} = 1.08 V	V_{CCB} = 3.6 V		25		ns

		V_{CCA} = 1.8 V			10		
		V_{CCA} = 2.5 V			9.5		
		V_{CCA} = 3.6 V			9		
t_{FB}	From port A to port B	V_{CCA} = 1.08 V	V_{CCB} = 1.08 V		18.5		ns
			V_{CCB} = 1.8 V		27		
			V_{CCB} = 2.5 V		27		
			V_{CCB} = 3.6 V		28		
		V_{CCA} = 1.8 V	V_{CCB} = 1.08 V		18.5		ns
			V_{CCB} = 1.8 V		12		
			V_{CCB} = 2.5 V		14		
			V_{CCB} = 3.6 V		15		
		V_{CCA} = 2.5 V	V_{CCB} = 1.08 V		17		ns
			V_{CCB} = 1.8 V		12		
			V_{CCB} = 2.5 V		10		
			V_{CCB} = 3.6 V		11.5		
		V_{CCA} = 3.6 V	V_{CCB} = 1.08 V		10		ns
			V_{CCB} = 1.8 V		9.5		
			V_{CCB} = 2.5 V		9		
			V_{CCB} = 3.6 V		9		

Note:

(1) Specifications subject to change without notice.

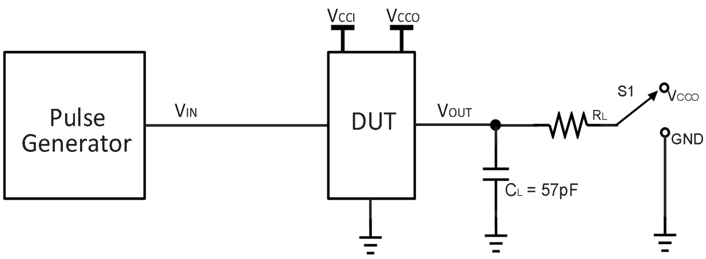


Figure 4. Test circuit for open-drain output

Note:

(1) R_L = 1.3 kΩ.

(2) C_L includes probe and jig capacitance. C_L = 47 pF when on the B-side.

(3) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.

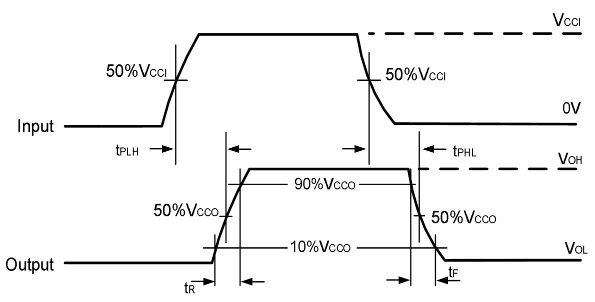


Figure 5. Propagation delay times

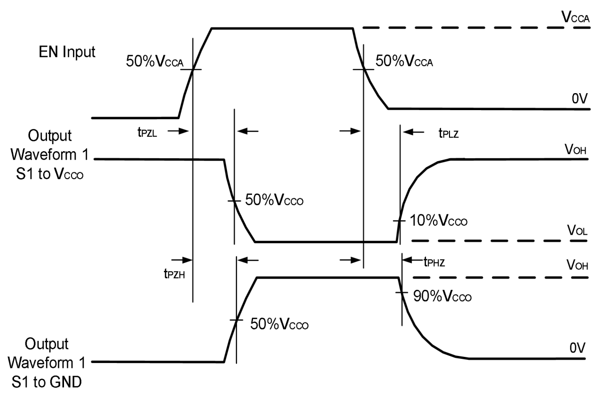


Figure 6. Enable and disable times

Note:

(1) t_{PLH}: Low to high delay time; t_{PHL}: High to low delay time.

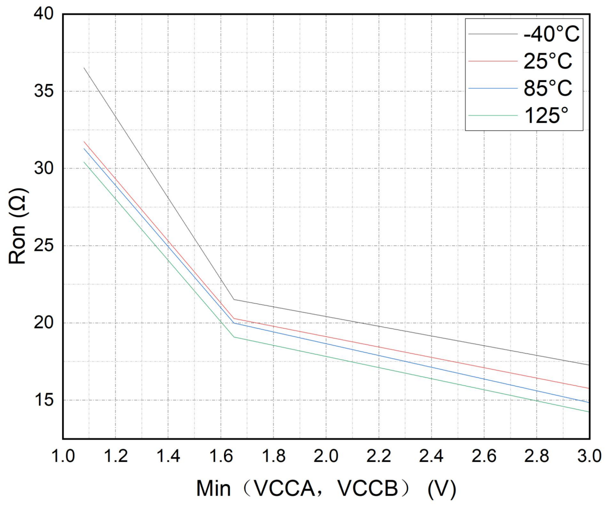
(2) t_{EN}: The larger one between t_{PZL} and t_{PZH}. t_{PZL} is the delay time between EN rising to 50% of V_{CCI} and Vout falling to 50% of V_{CCO}.

(3) V_{OUT} is set to V_{CCO} when EN is logic 0 and will be driven to GND when EN is logic 1. t_{PZH} is the delay time between EN rising to 50% of V_{CCI} and V_{OUT} rising to 50% of V_{CCO}. V_{OUT} is set to GND when EN is logic 0 and will be driven to V_{CCO} when EN is logic 1.

(4) t_{DIS}: The larger one between t_{PLZ} and t_{PHZ}. t_{PLZ} is the delay time between EN falling to 50% of V_{CCI} and V_{OUT} rising to 10% of V_{CCO}. V_{OUT} is set to V_{CCO} when EN is logic 0 and will be driven to GND when EN is logic 1. t_{PHZ} is the delay time between EN falling to 50% of V_{CCI} and V_{OUT} falling to 90% of V_{CCO}. V_{OUT} is set to GND when EN is logic 0 and will be driven to V_{CCO} when EN is logic 1.

(5) V_{CCI} is the V_{CC} associated with the input port. V_{CCO} is the V_{CC} associated with the output port.

7. Typical Characteristics



The Min(V_{CCA}, V_{CCB}) signifies that the lower voltage of V_{CCA} or V_{CCB} is used. As an example, if V_{CCA} = 1.8 V and V_{CCB} = 1.08 V, then the Min(V_{CCA}, V_{CCB}) is 1.08 V.

Figure 7. R_{on} vs. Min(V_{CCA}, V_{CCB})

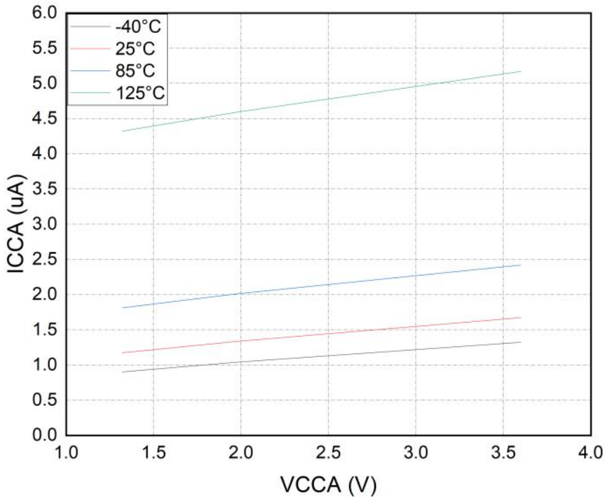


Figure 8. I_{CCA} vs. V_{CCA}

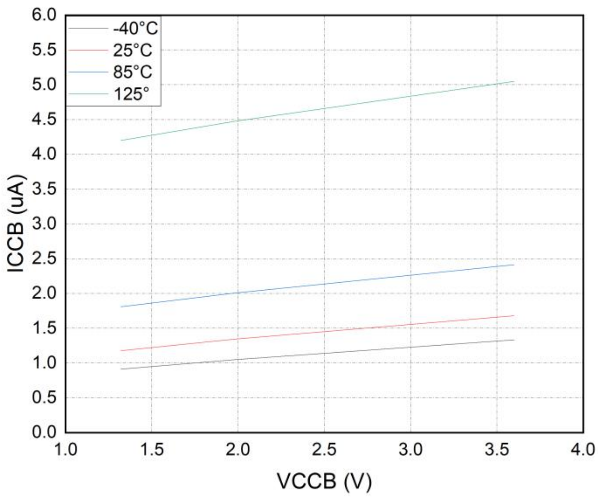
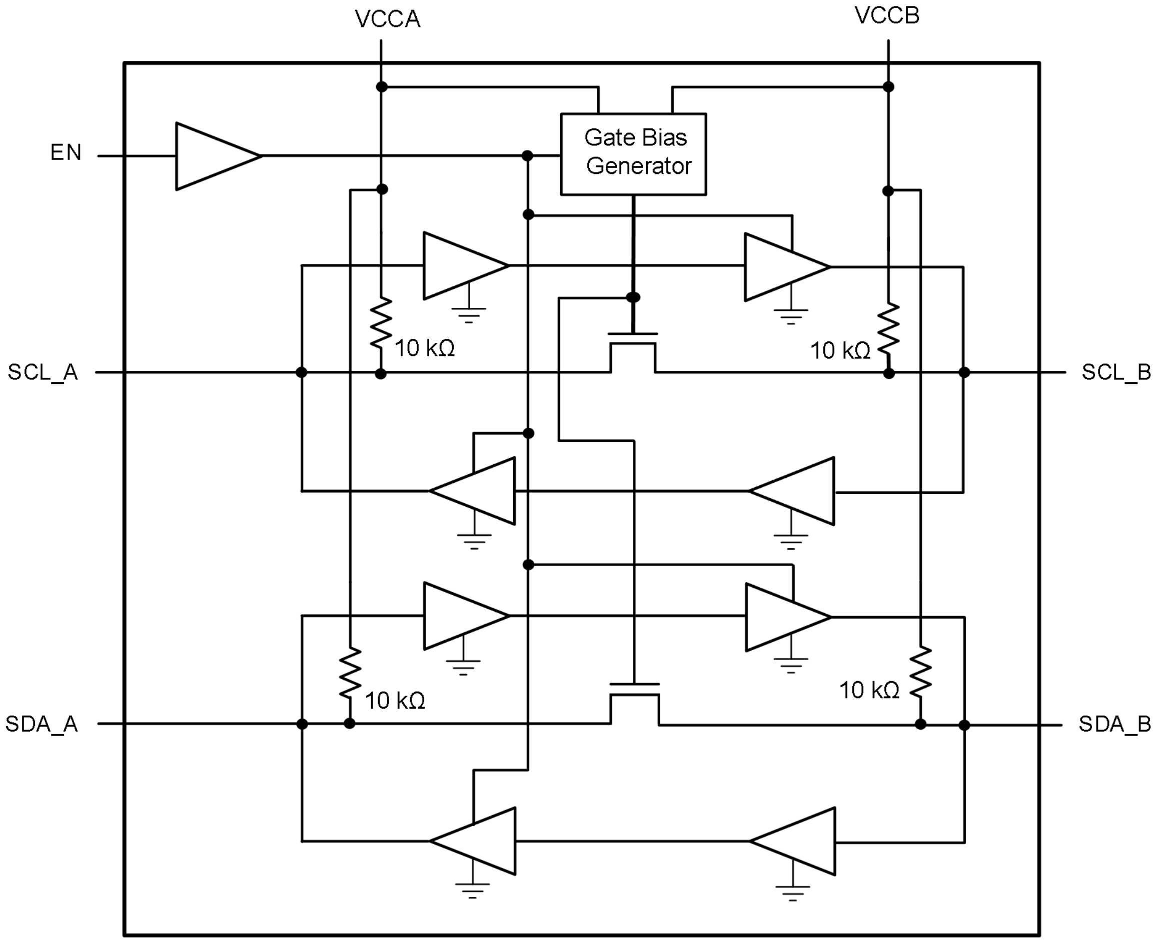


Figure 9. I_{CCB} vs. V_{CCB}

8. Block Diagram



9. Function Description

With rising and falling edge accelerators, the DIO7416 is a 2 bit bidirectional I²C voltage translator with output enable (EN) pin. V_{CCA} and V_{CCB} are able to accept input voltage ranging from 1.08 to 3.6 V. The EN pin can be controlled and set to logic low. A 10 kΩ pull-up resistor of I/O is integrated inside the device.

9.1. Functional modes

The DIO7416 device has two functional modes, enabled and disabled. To disable the device, set the EN input low, which disables the rise time and fall time accelerators and prevents the signal from propagating through the channel. Internal pull-up resistors are not affected by the EN input. Setting the EN input high enables the device.

9.2. Rise/fall time accelerator

Pull-up resistors are included in this bidirectional voltage translation device to provide DC current source capability. The rise and fall time accelerator circuits speed up the output slew rate by monitoring the transitions of the input edges. The output rise time accelerator circuit is used to detect and accelerate the rising edge of the A or B port. During the rising edge of the signal from low to high, the rise time accelerator circuit turns on to increase the current drive capability of the driver. The output falling edge time accelerator circuit is used to detect and accelerate the falling edge of the A or B port. During the falling edge of the signal from high to low, the fall time accelerator is turned on to increase the current drive capability of the driver. This edge rate acceleration improves AC drive by bypassing the internal 10 kΩ pull-up resistors during low-to-high/high-to-low periods.

9.3. Enable and disable

The DIO7416 has an EN input that disables the device by setting EN low, preventing any signal from propagating on the device and entering shutdown mode. This pin is referenced to the V_{CCA} supply. Rise and fall time accelerators are also disabled. However, if the supply is above V_{UVLO}, the internal pull-up resistor will still be enabled. The disable time represents the delay between EN going low and the output is disabled, and the enable time represents the amount of time the user must allow a trigger circuit to operate after EN is high.

9.4. Pull-up resistors on I/O lines

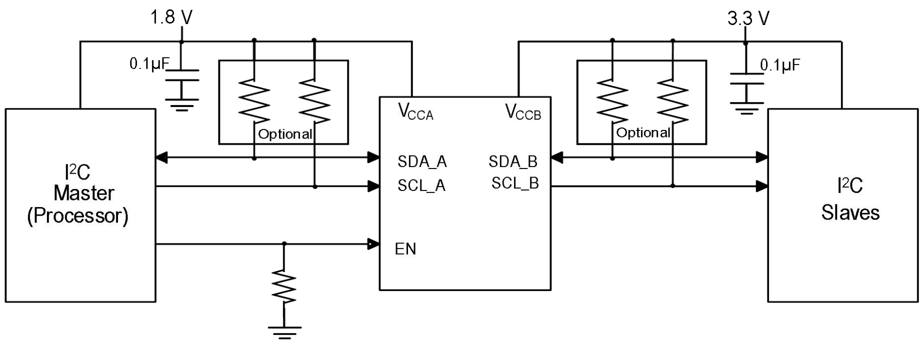
Each A port I/O has an internal 10 kΩ pull-up resistor to VCCA and each B port I/O has an internal 10 kΩ pull-up resistor to VCCB. If a smaller pull-up resistor value is required, an external resistor (in parallel with the internal 10 kΩ resistor) must be added to VCCA or VCCB from the input/output. The pull-up resistors inside the device are controlled by their respective power supplies, and the resistors are reverse biased protected, so if the power is turned off, current cannot flow back through the resistors to the power supply. If the supply is above V_{UVLO}, the pull-up resistor on one side of it will be enabled.

10. Application Information

Important notice: Validation and testing are the most reliable ways to confirm system functionality. The application information is not part of the specification and is for reference purposes only.

The DIO7416 can be used in level conversion applications for interfacing devices or systems operating under different interface voltages.

10.1. Application examples



Note:
(1) EN is referenced to V_{CCA}

10.2. Design requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design parameters

Design Parameter	Example Value
Input voltage range	1.08 V to 3.6 V
Output voltage range	1.08 V to 3.6 V

To start the design process, determine the following:

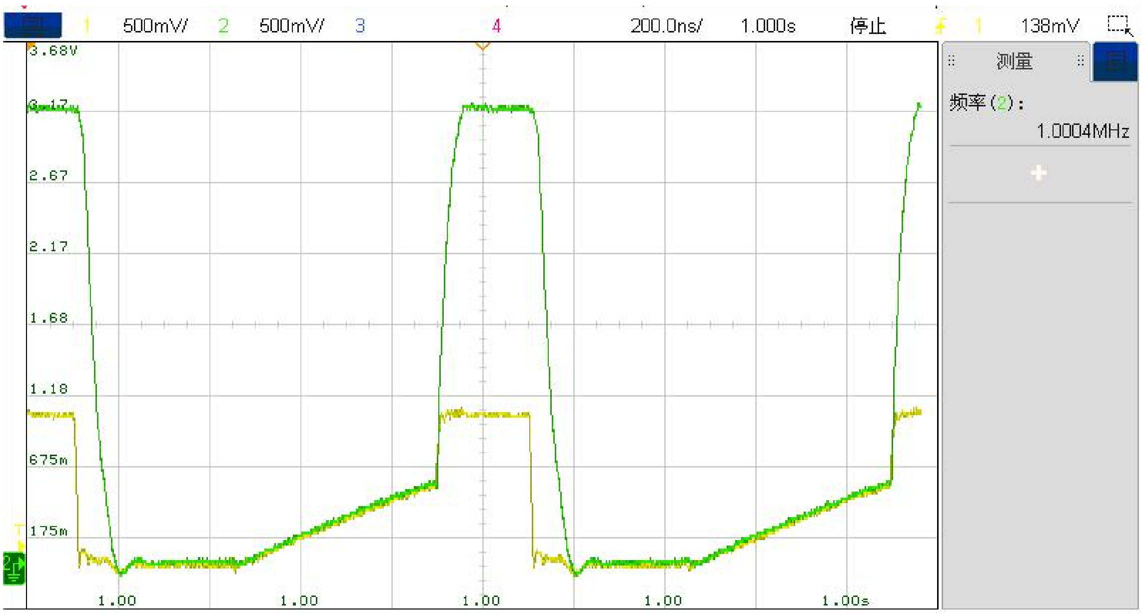
- Input voltage range
  Use the supply voltage of the device driving the DIO7416 device to determine the input voltage range. For a valid logic high, this value must exceed the V_{IH} of the input port. For a valid logic low, this value must be less than the V_{IL} of the input port.
- Output voltage range
  Determining the output voltage range by using the supply voltage of the device driven by the DIO7416 device.The DIO7416 device has 10 kΩ internal pull-up resistors. If necessary, add external pull-up resistors to reduce the total RC of the signal traces.

- Startup considerations with large capacitive load mismatches

  Due to the FET based architecture of this translator, there are some considerations a designer must be aware of during powering up with large differences in capacitance between the sides. If one supply with smaller capacitance is already powered up, and the other is ramping (with EN pin high), the side with the heavier load can ramp slower than the power supply ramp, due to only having an internal 10 kΩ pull up resistor. In this situation, once the rising POR threshold is met, the device enables all circuitry. If the heavy capacitance side has not yet risen above about 70% of supply, the device determines this as low, and briefly turns on the fall time accelerators to propagate a low. Once the fall time accelerator has timed out, the signals rise and sit idle high.

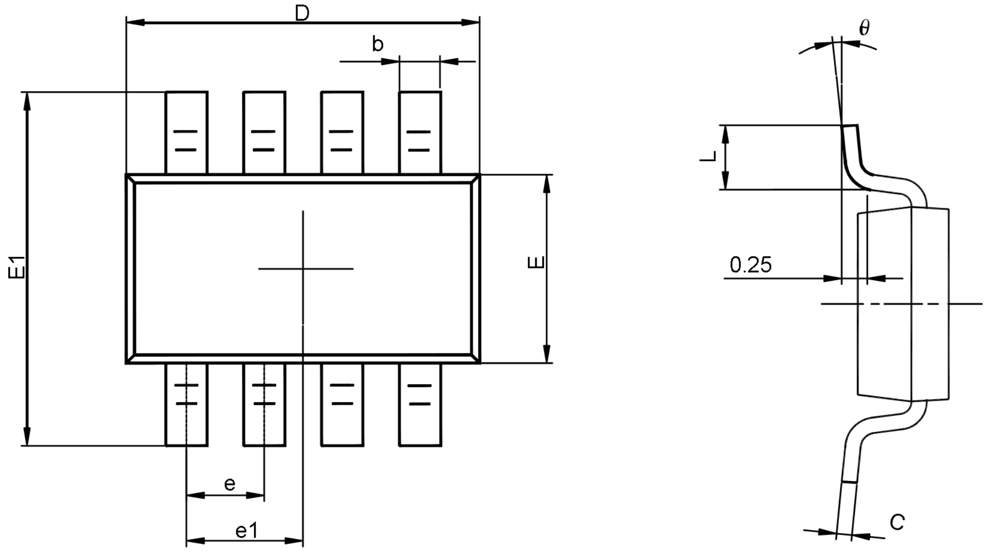
  This phenomenon can be eliminated by holding the EN pin low (disabled) until all supplies and busses have ramped up, since this explicitly disables the bus acceleration circuitry until the bus has completed power up. Slower supply ramps also help reduce this because the bus voltage follows the supply closer if the ramp is slow.

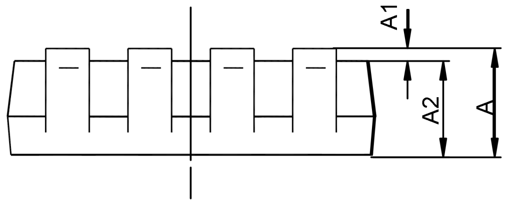
10.3. Application curve



11. Physical Dimensions

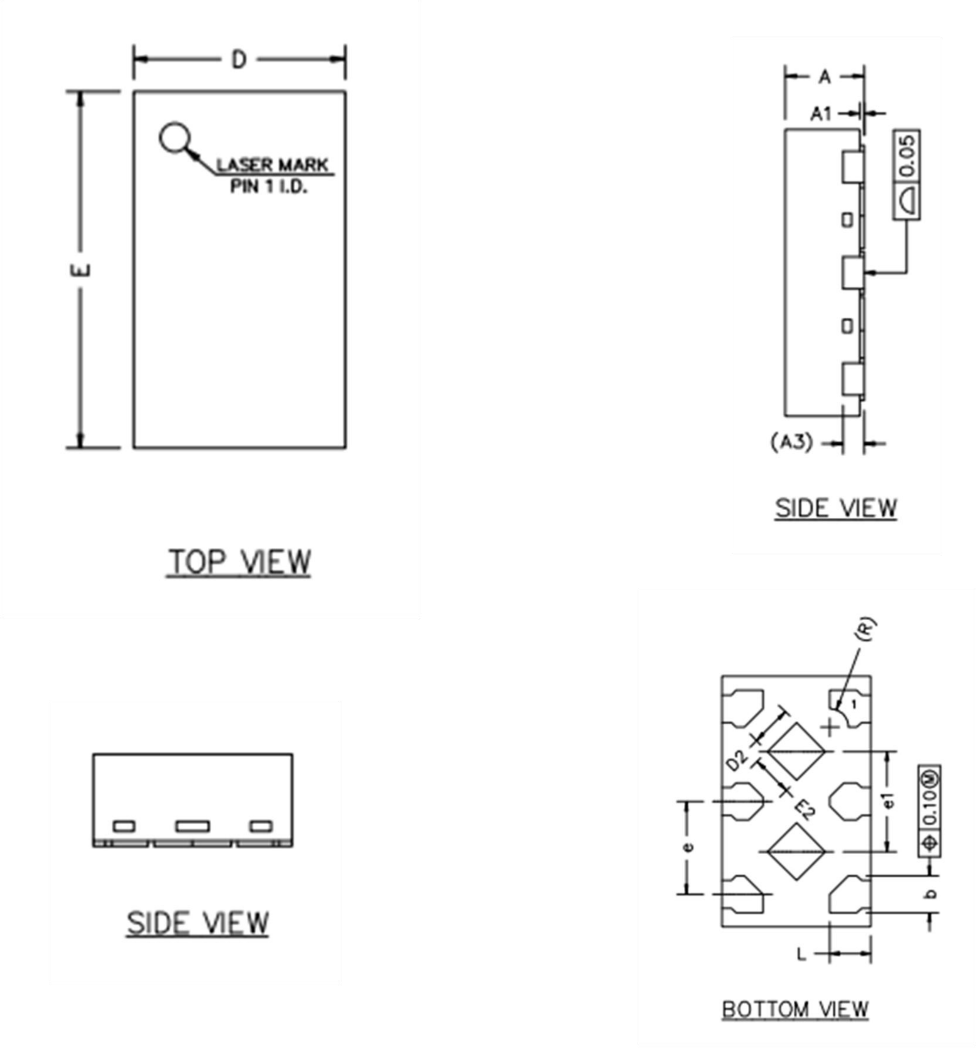
11.1. TSOT23-8





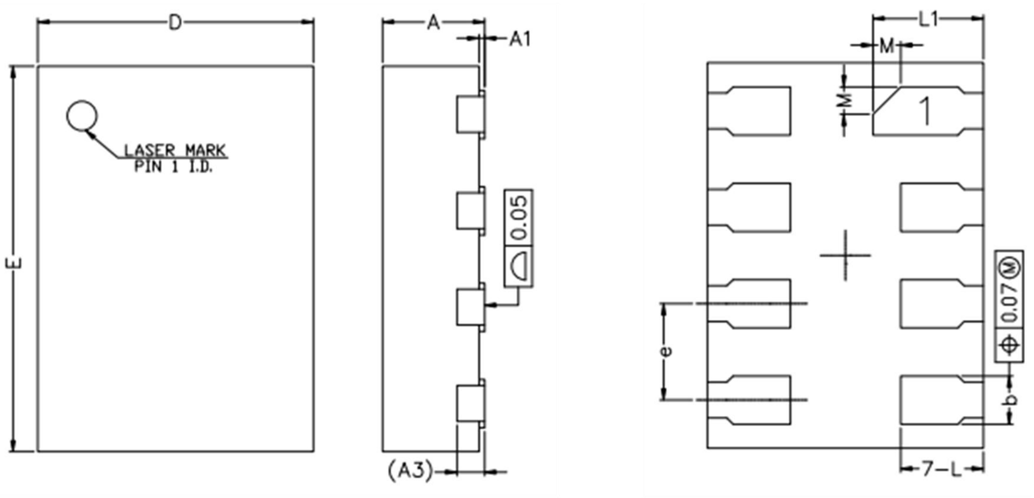
Common Dimensions (Units of measure = Millimeter)		
Symbol	**Min**	**Max**
A	0.700	0.900
A1	0.000	0.100
A2	0.700	0.800
b	0.300	0.500
c	0.080	0.200
D	2.820	3.020
E	1.600	1.700
E1	2.650	2.950
e	0.65 BSC	
e1	0.975 BSC	
L	0.300	0.600
θ	0°	8°

11.2. DFN1.35*0.8-8

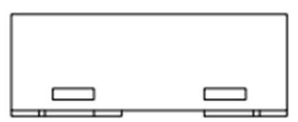


Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.34	0.37	0.40
A1	0.00	0.02	0.05
A3		0.10 REF	
b	0.15	0.20	0.25
D	0.75	0.80	0.85
E	1.30	1.35	1.40
D2	0.17	0.22	0.27
E2	0.17	0.22	0.27
e	0.40	0.50	0.60
e1	0.44	0.54	0.64
L	0.17	0.22	0.27
R		0.10 REF	

11.3. DFN1.4*1-8



TOP VIEW SIDE VIEW BOTTOM VIEW



SIDE VIEW

Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.34	0.37	0.40
A1	0.00	0.02	0.05
A3	0.100 REF		
b	0.125	0.175	0.225
D	0.90	1.00	1.10
E	1.30	1.40	1.50
e	0.30	0.35	0.40
L	0.25	0.30	0.35
L1	0.35	0.40	0.45
M	0.10 REF		

Disclaimer

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